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INTEGRATION, the VLSI journal 41 (2008) 210–218
INTEGRATION the VLSI journal
www.elsevier.com/locate/vlsi

An efficient terminal and model order reduction algorithm ☆

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Received 2 November 2006; received in revised form 29 May 2007; accepted 30 May 2007

Abstract

The paper proposes an efficient terminal and model order reduction method for compact modeling of interconnect circuits with many terminals. The new method is inspired by the recently proposed terminal reduction method, SVDMOR [P. Feldmann, F. Liu, Sparse and efficient reduced order modeling of linear subcircuits with large number of terminals, in: Proceedings of the International Conference on Computer Aided Design (ICCAD), 2004, pp. 88–92]. But different from SVDMOR, the new method considers higher order moment information for terminal responses during the terminal reduction and separately applies singular value decomposition (SVD) on both input and output terminals for low-rank approximations. This is in contrast to the SVDMOR method where input and output terminal responses are approximated by SVD at the same time, which can lead to large errors when the numbers of inputs and outputs are quite different. We analyze the passivity requirements for SVD-based terminal and model order reduction and show that the combined passive terminal and MOR using SVD method will not lead an effective terminal reduction in general. Our experimental results show that the proposed ESVDMOR method outperforms the SVDMOR method in terms of accuracy for the same reduced model sizes when the numbers of input and output terminals are quite different.

Keywords: Model order reduction; Terminal reduction; Interconnect

1. Introduction

Compact modeling of passive RLC interconnect circuits by model order reduction (MOR) techniques have been intensively studied in the past as a result of the urgent need to reduce the increasing circuit complexity. The most efficient and successful algorithms are based on Krylov subspace projection methods [3–7].

But existing MOR methods mainly focus on the reduction of the internal nodes. When there are many terminal nodes, the efficiency of the existing Krylov subspace methods will degrade significantly. There are several reasons for the low efficiency. First, the time complexity of the projection-based methods is proportional to the number of terminals of the circuits as moments excited by every terminal need to be computed and matrix-valued transfer functions are generated. Second, the poles of the reduced models are linearly increasing with the number of terminals, which make the reduced models much larger than necessary or even larger than the original models with dense matrices.

One way to mitigate this problem is by means of combined terminal reduction and MOR. Terminal or port reduction is to reduce the number of terminals/ports of given circuits under the assumption that some terminals are similar or correlated in terms of their timing information. Such similar or correlated terminals are justified by the facts that many terminals are indeed close to each other structurally during the mathematic approximation steps involved (finite element, finite difference, etc.). So their timing responses are similar also. Several terminal reduction algorithms have been proposed [8,1,9]. Recently,

☆Some preliminary results of this paper were presented at IEEE International Workshop on Behavioral Modeling and Simulation (BMAS'06) [2], San Jose, CA. This work was sponsored by NSF CAREER Award CCF-0448534, NSF Grant OISE-0623038 and University of California MICRO Program (#04-088 and #05-111) via Cadence Design System Inc.
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doi:10.1016/j.vlsi.2007.05.004

a terminal reduction method, called SVDMOR, has been proposed [8,1], which is based on the low-rank approximation of input and output position matrices before the MOR process. The low-rank approximation can be carried out on the DC [8] or a specific order of moment [1]. However, our experimental results show that SVDMOR does not perform well when the numbers of the input and output terminals are quite different. The singular value decomposition (SVD) approximation is performed on the block moment matrix, which represents the response for both input and output terminals at the same time. So the approximation will not work well when the numbers of inputs and outputs are dramatically different. Basically the low-rank approximation or the number of independent terminals (or their correlation) may not be same for both input and output terminals. This typically happens when the numbers of input and output terminals are quite different. This is the case for many clock distribution networks and the signal nets in the memory circuits (word lines and bit lines) where you have a few driver (inputs) and many sinks (outputs).

Terminal reduction by SVD-based rank computation and terminal clustering via K-means method on terminal timing was proposed in [9]. The clustering is based on the higher order timing information. The method uses representative terminals to represent the reduced terminals. This method is very suitable for circuits with separate input and output terminals. But this method loses the timing difference between the representative terminals and their suppressed terminals.

In this paper, we propose a new SVD-based terminal reduction algorithm, called Extended SVDMOR or ESVDMOR method. Our approach is based on the SVDMOR method [1]. But the new method uses higher order moment information during the SVD approximation process to ensure that we can find the better correlations between input and output terminals. Also the ESVDMOR performs the SVD on input and output moment responses separately so that it can exploit the input and output correlations separately when they are different. We also show that by using the projection-based MOR method and the SVD-based terminal reduction framework, passivity requirements, which retain all the terminals as both input and output terminals, will not lead to effective terminal reduction. As a result, separation of the terminals into input and output is necessary for effective terminal reductions for SVDMOR-like methods. Experimental results show that ESVDMOR outperforms SVDMOR in terms of accuracy for the same size of the reduced models when the input and output terminals are quite different.

The paper is organized as follows. In Section 2, we review the SVDMOR method for model reduction with large number of terminals and show its weakness with experimental results. Section 3 presents our new ESVDMOR method. We first present main idea of the new terminal reduction method. Then we show how higher order moment information is represented for input and output terminal responses. After that we discuss some practical issues associated with the implementation, and present the whole terminal reduction and MOR flow of ESVDMOR. We also present a short discussion on the passivity issue in terminal reduction 4. The experimental results and conclusions are presented in Sections 5 and 6, respectively.

2. Review of the SVDMOR method

In this section, we briefly review the SVDMOR method for terminal reduction, which was proposed recently for reducing the terminals of interconnect circuits [8,1].[1]

For a linear RLC interconnect network with p input and q output terminals, we can apply modified nodal analysis to formulate it into the state space equation form

$$G\mathbf{x}(t) + C\dot{\mathbf{x}}(t) = B\mathbf{u}(t),$$

$$\mathbf{y}(t) = L^{\mathrm{T}}\mathbf{x}(t), \tag{1}$$

where $G \in R^{n\times n}$ and $C \in R^{n\times n}$ are the conductive and storage element matrices. $L \in R^{n\times q}$ and $B \in R^{n\times p}$ are the output and input position matrices. $\mathbf{u}(t) \in R^p$ and $\mathbf{y}(t) \in R^q$ are the inputs and outputs, respectively. State variables $\mathbf{x}(t) \in R^n$ can be nodal voltages or branch currents of the linear circuit.

The circuit transfer function is

$$H(s) = L^{\mathrm{T}}(G + Cs)^{-1}B. \tag{2}$$

Then the ith block moment of the system is defined as

$$\mathbf{m}_i = L^{\mathrm{T}}(-G^{-1}C)^i G^{-1}B, \tag{3}$$

where $\mathbf{m}_i$ is a $q \times p$ matrix.

The block moment $\mathbf{m}_i$ can be directly computed in a recursive way

$$\begin{aligned} &\mathbf{x}_0 = G^{-1}B, && \mathbf{m}_0 = L^{\mathrm{T}}\mathbf{x}_0,\\ &\mathbf{x}_1 = -G^{-1}C\mathbf{x}_0, && \mathbf{m}_1 = L^{\mathrm{T}}\mathbf{x}_1,\\ &\vdots && \vdots\\ &\mathbf{x}_i = -G^{-1}C\mathbf{x}_{i-1}, && \mathbf{m}_i = L^{\mathrm{T}}\mathbf{x}_i. \end{aligned} \tag{4}$$

SVDMOR basically exploits the fact that many terminals are not independent or are correlated in terms of their timing information, which can be reflected in their frequency domain moments. As a result, we can perform the SVD on a block moment of a specific order. For instance, if we perform the SVD on 0th order block moment (DC response) $\mathbf{m}_0$, we have

$$\mathbf{m}_0 = L^{\mathrm{T}}G^{-1}B = U\Sigma V^{\mathrm{T}}, \tag{5}$$

where U and V are orthogonal matrices and Σ is a diagonal matrix with singular values in the diagonal in a decreasing order. If there are k dominant singular values

[1] The algorithm proposed in [1] was also called *RecMOR*, which is an improved version of the SVDMOR algorithm in [8]. In this paper, we refer the two algorithms as SVRMOR only to simplify our presentation.

then we can use a k-rank matrix (a $k \times k$ full rank matrix) to approximate the original $\mathbf{m}_0$ based on the SVD theory as

$$\mathbf{m}_0 = U\Sigma V^{\mathrm{T}} \approx U_k \Sigma_k V_k^{\mathrm{T}}. \quad (6)$$

Notice that $U_k \in R^{q\times k}$, $V_k^{\mathrm{T}} \in R^{k\times p}$ and $\Sigma_k \in R^{k\times k}$. After this, we can have the following expressions:

$$B = B_{\mathrm{b}} V_k^{\mathrm{T}},$$

$$L^{\mathrm{T}} = U_k L_{\mathrm{c}}^{\mathrm{T}}, \quad (7)$$

where $B_{\mathrm{b}} \in R^{n\times k}$ and $L_{\mathrm{c}} \in R^{n\times k}$ are obtained using the Moore–Penrose pseudoinverses of V_k and U_k, respectively.

$$B_{\mathrm{b}} = BV_k(V_k^{\mathrm{T}}V_k)^{-1},$$

$$L_{\mathrm{c}} = LU_k(U_k^{\mathrm{T}}U_k)^{-1}. \quad (8)$$

The circuit transfer function now becomes

$$H(s) = U_k L_{\mathrm{c}}^{\mathrm{T}}(G + Cs)^{-1} B_{\mathrm{b}} V_k^{\mathrm{T}}. \quad (9)$$

Notice that the transfer function $H_r(s)$, which is inside (9)

$$H_r(s) = L_{\mathrm{c}}^{\mathrm{T}}(G + Cs)^{-1} B_{\mathrm{b}}, \quad (10)$$

is a $k \times k$ matrix transfer function, which actually is the terminal-reduced transfer function of (2) and can be reduced by the traditional Krylov subspace based MOR methods. If the reduced transfer function of (10) is $\hat{H}_r(s)$, then the final order reduced transfer function is

$$\hat{H}(s) = U_k \hat{H}_r(s) V_k^{\mathrm{T}}. \quad (11)$$

SVDMOR performs the terminal reduction on the both input and output responses at the same time. This reflects on the $q \times p$ block moment $\mathbf{m}_i$, where the column vectors of $\mathbf{m}_i$ represent the ith moments from the p inputs and row vectors of $\mathbf{m}_i$ represent the ith moments at the q outputs. The k-rank approximation in (6) can approximate well only one smaller-rank space spanned by either the column vectors or row vectors of $\mathbf{m}_i$. If two spaces have quite different ranks caused by significant different numbers of input and output terminals, the approximation will not work well. This reflects the accuracy loss at the high frequency.

Fig. 1 shows the SVDMOR reduction results for an interconnect circuit, *net1026*, in frequency domain. This circuit has 6 inputs and 256 outputs. We perform both terminal reduction and following Krylov subspace based MOR. SVDMOR based on $\mathbf{m}_0$ reduces the terminals to only one input and one output terminals based on the singular values as shown in Table 2. From Fig. 1 we can see that results from SVDMOR are quite different from the original circuit at high frequencies (this is not caused by the MOR operation as shown in the experimental section).

Accuracy loss at high frequency after terminal reduction reflects the fact that the input and output terminals have different numbers of independent terminals. But SVDMOR can only approximate well one type of terminals as the SVD process is performed on the specific order of block moment matrix, which consists of both input and output terminal response information.

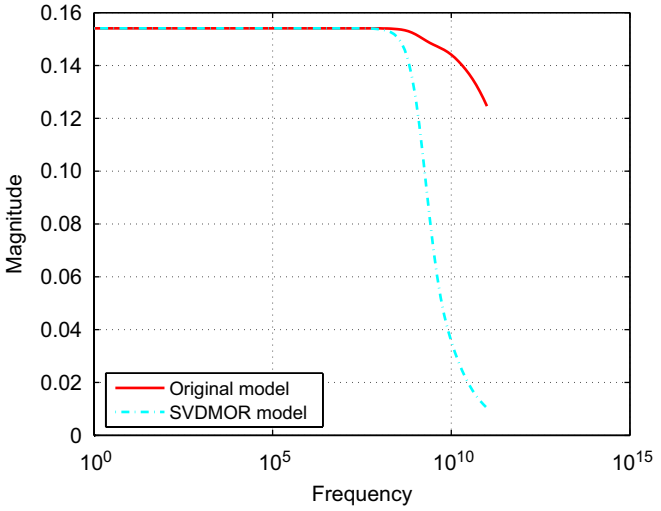

Fig. 1. Frequency responses from SVDMOR method for *net1026* circuit.

In the next section, we show how this problem can be mitigated by the proposed ESVDMOR method using the higher order moment information.

3. The new extended SVD-based (ESVDMOR) method

In this section, we present our new terminal and MOR algorithm, ESVDMOR. The basic idea of the new method is to perform the SVD low-rank approximation for the input and output terminals *separately* and use higher order moment information during the SVD approximation to find true terminal independency to ensure the accuracy of the reduced model.

3.1. The new terminal reduction algorithm

The main idea of the new terminal reduction method is to perform the SVD approximation on the input and output moment response *separately* with the use of the high order moment information. We basically follow the terminal reduction framework of SVDMOR method [1] but with different moment matrices. But we improve the efficiency of SVDMOR by saving one computation step as shown later.

The major problem for the SVDMOR method is that both input and output responses are considered at the same time during SVD as a result of using the specific order of block moments $\mathbf{m}_i$. So SVDMOR cannot accommodate higher order moment information. To mitigate this problem, we create new moment matrices for input and output terminals separately. In this way, we can use higher order moments during the SVD process for input and output responses.

Specifically, let us look at one specific moment block first. For a general linear system with p inputs and q

outputs, each moment $\mathbf{m}_i$ is a $q \times p$ matrix,

$$\mathbf{m}_i = \begin{bmatrix} m^i_{1,1} & m^i_{1,2} & \cdots & m^i_{1,p} \\ m^i_{2,1} & m^i_{2,2} & \cdots & m^i_{2,p} \\ \vdots & \vdots & & \vdots \\ m^i_{q,1} & m^i_{q,2} & \cdots & m^i_{q,p} \end{bmatrix}, \tag{12}$$

where each column j in $\mathbf{m}_i$ represents the moment vector of all output terminals owning to the input terminal j and each row k in $\mathbf{m}_i$ represents the moment vector at the output terminal k owning to all input terminals. Then a moment matrix, which consists of 0th to $(r-1)$th order of block moments, can be written as

$$M = [\mathbf{m}_0 \ \ \mathbf{m}_1 \ \ \cdots \ \ \mathbf{m}_{r-1}]. \tag{13}$$

In order to perform terminal reduction for inputs and outputs separately, different moment matrices are constructed. Specifically for the output terminal reduction, we define the *output moment response matrix* M_{O} as

$$M_{\mathrm{O}} = \begin{bmatrix} \mathbf{m}_0^{\mathrm{T}} \\ \mathbf{m}_1^{\mathrm{T}} \\ \vdots \\ \mathbf{m}_{r-1}^{\mathrm{T}} \end{bmatrix}, \tag{14}$$

where M_{O} is a $rp \times q$ matrix and each column j represents a moment series of output node j owning to all input's impulse stimuli. Typically we expect the number of rows in M_{O} will be larger than the number of its columns so that the rank of the M_{O} is determined by the column vectors of M_{O}, which represents the q output terminals.

Similarly, for input terminal reduction, the *input moment response matrix* M_{I} is defined as

$$M_{\mathrm{I}} = \begin{bmatrix} \mathbf{m}_0 \\ \mathbf{m}_1 \\ \vdots \\ \mathbf{m}_{r-1} \end{bmatrix}, \tag{15}$$

where M_{I} is a $rq \times p$ and each column k represents a moment series at all output's nodes owning to an input node k.

For both M_{O} and M_{I}, we require that the column vectors represent the responses for outputs owning to inputs, respectively, and the rows in both M_{O} and M_{I} will lose the terminal-related physic information as they represent the different orders of moments.

Notice that it is well known that explicit evaluations of high order moments will cause numerical ill-condition problem [3]. But for our work, this problem is less concerned. First we perform the SVD on the input and output moment matrices. So ill-conditioning is not a problem as SVD is specifically designed for handling ill-conditioning (low-rank) matrices. Second, we know that high order moments will lose the information about the non-dominant poles numerically. This actually does not cause significant problem as we do not compute the poles here. Instead, we try to find the low-rank approximation. Also the moments come from the Taylor expansion of the transfer function. The higher order moments, the less important they are. Actually, even with a few more orders of moments, we are better off than that the SVDMOR, which only uses one specific order of moments (saying DC moment). In practice, we do not need many high order moments (usually the number of moments is less than 10).

Next, we perform SVD to both input moment response matrix M_{I} and output moment response matrix M_{O}.

$$M_{\mathrm{I}} = U_{\mathrm{I}}\Sigma_{\mathrm{I}}V_{\mathrm{I}}^{\mathrm{T}} \approx U_{\mathrm{I}_{k_i}}\Sigma_{k_i}V_{\mathrm{I}_{k_i}}^{\mathrm{T}},$$

$$M_{\mathrm{O}} = U_{\mathrm{O}}\Sigma_{\mathrm{O}}V_{\mathrm{O}}^{\mathrm{T}} \approx U_{\mathrm{O}_{k_o}}\Sigma_{k_o}V_{\mathrm{O}_{k_o}}^{\mathrm{T}}, \tag{16}$$

where Σ_{k_i} is a $k_i \times k_i$ diagonal matrix and k_i is the number of significant singular values for matrix M_{I}. $V_{\mathrm{I}_{k_i}}^{\mathrm{T}}$ is a $k_i \times p$ matrix. Similarly, Σ_{k_o} is a $k_o \times k_o$ diagonal matrix and k_o is the number of significant singular values for matrix M_{O}. $V_{\mathrm{O}_{k_o}}^{\mathrm{T}}$ is a $k_o \times q$ matrix.

Then we can perform the low-rank approximation for the input and output position matrix B and C, respectively.

$$B = B_r V_{\mathrm{I}_{k_i}}^{\mathrm{T}},$$

$$L^{\mathrm{T}} = V_{\mathrm{O}_{k_o}}L_r^{\mathrm{T}}, \tag{17}$$

where $B_r \in R^{n\times k_i}$ and $L_r^{\mathrm{T}} \in R^{k_o\times n}$ are obtained by computing the Moore–Penrose pseudoinverses of $V_{\mathrm{I}_{k_i}}$ and $V_{\mathrm{O}_{k_o}}$, respectively.

$$B_r = BV_{\mathrm{I}_{k_i}}(V_{\mathrm{I}_{k_i}}^{\mathrm{T}}V_{\mathrm{I}_{k_i}})^{-1},$$

$$L_r^{\mathrm{T}} = (V_{\mathrm{O}_{k_o}}^{\mathrm{T}}V_{\mathrm{O}_{k_o}})^{-1}V_{\mathrm{O}_{k_o}}^{\mathrm{T}}L^{\mathrm{T}}. \tag{18}$$

Notice that both $V_{\mathrm{I}_{k_i}}$ and $V_{\mathrm{O}_{k_o}}$ are orthonormal matrices, i.e. $V_{\mathrm{I}_{k_i}}^{\mathrm{T}}V_{\mathrm{I}_{k_i}} = I$ and $V_{\mathrm{O}_{k_o}}^{\mathrm{T}}V_{\mathrm{O}_{k_o}} = I$. Therefore, (18) can be further simplified as

$$B_r = BV_{\mathrm{I}_{k_i}},$$

$$L_r^{\mathrm{T}} = V_{\mathrm{O}_{k_o}}^{\mathrm{T}}L^{\mathrm{T}}. \tag{19}$$

So we save one computation step compared to the SVDMOR method [1]. The proposed utilization of the orthonormality can be also used in SVDMOR method.

As a result, the circuit transfer function now becomes

$$H(s) = V_{\mathrm{O}_{k_o}}L_r^{\mathrm{T}}(G+Cs)^{-1}B_rV_{\mathrm{I}_{k_i}}^{\mathrm{T}}. \tag{20}$$

Consequently we get a terminal reduced subsystem with transfer function $H_r(s)$.

$$H_r(s) = L_r^{\mathrm{T}}(G+Cs)^{-1}B_r. \tag{21}$$

For this subsystem, the standard MOR techniques [3–7] can now be applied.

Consider both terminal and model reductions, we can obtain the order reduced transfer function $\hat{H}_r(s)$,

$$\hat{H}_r(s) = \hat{L}_r^{\mathrm{T}}(\hat{G} + \hat{C}s)^{-1}\hat{B}_r, \tag{22}$$

where

$$\hat{G} = V^{\mathrm{T}}GV; \quad \hat{C} = V^{\mathrm{T}}CV,$$

$$\hat{B}_r = V^{\mathrm{T}}BV_{\mathrm{I}_{k_i}}; \quad \hat{L}_r^{\mathrm{T}} = V_{\mathrm{O}_{k_o}}^{\mathrm{T}}L^{\mathrm{T}}V, \tag{23}$$

where V is the projection matrix for reducing system of (21).

The final reduced transfer function becomes

$$\hat{H}(s) = V_{\mathrm{O}_{k_o}}\hat{L}_r^{\mathrm{T}}(\hat{G} + \hat{C}s)^{-1}\hat{B}_r V_{\mathrm{I}_{k_i}}^{\mathrm{T}}. \tag{24}$$

3.2. Practical observation and considerations

One important issue for the proposed method is to select the proper order of moments for the terminal reduction and the model reduction.

For the terminal reduction, our experimental results show that when the ranks of input and output moment response matrices are similar, SVDMOR typically performs well also. For the RC circuits tested in the experimental result section, we observe that the DC or first moments are typically sufficient for determining the ranks of input and output moment response matrices when they are similar. However, when the ranks of the input and output moment response matrices are different, higher order moment information can be useful for determining the true ranks of input and output moment response matrices. This typically happens when the input and output terminal numbers are quite different and SVDMOR does not perform well. Specifically, we use the following rule:

$$r \leqslant \left\lceil \frac{q}{p} \right\rceil \quad \text{for } M_{\mathrm{O}} \text{ when } q > p, \tag{25}$$

$$r \leqslant \left\lceil \frac{p}{q} \right\rceil \quad \text{for } M_{\mathrm{I}} \text{ when } p > q, \tag{26}$$

where r is the order of moments used. For M_{O}, if output terminal number q is larger than the input terminal number p, we need to add all moments up to $(r-1)$th order such that we have an equal or larger number of rows than the number of columns in M_{O}. This is true for M_{I} when the input terminal number p is larger than the output terminal number q. This determination process considers the worst case that all terminals are independent.

When $p = q$, r is set to 1 to satisfy (25) and (26). Under this condition, the higher order moment information is not necessary.

ESVDMOR ALGORITHM:

Input : G, C, B matrices

Output : $\hat{H}$ (s) transfer function

1. Compute the block moments $\mathbf{m}_i$ up to the $(r-1)$th order using (4).
2. Construct the input and the output moment response matrices defined in (15) and (14) respectively.
3. Perform the SVD-based low-rank approximation on the position matrices B and L^T in (1) using (17) and (18).
4. Perform the normal Krylov subspace based MOR on the terminal reduced system (21) and perform the transformations using (23).
5. Compute the final reduced system $\hat{H}(s)$ using (24).

Fig. 2. ESVDMOR algorithm flow.

3.3. ESVDMOR algorithm flow

In this subsection, we give the whole combined terminal and model order reduction flow of the ESVDMOR method shown in Fig. 2.

4. Passivity discussions and terminal reduction effectiveness

For MOR, the input and output position matrices B and L^{T} are required to be the same for ensuring passivity in projection-based reduction framework. When B and L^{T} are not the same, passivity may not be ensured with existing projection methods. We notice that reduction by truncation balanced realization (TBR) can make passive reduction of RLCK circuits with different B and L^{T} [10]. But passive TBR is a very expensive process and does not scale to solve large problems.

One may think that one can make all the terminals as bidirectional (both input and output) ones by making B and L^{T} the same. But we show in the experimental section, such a simple strategy for enforcing passivity may significantly reduce the terminal reduction qualities. One obvious reason for this degradation is that many output terminals now become input terminals. As a result, we require that the input impedance of a terminal will be equal to its transfer function to another terminal if the two terminals are same, which is very unlikely. This is reflected in the fact that the resulting moment matrices have almost full rank as shown in example circuits (we only show one example but we observe this for all the examples we have).

Considering the terminal reduction, passivity further requires that B_r and L_r^{T} are the same, and $V_{\mathrm{O}_{k_o}}$ and $V_{\mathrm{I}_{k_i}}$ are identical as well as the result of the requirements of the congruence transformation. As a result, the moments $\mathbf{m}_i$ must be symmetric. This is required for both SVDMOR and ESVDMOR methods. It can be proved that when the inputs to the original models consist of only current sources or voltage sources for RLCK circuits, $\mathbf{m}_i$ is symmetric. If both current and voltage sources are present, $\mathbf{m}_i$ will not be symmetric and terminal reduction by both SVDMOR and ESVDMOR will not ensure the passivity.

Table 1
The singular values of DC moment, input moment matrix and output moment matrix of the circuit *net27*

No.	$\mathbf{m}_0$	M_I	M_O
1	5.1587	5.1587	19.828
2	3.9883×10^{-14}	3.9883×10^{-14}	4.4677
3	1.6681×10^{-14}	1.6681×10^{-14}	1.6517
4	–	–	0.3045
5	–	–	0.0348
6	–	–	2.4611×10^{-3}
7	–	–	1.6134×10^{-4}

In summary, we observe that for efficient terminal reduction, the input and output terminals cannot be bidirectional, which means B and L^T will be different and passivity will be difficult to be enforced using projection-based MOR methods. As a result, SVDMOR and the proposed ESVDMOR method will be more suitable for AC analysis where passivity is a less concerned problem as long as the reduced system is stable, which can easily enforced by the existing Krylov subspace methods.

5. Experimental results

The proposed method has been implemented in MATLAB 7.0. We tested our algorithm on a number of real industry interconnect circuits from our industry partner. For all the examples, we apply both SVDMOR[2] and ESVDMOR terminal reduction methods. The MOR operations are performed using PRIMA [6] for all the examples for both algorithms.

The first example, *net27*, has 14 inputs and 118 outputs with the model order of 182. Because there are more outputs than inputs, the number of the independent input terminals can be determined by using only DC moment as M_I. However, higher order moment information is needed to find the number of the independent output terminals. Here we use first nine order block moments to construct the output moment matrix M_O, which considers the worst case that all the output terminals are independent to each other.

The singular values for $\mathbf{m}_0$, which is used by SVDMOR, M_I, M_O are shown in Table 1. From the table we can see that we only need one input and one output terminal after terminal reduction by the SVDMOR method. By using M_I and M_O in the ESVDMOR method, we find that there are more than one dominant singular values of M_O. We choose one input and five outputs to make the reduced model more accurate.

To compare accuracy between the SVDMOR and ESVDMOR methods in a fair way, we make sure the reduced models for both algorithms have the same number of poles. If we use the same order of block moments, then more terminals will lead to more poles using the Krylov subspace MOR methods.

[2]We only use the DC moment for the SVDMOR implementation.

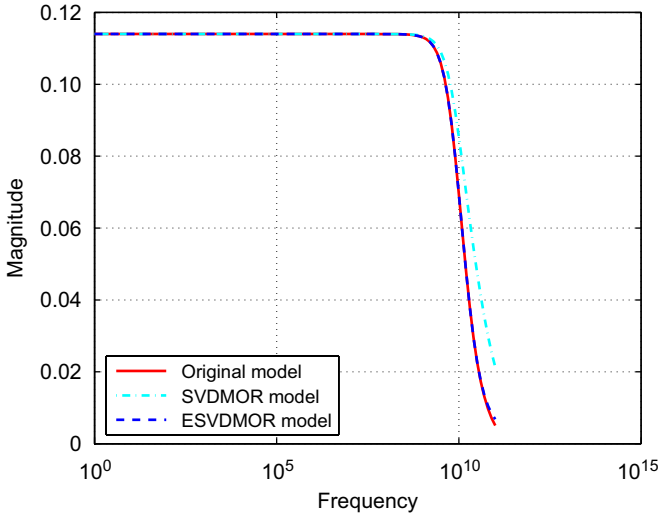

Fig. 3. Frequency responses from SVDMOR and ESVDMOR for *net27* circuit.

For circuit *net27*, six poles are used to approximate the original model for both SVDMOR and ESVDMOR methods. The results are shown in Fig. 3, which is the frequency responses corresponding to the 2nd input and the 10th output.

From these frequency response results, we can see that our ESVDMOR model could match the original model up to 5 GHz. In contrast, SVDMOR reduced model can only match frequency up to 500 MHz. This clearly shows the advantage of the ESVDMOR over SVDMOR method when the input and output terminals have different dependency (different ranks in their moment responses matrices).

One may argue that we are more accurate since we use more terminals. Actually if we use five inputs and five outputs in SVDMOR method, the results are still not good comparing to our ESVDMOR method under the six poles. The results are shown in Fig. 4, where SVDMOR model #2 refers to the SVDMOR results with five input and five output terminals. Hence simply increasing the number of terminals in SVDMOR does not help to improve the model accuracy.

The second example is circuit *net1026*, which has 6 inputs and 256 outputs with the model order of 522. Since the number of output terminals is also larger than the number of input terminals, we use $r = 43$ order moments to construct the output moment matrix M_O. After we obtain the singular values as shown in Table 2, the terminal reduced subsystem for SVDMOR becomes a single-input and single-output (SISO) system, and the terminal reduced subsystem for ESVDMOR is a one-input and five-output (SIMO) system. We still use the projection subspace based MOR with the same reduction order (five poles) for both methods.

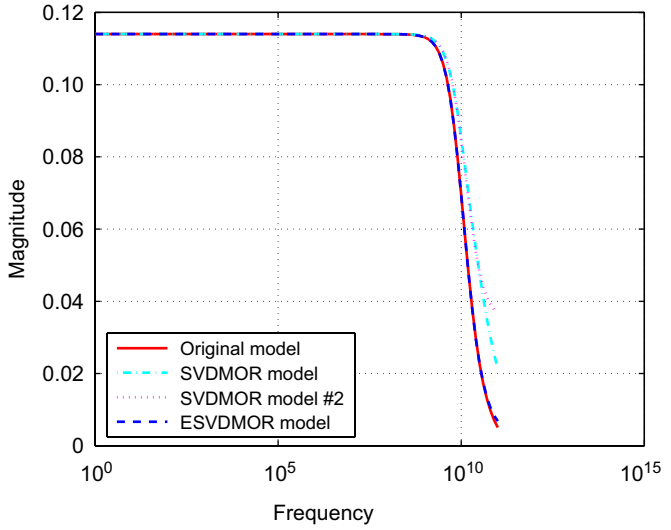

Fig. 4. Frequency response from SVDMOR and ESVDMOR with different terminals for *net27* circuit.

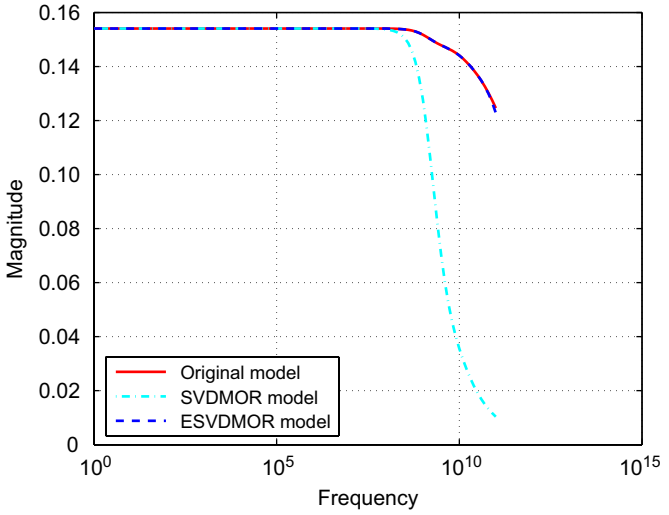

Fig. 5. Frequency responses from SVDMOR and ESVDMOR for *net1026* circuit.

Table 2
The singular values of DC moment, input moment matrix and output moment matrix of the circuit *net1026*

No.	$\mathbf{m}_0$	M_I	M_O
1	7.5175	7.5175	2097.6
2	2.7376×10^{-15}	2.7376×10^{-15}	10.501
3	7.5742×10^{-16}	7.5742×10^{-16}	1.6625
4	–	–	0.12577
5	–	–	0.00134
6	–	–	8.278×10^{-6}
7	–	–	3.9216×10^{-8}

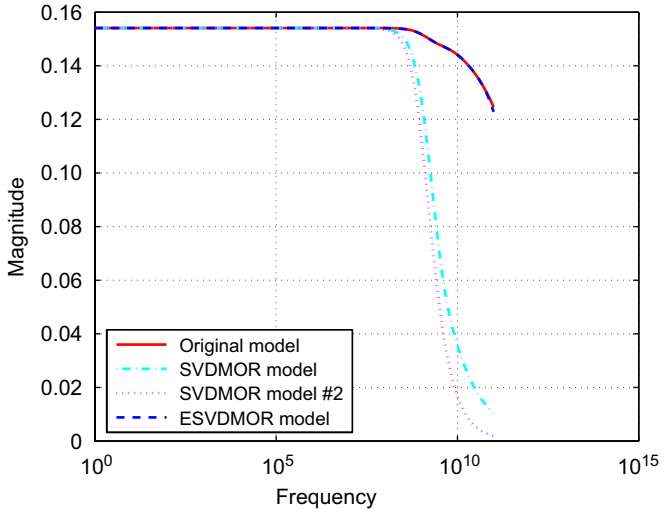

Fig. 6. Frequency responses from SVDMOR and ESVDMOR with different terminals for *net1026* circuit.

Although we use $r = 43$ order moments to find out the dominant singular values, we also observe that there are always five dominant singular values when we choose $r \geqslant 5$ for output moment matrix. That means we can find the number of the independent terminals by only using five moments information and higher order moments are not necessary. So the numerical problem resulting from direct moment computation is not a big issue any more for our algorithm.

We choose the response between the first input and the first output and show the frequency domain response results in Fig. 5. This example have the similar situations with the first example: it has larger number of output terminals than the input terminals. As a result, input and output terminals have different numbers of independent terminals. By just using one terminal for both input and output does not approximate well for the model order reduced system.

Again, if we use five inputs and five outputs for the SVDMOR model, the accuracy does not improve much as shown in Fig. 6 (SVDMOR model #2).

To compare the terminal reduction effects when all the terminals are treated as bidirectional for *net1026* circuits, we list the singular value results with decreasing order after the SVD on the 0th and 1th moment matrices in Table 3.

From Table 3, we can see that the singular values decay very slowly and the terminals cannot be reduced very much. Actually the rank of the moment matrix $\mathbf{m}_0$ (given by Matlab rank command) is 261, which is close to the full rank 262 ($= 256 + 6$) of the moment matrix. And the rank of the moment matrix $\mathbf{m}_1$ is the full rank. This happens for all the other test circuits we have and we think this is may be a general phenomena for RC circuits.

One obvious reason for this problem is that many output terminals now become input terminals. As a result, we require that the input impedance of a terminal will be equal to its transfer function to another terminal if the two terminal are same, which is unlikely and makes the reduction process more difficult.

Table 3
The singular values of the DC moment, 1th order moment matrices of the circuit *net1026* when all the terminals are treated as bidirectional ones

No.	$\mathbf{m}_0$	$\mathbf{m}_1$
1	0.58970	0.42268
2	0.55093	0.33515
3	0.50215	0.30440
4	0.41875	0.28897
5	0.31229	0.25942
6	0.064575	0.24131
⋮	⋮	⋮
258	0.0023181	0.0099492
259	0.0013246	0.0099117
260	0.00059548	0.0098789
261	0.0001499	0.0098567
262	2.9535×10^{-17}	0.0096795

Table 4
The singular value of DC moment, input moment matrix and output moment matrix of the circuit *net55*

No.	$\mathbf{m}_0$	M_I	M_O
1	4.224	4.224	4.224
2	2.4495	2.4495	2.4495
3	0.4126	0.4126	0.4126
4	5.5185×10^{-16}	3.1765×10^{-13}	5.5185×10^{-16}

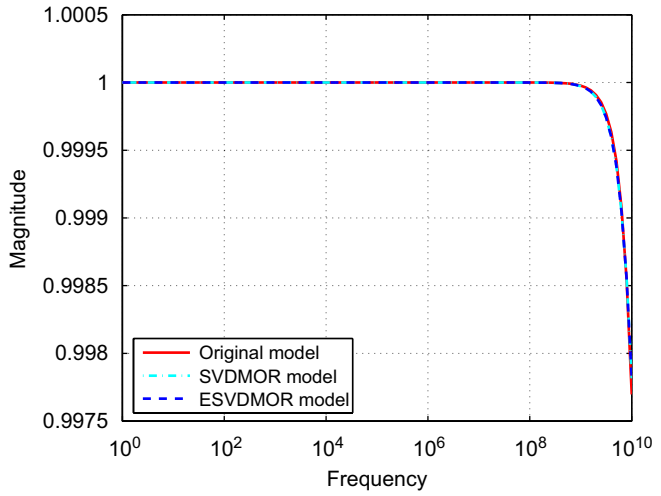

Fig. 7. Frequency responses from SVDMOR and ESVDMOR for *net55* circuit.

The third example is also a RC interconnect circuit, *net55*, which has 59 input terminals and 31 output terminals with model order of 187. Both the DC moment and the first moment are used to determine the number of independent inputs for the ESVDMOR method.

Table 4 gives the singular values for $\mathbf{m}_0$, M_I, M_O. We notice that both M_I and M_O have the same rank as $\mathbf{m}_0$. Moreover, the dominant singular values of M_I are the same as that of M_O although M_I uses two block moments instead of the only DC moment used in M_O. Actually for this example, the three dominant singular values are almost constants even if we use more high order moments to build the input matrix and the output matrix. That means this circuit system has both three independent inputs and three independent outputs. Therefore, SVDMOR has already achieved the best terminal reduction result by using only DC moment information. In this case ESVDMOR can obtain the same reduced models as SVDMOR which are shown in Fig. 7. The reduced order models have 12 poles.

Our testing circuits are RC circuits. For RLC circuits, we expect to use more moments (orders) as RLC circuits have much more complicate frequency responses (undershoot, overshoots, ringing, etc.) and terminal reduction effects will also be degraded as it is harder for two terminals to be similar for RLC circuits over the high frequency ranges.

6. Conclusions

In this paper, we have proposed a new combined terminal and model order reduction method, ESVDMOR, for compact modeling of interconnect circuits. The new method improves SVDMOR [1] by using higher order moment information for terminal responses during the terminal reduction and using separate SVD low-rank approximation on input and output terminals, respectively. The new method exploits the fact that input and output terminals may not have the same degree of correlations and it can better exploit the correlation of input and output terminals separately to achieve better approximation. We also discussed the passivity issues in terminal reduction and showed that simply treating all the terminals as bidirectional ones to enforce the passivity may not work well for the SVD-based terminal reductions under the projection-based MOR framework. Our experimental results have shown that ESVDMOR outperforms SVDMOR in terms of accuracy for the same reduced model size in a number of interconnect circuits when the input and output terminals are quite different.

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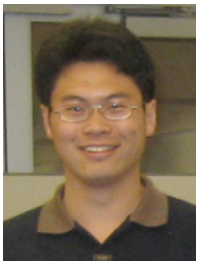

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