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INTEGRATION, the VLSI journal 41 (2008) 153–160
INTEGRATION the VLSI journal
www.elsevier.com/locate/vlsi

Large scale P/G grid transient simulation using hierarchical relaxed approach

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Received 28 August 2005; received in revised form 14 March 2007; accepted 4 April 2007

Abstract

This paper proposes a hierarchical relaxed approach to analyze large scale on-chip power/ground (P/G) grids with C4 packages efficiently. Different from the existing hierarchical approach where macro models and time-consuming matrix density reduction technique are used, this novel approach uses an iterative relaxation procedure to explicitly exploit the character of boundary nodes caused by C4 bumps, which can lead to more speedup without losing any accuracy. Also, an efficient partition strategy is generated to help the new algorithm to achieve higher performance on C4 based P/G grid. Experimental results demonstrate that the new algorithm is as accurate as the existing hierarchical method while it delivers more speedup over it for C4 based P/G grid.

Keywords: P/G networks; RLC circuits; Time-domain analysis; Relaxed hierarchical approach

1. Introduction

Nowadays, the design of both topology and performance of power/ground (P/G) grids is challenged by the growing current and power of complicated VLSI chips, especially different kinds of CPU chips. Usually, complicated high-performance microprocessors are often more susceptible to excessive IR drops, dI/dt noises, current coupling, electro-migration as well as resonance effects. So power integrity issues in microprocessor design need to be analyzed with especial care. On the other hand, more serious parasitic phenomenon due to rapid rising frequency and higher device density will cause the metal resources used by P/G grid growing rapidly. It is very common to use additional P/G resources to perform good shielding in order to reduce noises in real design. As a result, efficient and accurate transient analysis technique of P/G grid is required to capture the dynamic voltage fluctuations on the grid. Since billions of transistors can be integrated into one chip today, traditional circuit simulators, such as SPICE, are too time consuming to be applied in today's power verification process because a power grid always consists of billions of extracted resistors, inductors as well as capacitors (RLC), and the dynamic analysis has to be performed in a time step manner.

Driven by the increasing requirements on robust design of P/G network, many specific linear circuit simulation techniques have been proposed for fast P/G grid analysis in the past. Those methods include the hierarchical and macro-modeling-based method [1,2], preconditioned iterative-based approaches [3,4], transmission line modeling alternating direction implicit-based method [5], multi-grid methods [6–8], node reduction-based approaches [9,10], random walk-based approaches [11], and nonlinear programming techniques [12].

Among these methods, hierarchical analysis method is one of the most efficient strategies. This is because it can partition the original huge circuit into small macro blocks and solve each of them efficiently. However, one fatal shortage of hierarchical method presented in [1] is its expensive computation cost. It is not only because the decompositions of local matrices of internal circuits are costly, but also because the linear programming technique

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doi:10.1016/j.vlsi.2007.04.003

used in sparsification step is time consuming. Another problem of [1] is that the sparsification process has to be done in practical simulation to trade off between the memory usage and the computation time.

On the other hand, node reduction-based approaches [9,10] can be viewed as special hierarchical method. In these methods, lots of sub-circuits that contain only a few external ports can be reduced in an error-free manner naturally using special rules. However, the main drawback of this method is that it highly depends on the topology of the original circuits. Only when the original circuit contains special topologies, such as tree or chain structures, can this method be performed. So the acceleration ratio of these kinds of methods highly depends on the circuit topology.

In this paper, we analyze the boundary character of traditional P/G grid with C4 bumps, and propose another kind of hierarchical method which explicitly uses an iterative relaxation process on boundary nodes to eliminate the error introduced by *hard partition* which sets the boundary current to zero directly. This approach is inspired by the recent multi-grid methods [6,7] where a relaxation process is also used to smooth the error introduced by the simplified coarse grid. Comparing with [1,9,10], this method exploits the characteristic of P/G grid with C4 bumps sufficiently, it overcomes the shortages of traditional hierarchical analysis methods and can gain acceleration by using a relative simple geometry based relax process which will not introduce dense computation and obvious errors. Also, we have proposed an efficient scheme to partition P/G grids with C4 (Controlled Collapse Chip Connection) pads to exploit the *Locality Property* [13]. Experimental results show that this strategy is very efficient because only a few relaxation iterations are needed for usual P/G grid circuits to achieve good convergence.

This paper is organized as follows: Section 2 introduces the analysis of P/G grid boundary condition; Section 3 introduces our hierarchical P/G analysis approach and analyzes its performance; Section 4 presents the modeling and partition scheme for P/G grid with C4 pads; finally, experimental results are described in Section 5 while Section 6 concludes the whole paper.

2. P/G grid boundary condition analysis

One main contribution of [1] is that it introduces a good macro model to do the partition work. Each macro is described by a matrix transfer equation on the boundary node which can be used to do global computation. Also, both the transfer matrix and vector can be obtained by applying matrix decomposition to the internal matrices. However, it is a pure mathematical method to describe the boundary condition of P/G grid by transfer equation. Actually, some natural rules always hold for P/G grid. If we can make good use of these rules, computation process can be simplified.

First of all, let us take a multi-core microprocessor as an example, such as IBM Power 4 microprocessor, which contains two identical cores separated in left and right hand side of the chip. If the P/G grid provides power supply to two identical cores symmetrically, we can find that no boundary current will exist, as shown in Fig. 1.

This property can be proved easily in a contradiction manner by using the symmetry assumption and the identity assumption. Thus, in this case, if we partition the whole circuit into two parts, nothing else should be done to compensate for any error.

Secondly, let us consider the case that allows minor differences to exist in each of the units. From the circuit theory, we know that each black box circuit can be represented by its *Norton Equivalent Circuit* which consists of a current source and an equivalent resistance. For simplification, we can only consider the case that two blocks are connected by a resistor, as shown in Fig. 2.

In this case, if we cut the connection off, and compute the two blocks separately, we can get the voltage expression of boundary node A and boundary node B as formula (1):

$$V_a = \frac{I_a}{g_a}, \quad V_b = \frac{I_b}{g_b}. \tag{1}$$

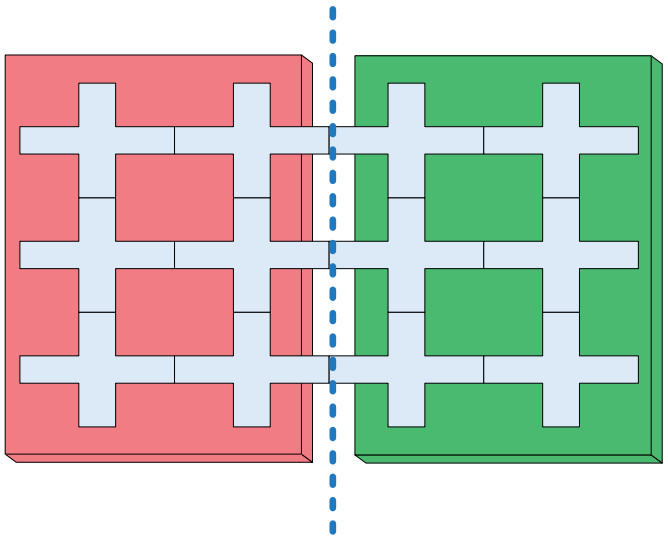

Fig. 1. Symmetrical and identical boundary.

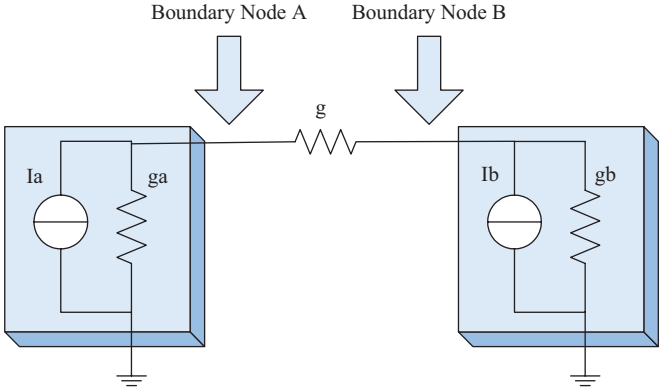

Fig. 2. Two different blocks connected by a resistor.

Table 1
Typical resistance data in a CPU benchmark

Layer	Process: tsmc 130 nm	
	Typical adjacent resistance (Ω)	Typical P/G grid resistance (mΩ)
M1	8.95	<10
M2	0.65	<10
M3	0.2	<10
M4	3	<10

Then, if the resistor connection is considered, we can get the actual voltage expression of node A and node B as formula (2):

$$V_a = \frac{I_a}{g_a}\frac{(1/g)+(1/g_b)}{(1/g)+(1/g_a)+(1/g_b)} + \frac{I_b}{g_b}\frac{1/g_a}{(1/g)+(1/g_a)+(1/g_b)}$$
$$V_b = \frac{I_b}{g_b}\frac{(1/g)+(1/g_a)}{(1/g)+(1/g_a)+(1/g_b)} + \frac{I_a}{g_a}\frac{(1/g_b)}{(1/g)+(1/g_a)+(1/g_b)} \quad (2)$$

From these two equations, we can see that, if $I_a = I_b$ and $g_a = g_b$, then we will have $V_a = V_b$, which means that there would not be any current flowing from the connection resistor. This is actually the symmetry and identity case we have discussed. Now, keep in mind that in P/G grid simulation, all the current sources in the black box are introduced by gates and pads while all the resistors in the black box are introduced by P/G grid metal which belongs to this box. Therefore, we will have $I_a \neq I_b$ if the partitioned blocks have different power density. However, from formula (2) we can know, if $g \ll \max\{g_a, g_b\}$, using (1) to replace (2) will cause little error. If we check the metal resistance between two adjacent gates along the P/G grid in Metal 1 to Metal 4, we can find that it is definitely magnitudes larger than the equivalent resistance of the partial power grid, as described in Table 1.

This data imply that if we partition the whole P/G grid into local blocks and just do simulation in local grid, the simulation error will not be as large as we expected. This results also are introduced in [13] as 'locality property' especially when C4 bumps are considered.

3. Hierarchical boundary relaxation

In this section, we introduce how to use a relaxation strategy to make the simulation process matching the boundary property of P/G grid perfectly.

For an extracted P/G network, which consists of elements of resistors, inductors and capacitors, the linear system equations can be formulated using modified nodal analysis (MNA) as follows [4]:

$$\begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix}\begin{bmatrix} \overline{V}(t) \\ \overline{I}(t) \end{bmatrix} + \begin{bmatrix} G & A_l^T \\ -A_l & 0 \end{bmatrix}\begin{bmatrix} V(t) \\ I(t) \end{bmatrix} = \begin{bmatrix} U(t) \\ 0 \end{bmatrix}, \quad (3)$$

in which C, L and G are sub-matrices for capacitors, inductors and conductors, respectively A_l is the sub-matrix which indicates the connectivity of independent inductors, $U(t)$ is the input vector standing for independent current sources [4]. By using numerical integration methods like Backward Euler, (3) can be transformed into a linear algebraic Equation (4):

$$Ax = b, \quad (4)$$

where A and b are defined in (5) and (6) and h is a fixed time step.

$$A = \begin{bmatrix} C/h + G & A_l^T \\ -A_l & L/h \end{bmatrix}, \quad (5)$$

$$b = \begin{bmatrix} U(t) + (C/h)V(t-h) \\ (L/h)I(t-h) \end{bmatrix}. \quad (6)$$

At a given time step, if we do not consider mutual inductance and mutual capacitance, then we can partition the original system at least into two sub-circuits, one is sub-circuit I and the other one is sub-circuit R, each of which corresponds to a node set naming set I and set R, respectively. Between part I and R, there are some boundary nodes belonging to both node sets connecting the two circuits together. By ordering the node sequence number, respectively, in each sub-circuit, the system equations can be reformulated to the following form:

$$\begin{bmatrix} A^{II} & A^{IB} & 0 \\ A^{BI} & A^{BB} & A^{BR} \\ 0 & A^{RB} & A^{RR} \end{bmatrix}\begin{bmatrix} x^I \\ x^B \\ x^R \end{bmatrix} = \begin{bmatrix} b^I \\ b^B \\ b^R \end{bmatrix}, \quad (7)$$

in which A^{II} is the matrix associated with nodes belonging to node set I, so as to the matrix A^{RR}. Matrix A^{IB} and A^{BI} are the connection matrices associated with nodes belonging to node set B and I.

The idea of our hierarchical analysis is like this: if it is possible to get a good estimation of x^B whose components are in boundary nodes set B, the original system equations can be divided into two sub-equations and be solved separately as shown in (8) and (9). If it is hard to get the estimation value of x^B, we also can use a zero vector according to the boundary property.

$$A^{II}x^I = b^I - A^{IB}x^B, \quad (8)$$

$$A^{RR}x^R = b^R - A^{RB}x^B. \quad (9)$$

Then, from Eq. (7) we can also obtain (10),

$$A^{BB}x^B = b^B - A^{BI}x^I - A^{BR}x^R, \quad (10)$$

which means that the initial estimation of x^B can be updated once the value of x^I and x^R are got. Therefore, given an initial estimation of vector x_0^B, instead of solving (7) directly, a vector sequence can be got via an iteration procedure, as shown in (11). Here, voltage vector of sub-circuits x_k^I and x_k^R can be obtained by applying either by a

direct method like LU or

$$\begin{cases} x_k^{\mathrm{I}} = A^{-\mathrm{II}}(b^{\mathrm{I}} - A^{\mathrm{IB}}x_k^{\mathrm{B}}), \\ x_k^{\mathrm{R}} = A^{-\mathrm{RR}}(b^{\mathrm{R}} - A^{\mathrm{RB}}x_k^{\mathrm{B}}), \\ x_{k+1}^{\mathrm{B}} = A^{-\mathrm{BB}}(b^{\mathrm{B}} - A^{\mathrm{BI}}x_k^{\mathrm{I}} - A^{\mathrm{BR}}x_k^{\mathrm{R}}), \end{cases} \tag{11}$$

an iterative method such as preconditioned conjugate gradient (PCG) [14] to (8) and (9). Similarly, we can get x_{k+1}^{B} by solving Eq. (10).

As we know, partition can gain benefit only when the original cost function is nonlinear. Otherwise if the original cost function is linear, no matter how many sub-blocks we can get, the total computation time will remain the same. Thus, the benefit of hierarchical relaxation is mainly based on two facts: (1) both the computation time and the fill in ratio of LU and Cholesky Decomposition processes will increase supper-linear with the matrix size and (2) the convergence speed of PCG method under the same kinds of precondition matrix will decrease dramatically as the matrix size increases, especially when the matrix has poor condition number [14]. So, using a partition strategy, no matter which kinds of methods we choose to solve the sub-circuits, if the relaxation process can converge fast, we can save a lot of computation time. Also, parallel computing technique can be used to accelerate the relaxation process naturally.

Now, the problem here is whether the relaxation process will converge fast? Generally, the simulation matrix A is a diagonal dominant matrix, also, the relaxation process is definitely a block Gauss–Seidel iteration process, so the convergence of this scheme is assured. Also, we find that when doing the P/G grid simulation under C4 package, if we partition the total P/G grid into small grids according to the C4 bumps, then solving local grid one by one, the error caused by neglecting boundary current is usually very small (described in Section 4). So, this is why the overall error can quickly come under control even if the Gauss–Seidel itself does not converge very fast for a general matrix case.

Our complete relaxed hierarchical simulation algorithm is shown in Fig. 3.

From this algorithm, we can see that for dynamic simulation, the whole process includes two kinds of iterations. First, it iterates on different time steps. Second, at a certain time step k, it begins internal iteration using the node voltage gained from time step $k-1$ as an initial prediction. Because the voltage of a node is a time domain continuous variable, the use of previous value as an initial prediction can still decrease the local simulation error dramatically although the boundary property holds.

For the initial vector, usually, an assumption that all the voltage value of nodes connected to power net are equal to Vdd, all the voltage value of nodes connected to ground net are equal to Vss and all the current sources are zero at time step zero, is usually given in transient simulation to satisfy initial condition of dynamic system named a stable initial condition, i.e., the SPICE does its work in this manner. Because of this assumption, we can generate a very good prediction vector at time step zero. Otherwise, if non stable initial condition is considered, prediction of the initial vector can be simply set to zero.

```
Algorithm Name:  Relax_Hier
Algorithm Input:   P/G grid circuit
                   total simulation time step
                   error bound e
Algorithm Output:  voltage vector at each time step
Relax_Hier(P)
{
    Partition the P/G grid if any symmetry and identical structure exists
    Partition the left P/G grid use some strategies
    For each time step k
    {
        p = 0
        If ( k = = 0 )
        {
            x^I_{k,p} = x^I_0    x^B_{k,p} = x^B_0    x^R_{k,p} = x^R_0
        }
        else
        {
            x^I_{k,p} = x^I_{k-1,p}    x^B_{k,p} = x^B_{k-1,p}    x^R_{k,p} = x^R_{k-1,p}
        }
        While ( norm(b-Ax)/norm(b) > e )
        {
            Solve (8) to get  x^I_{k,p+1}
            Solve (9) to get  x^R_{k,p+1}
            Solve (10) to get x^B_{k,p+1}
            p ++
        }
        x^I_{k,0} = x^I_{k,p-1}    x^B_{k,0} = x^B_{k,p-1}    x^R_{k,0} = x^R_{k,p-1}
    }
}
```

Fig. 3. Hierarchical relaxed iteration algorithm.

4. Efficient partition scheme for C4 pattern P/G grids

4.1. Model of C4 pattern P/G grid

For high performance VLSI chip, especially when flip chip package is used, the P/G grid is common to have several metal layers together with C4 pads. Fig. 4 shows a typical P/G grid layout, which consists of four metal layers: vertical Metal 1 (M1) and Metal 3 (M3); horizontal Metal 2 (M2) and Metal 4 (M4). The C4 pads are connected to M4 on the top layer and power is delivered to M1–M4 layers through vias. In each metal layer, the Vdd and Gnd rails run in parallel alternately while vias are placed at the crossings points of different rails running in adjacent layers [13]. The simulation model of P/G grid with C4 bumps can be modeled as a general mesh structured circuit consisting of RLC elements extracted from metal rails while gates can be modeled as independent current sources connecting to the lowest metal layer, as shown in Fig. 5.

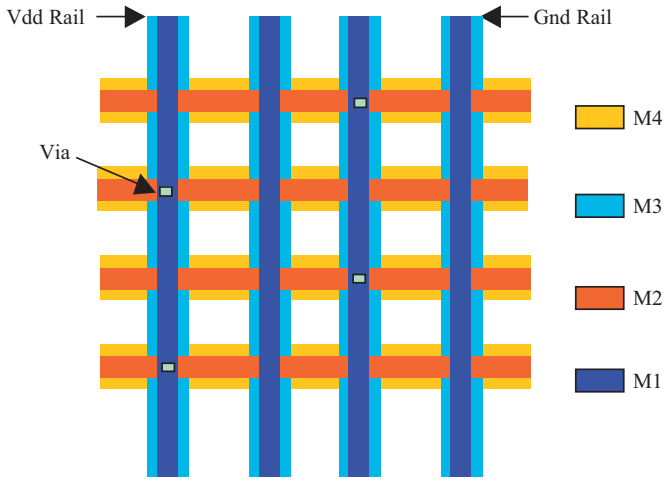

Fig. 4. Physical model of a multi-layer P/G distribution network.

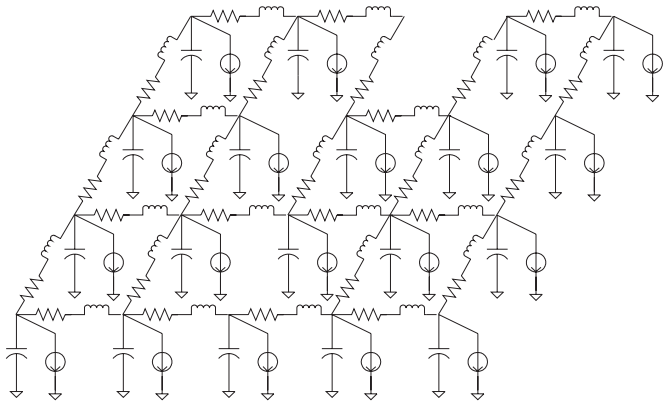

Fig. 5. Mesh structure RLC model for P/G grid.

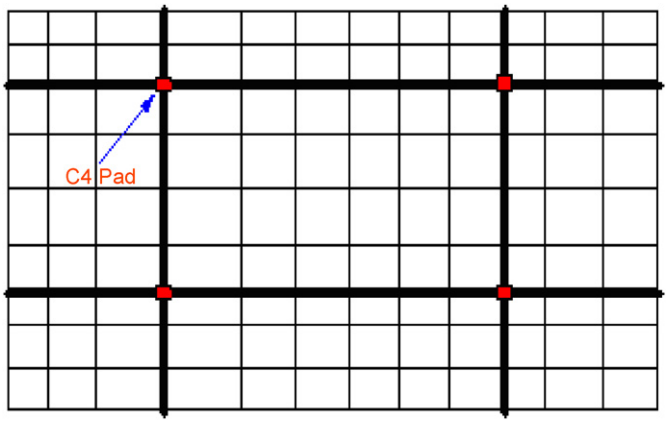

Fig. 6. Efficient partition scheme.

4.2. *Efficient partition scheme*

In this section, we introduce how to take advantage of P/G grid with C4 pads to perform our simulation efficiently. Our strategy is shown in Fig. 6. Firstly, on the top two layers M4 and M3, we can partition the grid according to C4 pads. Then for middle layers, M2 and M1, we can partition these middle layers to a number of smaller sub-blocks according to the vias.

Take Fig. 6 as an example, the red points in it stand for C4 bumps while wires in bold black stand for the block boundaries of first-level partition. Then the thin lines within each big block stand for block boundaries generated by second-level partition. The second-level partition process can be done recursively until the block granularity fits requirement. As in Fig. 6, the first-level partition process divides the whole area into 9 big blocks while the second-level partition process divides the center block into 24 sub-blocks.

Such geometry-based hierarchical partition is got according to the observation that the boundary nodes typically experience the smaller voltage fluctuation when power is distributed by C4 pads [13].

This means partition in this manner can minimize the boundary current and accelerate the convergence of inner iteration refinement process. Fig. 7 shows the typical voltage distributions of a center bumped P/G grid where the lowest voltage gradient can be found at the boundary nodes. This character is named *locality* in [13]. Recall that in our relaxation iteration procedure, if the boundary current approaches zero, then no more than one iteration step is needed in the inner iteration, so this is why together with this kind of partition strategy, our relaxation iteration method can accelerate usual direct or iteration based non-hierarchical simulation process a lot without losing any accuracy. Further, the partition granularity of the grid can be adjusted to adapt different via density in different metal layers to get the best result using least inner iteration times.

5. Experimental results

The proposed simulation algorithm has been implemented in C language and been tested on a SUN V880 workstation with 750 MHz Ultra Sparc CPU and 2 GB memory. PCG method using *incomplete Cholesky Decomposition* as its preconditioner is used to solve the sub-matrix. The number of time steps is assigned to 120 and each time step stands of 0.05 ns. Vdd here is set to 2.0 V.

First, we compare our new relaxed hierarchical method with SPICE3f40 and PCG method without hierarchical strategy in terms of accuracy. The three algorithms are used to solve a P/G network having about 2.5k nodes. The waveform of a randomly chosen node is shown in Fig. 8 where the horizontal axis stands for time in nano-second unit while the vertical axis stands for the node voltage fluctuation in standard unit. From Fig. 8, we can see that the three different algorithms share almost the same accuracy in time-domain dynamic analysis.

Then, we compare the accuracy and the simulation time of PCG method with and without the hierarchical strategy. Here each method is applied to solve a large P/G grid circuit containing about 1M nodes. We compare their

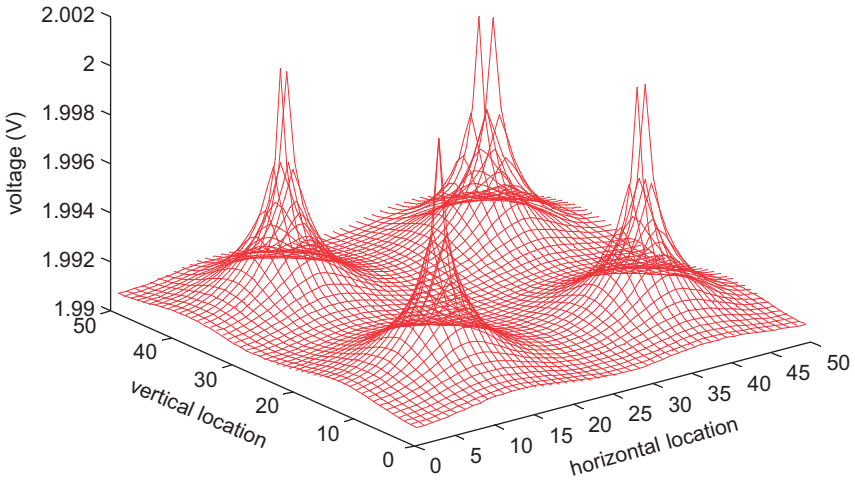

Fig. 7. The lowest voltage distribution in a circuit.

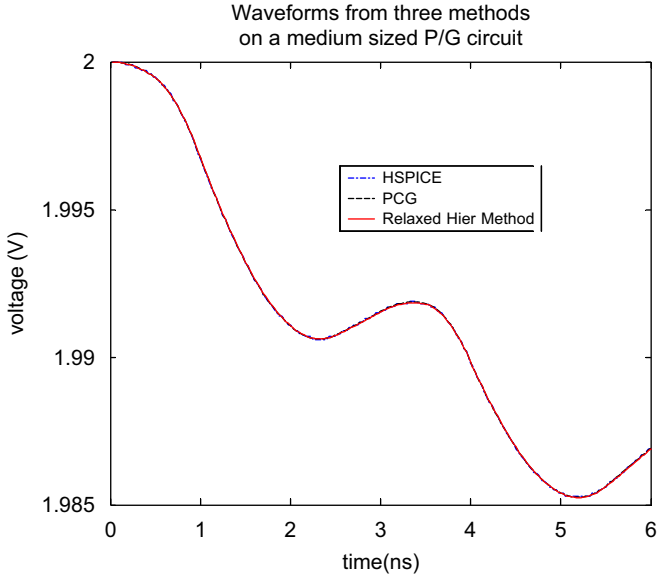

Fig. 8. Accuracy comparison for a 2500 node P/G net.

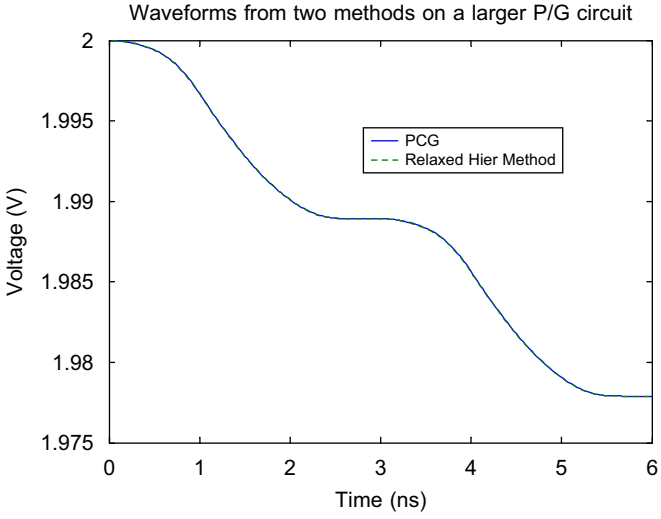

Fig. 9. Accuracy comparison for a large P/G net.

accuracy in Fig. 9. From it, we can still find that the same accuracy remains even as the problem size is scaling.

Table 2 compares the performance in terms of CPU time of the proposed hierarchical PCG, traditional PCG and SPICE3 on a number P/G grid benchmark circuits. The number of nodes and branches of these circuits are listed in columns 2 and 3. It can be seen that our new method can easily handle P/G grids dynamic simulation with 16 million nodes within 2.5 h. We also observe at least two orders of magnitudes speedup over SPICE3 for medium sized P/G circuits. More important, comparing with the traditional PCG we still have about 3× speedup. Compared with hierarchical approach in [1], where the computation time to solve a 20M circuits in 1000 times steps is about 43.5 h, our new method is about 2× in computation efficiency. Further, if parallel strategy is used, the speedup of our method will become obvious. Another important aspect of our method is that it will not slow down the serial computation efficiency while approach in [1] without parallel computing will cause performance degradation. So, consider all the aspects we discussed, we can say that the natural geometry based partition and low computation cost of our new hierarchical algorithm has more attractive characters over the existing hierarchical method.

Table 3 compares the maximal error caused by hierarchical and non-hierarchical PCG methods using the SPICE result as a standard. In the non-hierarchical PCG method, the iteration times is forced to be 20. In the hierarchical PCG method, the iteration times of sub-circuits is forced to be 10 while 10 times refinement is allowed to perform global relaxation. From Table 3, it is clear that the hierarchical PCG can gain more accuracy while using the same computation time. The data imply that the non-hierarchical PCG will cause more than 10% relative error while the hierarchical PCG only causes about 0.5% relative error under the given iteration times. This is obvious because for smaller circuits, the PCG method using the same kind of preconditioner will converge faster.

Table 2
Run time comparison results with PCG and SPICE3

Circuit name	# Node number	# Branch number	CPU time (s)			Speedup over (*X*)	
			Relaxed PCG	PCG	SPICE3	PCG	SPICE3
Ckt1	2.5k	4.7k	0.71	1.01	15.62	1.42	22.3
Ckt2	10k	19.4k	2.93	4.53	197.46	1.55	67.4
Ckt3	40k	78.8k	13.90	21.82	2797.76	1.57	201.3
Ckt4	250k	496k	122.65	271.25	N/A	2.21	N/A
Ckt5	1M	1.92M	491.62	1305.0	N/A	2.65	N/A
Ckt6	4M	7.66M	2002.46	5412.61	N/A	2.70	N/A
Ckt7	6.25M	12.3M	3151.94	N/A	N/A	N/A	N/A
Ckt8	16M	31.8M	8022.90	N/A	N/A	N/A	N/A

Table 3
Accuracy comparison on PCG with and without relaxation using the same iteration times

Circuit name	# Node number	Maximal absolute error (V)		Maximal relative error (%)	
		No relaxation	Relaxation	No relaxation	Relaxation
Ckt1	2.5k	0.12965	0.0031	6.4825	0.155
Ckt2	10k	0.19904	0.0038	9.9520	0.19
Ckt3	40k	0.21503	0.0047	10.7515	0.235
Ckt4	250k	0.21516	0.0043	10.7580	0.215
Ckt5	1M	0.10790	0.0056	5.3951	0.28
Ckt6	4M	0.18266	0.0044	9.1330	0.22

Relative error = 100% × absolute error/Vdd, Vdd = 2.0 V.

Table 4
Run time comparison between [1] and new method

Grid sized	Macro size	NNZ entries		Solve time (s)	
		HM	NEW	LU time in HM	Relaxed PCG time in NEW
1 M	5k	203k	15k	0.43	0.11
1 M	10k	812k	30k	12	1.4
1 M	20k	2M	60k	31	4.3

Also, we have compared our new strategy with the hierarchical method proposed in [1]. Table 4 gives the run time comparison between these two methods. Here, HM in the table stands for the hierarchical method without sparsifcation process in [1] while NEW stands for our relaxed PCG method. In this experiment, we use three different test P/G grids each of which contains 1 million nodes. From the table we can see that, different formulation results different simulation matrices containing different number of non-zero entries. In HM method, it tends to generate matrices with more non-zero elements, while in our new method, the simulation matrices are sparser due to the nature topology of P/G grid. Further, this situation will become worse as the size of macro increases. Therefore, due to the differences in matrix density, we can see it clearly in the table, that when a good partition strategy is used to isolate the strong coupled P/G grid, the convergence speed of the relaxed PCG method is fast. Compared with the HM method, we can obtain about 10 × speedup.

6. Conclusion and future work

In this paper, we have proposed a novel hierarchical simulation algorithm for efficient analysis of large scale P/G grids with C4 package. The new algorithm explicitly compensates the error introduced by partitioning and solving sub-circuits individually using a relaxation iteration process. Due to the 'locality property' held by C4-based P/G grid, such kind of relaxed hierarchical approach can allow more aggressive complexity reduction and thus lead to more speedup without significant loss of accuracy. We also have proposed an efficient scheme for partitioning P/G grids with C4 pads in an optimal manner. Experimental results show that the new algorithm is more accurate than the existing hierarchical method under C4 based P/G grids while it delivers more speedup over the traditional simulators.

In the future, the parallel computing techniques can be applied in this algorithm to further improve the efficiency of this hierarchical relaxed analysis approach.

Acknowledgements

Supported by "the National Natural Science Foundation of China (NSFC) 60476014"and "Hi-Tech Research & Development (863) Program of China 2005AA1Z1230".

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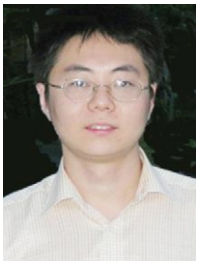

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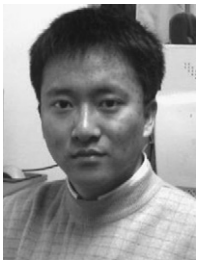

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