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Statistical modeling and analysis of chip-level leakage power by spectral stochastic method ☆

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In this paper, we present a novel statistical full-chip leakage power analysis method. The new method can provide a general framework to derive the full-chip leakage current or power in a closed form in terms of the variational parameters, such as the channel length, the gate oxide thickness, etc. It can accommodate various spatial correlations. The new method employs the orthogonal polynomials to represent the variational gate-level leakages in a closed form first, which is generated by a fast multi-dimensional Gaussian quadrature method. The total leakage currents then are computed by simply summing up the resulting orthogonal polynomials (their coefficients). Unlike many existing approaches, no grid-based partitioning and approximation are required. Instead, the spatial correlations are naturally handled by orthogonal decompositions. The proposed method is very efficient and it becomes linear in the presence of strong spatial correlations. Experimental results show that the proposed method is about 16× faster than the recently proposed method (Chang and Sapatnekar, 2005 [1]) with constant better accuracy.

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1. Introduction

Process-induced variability has huge impact on the circuit performance in the sub-90 nm VLSI technologies [3]. This is the particular case for leakage power, which has increased dramatically with the technology scaling and is becoming the dominant chip power dissipation [4]. The dominant factors in the leakage currents are the subthreshold leakage current I_{sub} and gate oxide leakage current I_{gate}. The subthreshold leakage current has a rapid increasing rate (about 5X–10X increase per technology generation [5]), and it is highly sensitive to threshold voltage V_{th} variations, owning to the exponential relationship between subthreshold current I_{sub} and threshold voltage V_{th}. On the other hand, as the gate oxide thickness, T_{ox}, is scaling down, I_{gate} is growing rapidly as I_{gate} has an exponential dependence on T_{ox}.

As a result, leakage variations become significant, and traditional worst case based approach will lead to extremely pessimistic and expensive design solutions. Statistical estimation and analysis of leakage powers considering the process variability are critical in various chip design steps to improve the design yield and robustness.

Many existing works have been proposed to statistically model and analyze the full-chip leakage currents and powers considering the process variations in the past [1]. Early work in [6] gives the analytic expressions of mean value and variance of leakage currents of CMOS gates considering only subthreshold leakage. Method in [7] provides simple analytic expressions of leakage currents of the whole chip considering global variations only. Method in [8] uses third order Hermite polynomial without considering spatial correlations, and only calculates the mean value of full-chip leakage current.

In [9], reverse biased source/drain junction band-to-band tunneling (BTBT) leakage current is considered, in addition to the subthreshold leakage currents, for estimating the mean values and variances of the leakage currents of gates only. In [10], the probability density function (PDF) of stacked CMOS gates and whole chip are derived considering both inter-die and intra-die variations. In [11], a hardware-based statistical model of dynamic switching power and static leakage power was presented, which was extracted from experiments in pre-determined process window.

Recently a full-chip leakage analysis method considering spatial correlations in the intra-die and inter-die variations was proposed [1]. But it requires $O(n^2)$ time complexity to compute the variance, where n is the number of gates in the design, which can be expensive for the large circuits. The method then introduced

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the grid-based partitioning of the circuits to reduce the number of variables at the loss of accuracy [1]. Reduction based approach has been proposed in [12] to speed up the leakage analysis, where Krylov subspace based reduction has been performed on the coefficient matrices of second order expressions. This method starts with independent random variables pre-extracted by principal components analysis (PCA). The number of resulting independent variables is assumed to be large (10^3-10^6). But converting the correlated random variables into uncorrelated ones via PCA can be expensive (at least non-linear) for large number of random variables, which will diminish the efficiency of the proposed method. Work in [13] proposed a linear time complexity method to compute the mean and variance of full-chip leakage currents by exploiting the symmetric property of one existing exponential spatial correlation formula. The method only considers subthreshold leakage and it requires the chip cells/modules to be partitioned into a regular grid with similar uniform fitting functions, which typically is not practical.

Recently, Bhardwaj et al. [14] presented a unified approach for statistical timing and leakage current analysis using quadratic polynomials. However this method only considers the long-channel effects and ignores the short-channel effects (ignoring channel length variables) for the gate leakage models. The coefficients of the orthogonal polynomials at gate-level are computed directly by the inter-production via the efficient Smolyak quadrature method. The method also tries to reduce the number of variables via the moment matching method, which further speeds up the quadrature process at the cost of more added errors.

In the paper, we propose a new general full-chip leakage modeling and analysis method. The new method starts with the process variational parameters such as the channel length, δL, gate oxide thickness, δT_{ox}, and it can derive the full-chip leakage current I_{leak} in terms of those variables directly (or their corresponding transformed variables). Unlike existing grid-based methods, which trade the accuracy for speedups, the new method is gate-based method and uses principal component analysis (PCA) to reduce the number of variables with much less accuracy loss assuming that the geometrical variables are Gaussian. For non-Gaussian variables, independent component analysis (ICA) [15] can be used. The new method considers both inter-die and intra-die variations and it can work with various spatial correlations. The proposed method becomes linear under strong spatial correlations. Unlike the existing approaches [1,13], the new method does not make any assumptions about the distributions of final total leakage currents for both gates and chips and does not require any grid-based partitioning of the chip. Compared with [14], the proposed method applies a more efficient multi-dimensional numerical quadrature method (versus on reduced number of variables using inter-production via the moment matching), considers more accurate leakage models and presents more comprehensive comparisons with other methods.

In the new method, we first fit both the subthreshold and gate oxide leakage currents into analytic expressions in terms of parameter variables. We show that by using more terms in the gate level analytic models, we can achieve better accuracy than [1]. Second, the new method employs the orthogonal polynomials, which gives the best representation for specific distributions [16] and is also called the *spectral stochastic* method, to represent the variational gate leakages in an analytic form in terms of the random variables. The step is achieved by using the numerical Gaussian quadrature method, which is much faster than the Monte Carlo method. The total leakage currents are finally computed by simply summing up the resulting analytical orthogonal polynomials of all gates (their coefficients). The spatial correlations are taken care of by PCA or ICA, and at the same time, the number of random variables can also been substantially reduced in the presence of strong spatial correlations during the decomposition process. Experimental results on the PDWorkshop91 benchmarks on a 45 nm technology show that the proposed method is about 10× faster than the recently proposed method [1] with constant better accuracy.

The rest of this paper is organized as follows: Section 2 presents the process variational models used in this work. Then in Section 3 we present the static analytic models for gates used in our work for computing the full-chip leakage currents. Section 4 reviews the orthogonal polynomial chaos based stochastic simulation methods and Section 5 presents our new full-chip statistical leakage analysis method. Section 6 presents the experimental results and Section 7 concludes this paper.

2. Process variational models

In this section, we present the process variations for computing variational leakage currents. Process variations include variations at different levels: wafer level, inter-die level, and intra-die level. They are caused by different sources such as lithograph, materials, aging, etc. Some of the variations are systematic, e.g., those caused by lithography process [17,18]. Some are purely random, e.g., the doping density of impurities and edge roughness [19].

The main process parameter that has big impact on leakage current is the transistor threshold voltage V_{th}, and V_{th} is observed to be the most sensitive to effective gate length L and gate oxide thickness T_{ox}. The ITRS-08 [20] indicates that the gate length variation is a primary factor for device parameter variation, and the number of dopants in channel results in unacceptably large statistical variation of the threshold voltage.

Our circuit model is built by using the predictive technology model (PTM) 45 nm technology [21], and simulated in HSPICE with supply voltage of 1 V. We compose each category of variations into "inter-die" and "intra-die" variations. And for intra-die variation, we further decompose it into with and without spatial correlation. These variations are modeled in normal distributions [22,23]. The total variance (σ^2) is computed by summing up variance of each component because the sum of normal distributions is still a normal distribution, and their variances are thus additive. We list the detailed parameters for gate length and gate oxide thickness variations in Table 2.

Electrical measurements of a full wafer show that the intra-die gate length variation has strong spatial correlations [17]. This implies that devices that are physically close to each other are more likely to be similar than those that are far apart. Therefore, in our model, the intra-die variation of gate length is modeled based on such kind of correlation. We use the empirical formulation such as the exponential model [24]:

$$\gamma(r) = e^{-r^2/\eta^2}, \tag{1}$$

where r is the distance between two panel centers and η is the correlation length. We notice that the strong spatial correlation suggested by (1) has been exploited by [1] to speed up the calculation, where the full chip is divided into N grids and the correlated random variables are perfectly correlated in a grid. In our approach, the strong spatial correlation is explored naturally by PCA, which can transfer the correlated R.V.s into independent ones with reduced numbers. But for comparison purpose, we also implemented the grid-based variational model. We remark that for non-Gaussian distributions, we can use independent component analysis (ICP) to perform the reduction [15]. On the other hand, the gate oxide thickness T_{ox} is in vertical layout feature dimension, and caused by chemical mechanical polishing (CMP)

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process. As a result, it depends on local layout density, and has no spatial correlation [25].

According to statistical theory, in normal distribution, 99% of the samples should fall in the range of $\pm 3\sigma$. According to [20], the physical gate length for high performance logic in 45 nm technology will be 18 nm, and the physical variation should be controlled within $\pm 12\%$. Therefore, we let 3σ be 12%. While it is similar for T_{ox}.

For a gate/module in a chip with equivalent length (ΔL), using our model parameters in Table 2, we have

$$\Delta L = \Delta L_{inter} + \Delta L_{intra_corr}, \tag{2}$$

ΔL_{inter} is constant for all cells in all grids because it is a global factor that applies to the whole chip. For one chip sample, we only need to generate it once. ΔL_{intra_corr} is different for each gate (our method) or each grid (method in [1]), and has spatial correlations. Therefore, we generate one value for each gate (our method)/grid (method in [1]), and the spatial correlation is modeled such that the correlation coefficient value diminishes equally with the distance between any two gates/grids.

3. Static leakage modeling for gates

Full-chip leakage current has two components, subthreshold leakage current and gate leakage current. Here we describe the empirical models for both of them, based on the assumption that the leakage current under process variations is estimated under lognormal distributions.

The subthreshold leakage current, I_{sub}, is exponentially dependent on the threshold voltage, V_{th}. And V_{th} is observed to be most sensitive to gate oxide thickness T_{ox} and effective gate channel length L due to short-channel effects. When the change in L or T_{ox} is small, the precise relationship shows an exponential dependent effect on I_{sub}, with the effect of T_{ox} relatively weak. For the gate oxide leakage current, both channel length and oxide thickness have strong impacts on the leakage currents, which are exponential functions of the two variables.

In our work, we also follow the analytical expressions given in [1], which estimate the subthreshold leakage currents and the gate oxide leakage currents as follows:

$$I_{sub} = e^{a_1 + a_2 L + a_3 L^2 + a_4 T_{ox}^{-1} + a_5 T_{ox}}, \tag{3}$$

$$I_{gate} = e^{a_1 + a_2 L + a_3 L^2 + a_4 T_{ox} + a_5 T_{ox}^2}, \tag{4}$$

where a_1 to a_5 are the fitting parameters for each unique input combination of a gate. Then we can use a look-up table (LUT) to store the fitting parameters. For a k-input gate, the size of the LUT is $2^k \times 10$ as we have two equations for each input combination, and each equation has 10 fitting parameters. While in [1], they only keep dominant states for leakage current, i.e., only one "off" transistor in a series transistor stack. However, with technology downscaling to 45 nm, this is not the practical case. The I_{sub} based on the model in (3) still has large error compared to the simulation results. Take the AND2 gate in Fig. 1 as an example. For subthreshold leakage current, there are four different input patterns, as shown in Fig. 2. In [1], they mentioned the "Dominant States", and assumed that only the leakage for dominant input patterns need to be considered. However, the AND2 gate is composed of two sub-circuits, one NAND gate and one inverter, and they have different dominant input patterns. Actually, there is no significant difference between the four kinds of input patterns. Also, when inputs are "01" or "10", the leakage sources are NMOS gates. But when input is "11", the main contribution comes from the PMOS gates (as shown in Fig. 2). So here, we need to measure the leakage currents for all input patterns. We choose 100 points for L and T_{ox} in their 3σ region linearly. After that by SPICE simulation at each point, the subthreshold leakage currents and gate leakage currents are stored as the original curve. Then we can do the curve fitting process. Figs. 3 and 4 show the curve fitting results of I_{sub} and I_{gate} for four input patterns in AND2 gate. From these two figures we can see that the curves we get fit the SPICE result very well, and the currents in the four cases are comparable with each other. So there is no "Dominant State", we need to consider all of them. Table 1 shows that the errors compared with industry SPICE simulation results for the AND2 gate for I_{sub}. *Max Err.* is the maximum error given by one input combination and *Avg Err.* refers to the average error over all the input patterns. If we add more terms into (3) as shown in Table 1, we can reduce

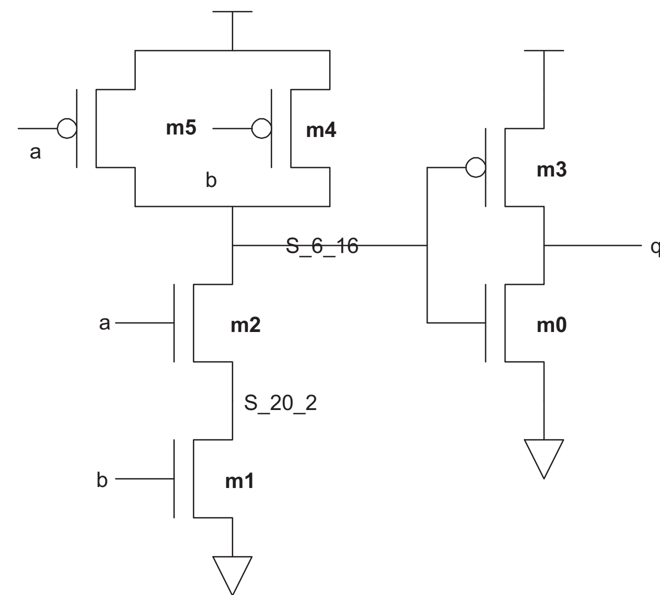

Fig. 1. Schematic of the AND2 gate.

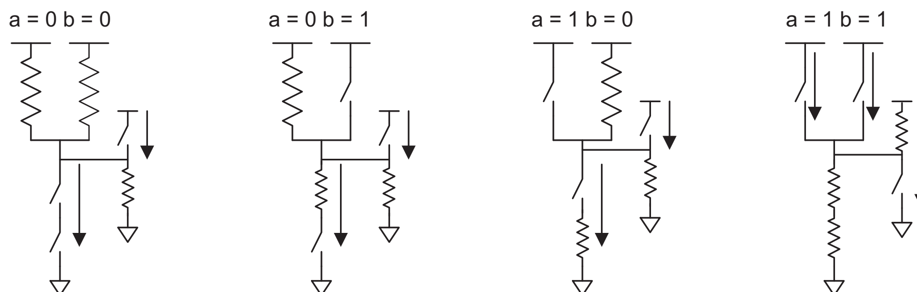

Fig. 2. Four leakage cases ($ab = 00$—pattern 0, $ab = 01$—pattern 1, $ab = 10$—pattern 2, $ab = 11$—pattern 3).

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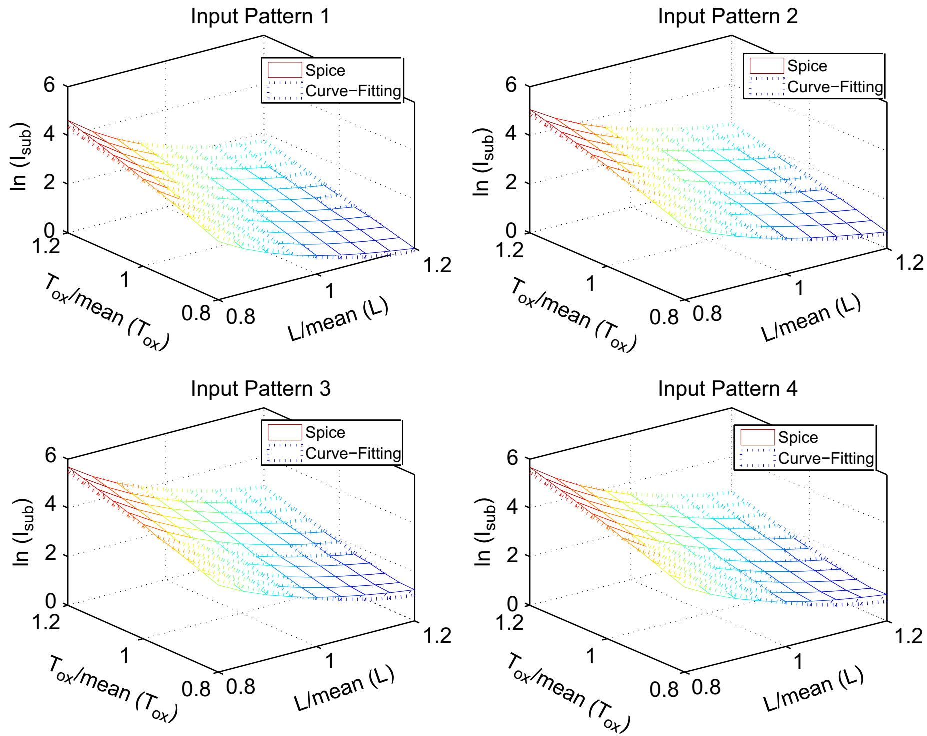

Fig. 3. Subthreshold leakage currents for four different input patterns in AND2 gate.

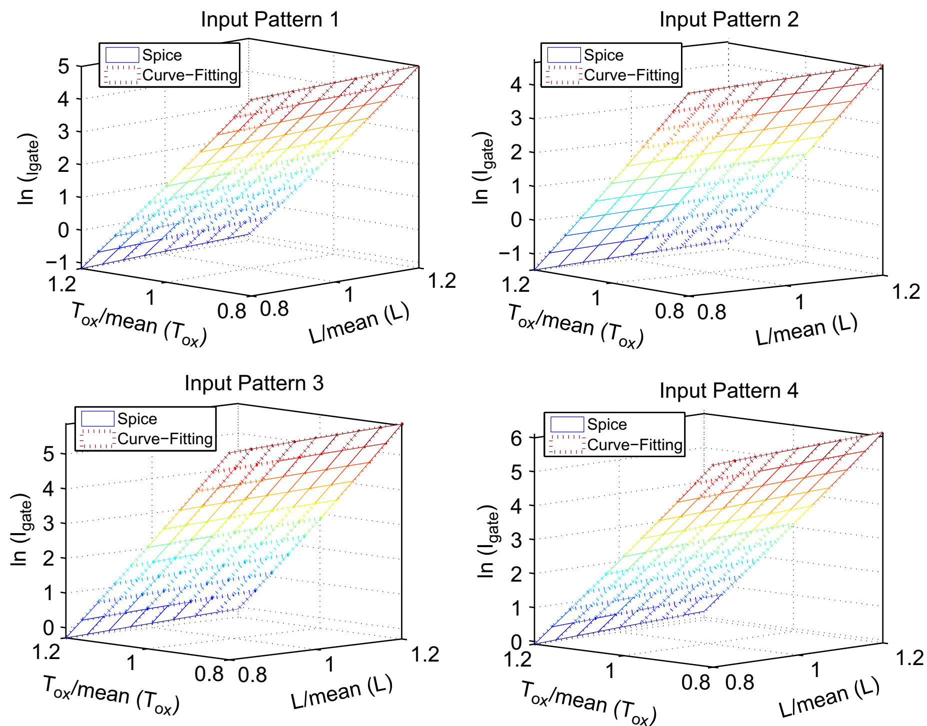

Fig. 4. Gate leakage currents for four different input patterns in AND2 gate.

the errors from 8% to about 3%. After we obtain the analytic expression for each input combination, we take the average of the leakage currents of all the input combinations to arrive final analytic expression for each gate in lieu of the dominant states used in [1].

4. Review of the orthogonal polynomial method

In the following, we briefly review the orthogonal polynomial based modeling approaches. Note that for the Gaussian and log-normal distributions, Hermite polynomial is the best choice as it

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Table 1
Relative errors by using different fitting formulas for leakage currents of AND2 gate.

Fitting components	Max. err. (%)	Avg. err. (%)
Original: $L, L^2, T_{ox}^{-1}, T_{ox}$	14.7	8.46
Add T_{ox}^2	13.95	8.26
Add $T_{ox}^2, T_{ox}/L$	7.08	5.95
Add T_{ox}^2, $T_{ox}/L, L/T_{ox}$	7.14	4.94
Add $T_{ox}^2, T_{ox}/L$, $L/T_{ox}, T_{ox} * L$	3.67	3.49

leads to exponential convergence rate [16]. For non-Gaussian and non-log-normal distributions, there are other orthogonal polynomials such as Legendre for uniform distribution, Charlier for Poisson distribution and Kraw-tchouk for binomial distribution, etc. [26,27]. The proposed method can be extended to other distributions with different orthogonal polynomials [28].

Hermite polynomial chaos (PC) utilizes a series of orthogonal polynomials (with respect to the Gaussian distribution) to facilitate stochastic modeling [28]. These polynomials are used as the orthogonal basis to decompose a random process in the similar way as sine and cosine functions are used to decompose a periodic signal in Fourier series expansion.

The polynomial chaos expansion is guaranteed to converge for any Gaussian random process with finite second-order moments [16]. Moreover, the Askey principle [29] shows that the expansion based on Hermite polynomials has the optimal convergence rate for a Gaussian random process. Also, the advantage of homogeneous polynomial chaos expansion over the traditional Taylor expansion is clearly demonstrated in recent related works [30,27].

For a random variable $v(t,\xi)$ with limited variance, where $\xi = [\xi_1, \xi_2, \ldots, \xi_n]$ is a vector of independent orthonormal Gaussian random variables with zero mean values. The random variable can be approximated by truncated Hermite PC expansion as follows [16]:

$$x(\xi) = \sum_{k=0}^{P} a_k H_k^n(\xi), \tag{5}$$

where $H_k^n(\xi)$ is n th order Hermite polynomial and a_k is the deterministic coefficient. The number of terms P is given by

$$P = \sum_{k=0}^{n} \frac{(n-1+k)!}{k!(n-1)!}. \tag{6}$$

When one random variable is considered, one-dimensional Hermite polynomials are expressed as follows:

$$H_0^1(\xi) = 1, \quad H_1^1(\xi) = \xi, \quad H_2^1(\xi) = \xi^2 - 1, \quad H_3^1(\xi) = \xi^3 - 3\xi, \ldots. \tag{7}$$

Hermite polynomials are orthogonal with respect to Gaussian weighted expectation (the superscript n is dropped for simple notation)

$$\langle H_i(\xi), H_j(\xi) \rangle = \langle H_i^2(\xi) \rangle \delta_{ij}, \tag{8}$$

where δ_{ij} is the Kronecker delta and $\langle *, * \rangle$ denotes an inner product defined as follows:

$$\langle f(\xi), g(\xi) \rangle = \frac{1}{\sqrt{(2\pi)^n}} \int f(\xi) g(\xi) e^{-(1/2)\xi^T \xi} \, d\xi. \tag{9}$$

Like Fourier series, the coefficient a_k can be found by a projection operation onto the Hermite PC basis:

$$a_k(t) = \frac{\langle x(\xi), H_k(\xi) \rangle}{\langle H_k^2(\xi) \rangle}, \quad \forall k \in \{0, \ldots, P\}. \tag{10}$$

In our problem, $x(\xi)$ will be the leakage current for each gate and for the full chip eventually.

5. The proposed method

To analyze the statistical model of chip-level leakage current, traditional methods are grid-based. Since the number of gates on a whole chip is very large, and every gate has its own variational parameters, which means that the number of random variables is huge. So considering efficiency, the traditional methods partition a chip to several grids, and assume that all the gates in one grid have the same parameters. However, this is not the real case. Take Fig. 5 as one example. Here the distance between Gate1 and Gate2 is smaller than the distance between Gate1 and Gate3. In grid-based method, we suppose that Gate1 has strong correlation with Gate3, and has weak correlation with Gate2. But actually, the situation is opposite. In this section, we will present the new full-chip statistical leakage analysis method. This method is gate-based instead of grid-based, while it can gain better speed as well as better accuracy than the method in [1], which is based on grid. Our algorithm is shown in Fig. 6. The new algorithm basically consists of three major parts. The first part (step 1) is pre-characterization, which builds the analytic leakage expressions (3) and (4) for each type of gates. This step only need to be done once

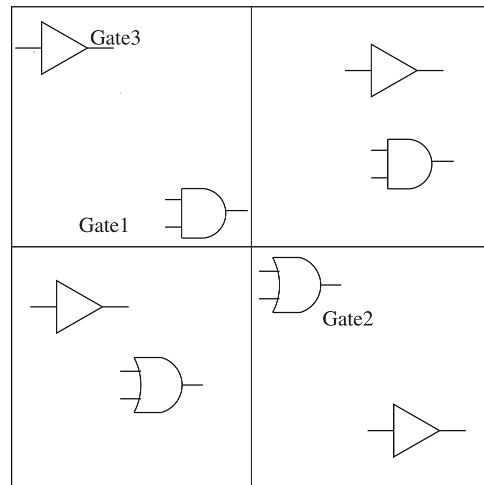

Fig. 5. An example of a grid-based partition.

Algorithms: NEW FULL-CHIP LEAKAGE CURRENT COMPUTATION ALGORITHM

Input: standard cell lib, netlist, placement information of design, σ of L and T_{ox}

Output: analytic expression of the full-chip leakage currents in terms of Hermite polynomials.

(1) Generate fitting parameter matrices a_{sub} and a_{gate} of I_{sub} and I_{gate} in (3) and (4) for each type of gates (after SPICE run on each input pattern) (Section 3).
(2) Perform PCA to transform and reduce the original parameter variables in $\mathbf{L}$ into independent random variables in $\mathbf{L_k}$. (Section 5.3).
(3) Generate Smolyak quadrature points set Θ_n^2 with corresponding weights.
(4) Calculate the coefficients of Hermite polynomial of $I_{sub,k}$ and $I_{gate,k}$ for the final leakage analytic expression for each gate using (21) and (22).
(5) Calculate the analytic expression of the full-chip leakage current by simple polynomial additions and calculate $\mu_{leakage}$, $\sigma_{leakage}$, PDF and CDF of the leakage current if required.

Fig. 6. The flow of proposed algorithm.

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for a standard cell library. The second part (steps 2–5) generates a set of independent random variables and builds the gate-level analytic leakage current expressions and covariances. The final part (step 6) computes the final leakage expressions by simple polynomial additions and calculates other statistical information.

5.1. Gaussian quadrature technique

The Gaussian quadrature method is an efficient numerical method to compute the definite integral of a function [31]. We apply it to compute the coefficients $a_k(t)$ in (10). We will review the method based on the Hermite polynomial below.

Our goal is to compute the integral equation $\langle x(\xi), H_j(\xi)\rangle$ numerically. In this case, this problem boils down to the one-dimensional numerical quadrature problem based on the Hermite polynomials [32]. Specifically, for Hermite polynomials, we have

$$\langle x(\xi), H_k(\xi)\rangle = \frac{1}{\sqrt{(2\pi)}}\int x(\xi)H_k(\xi)\, e^{-1/2\xi^2}\, d\xi \approx \sum_{i=0}^{P} x(\xi_i)H_i(\xi_i)w_i. \tag{11}$$

Here, $\xi = \{\xi\}$ contains only one random variable. ξ_i and w_i are Gaussian-Hermite quadrature abscissas (quadrature points) and weights, respectively.

The quadrature rule basically says that if we select the roots of P th Hermite polynomial as the quadrature points, the quadrature is exact for all polynomials of degree $2P-1$ or less for (11). This is called $(P-1)$-level accuracy of Gaussian-Hermite quadrature here.

For multiple random variables, which require multi-dimensional quadrature, traditional way to compute the multi-dimensional quadrature is to use a direct tensor product based on one-dimensional Gaussian-Hermite quadrature abscissas and weights [33]. With this method, the number of quadrature points needed for n dimension (variables) and P-level is about $(P+1)^n$, which is well known as the curse-of-dimensionality.

5.2. Smolyak quadrature for multi-dimensional integration

Smolyak quadrature [33] is used as an efficient method to reduce the number of quadrature points (also called sparse grid quadrature). Let us define one-dimensional Smolyak quadrature point set $\Theta_1^P = \{\gamma_1, \gamma_2, \ldots, \gamma_P\}$, which uses $P+1$ points to achieve degree $2P+1$ of exactness. The level-P Smolyak quadrature for n-dimensional integration chooses points from the following set:

$$\Theta_n^P = \bigcup_{P+1 \le |\vec{i}| \le P+n} (\Theta_1^{i_1} \times \cdots \times \Theta_1^{i_n}), \tag{12}$$

where $|\vec{i}| = \sum_{j=1}^{n} i_j$. And the corresponding weight is

$$w_{j_{i_1}\cdots j_{i_n}}^{i_1\ldots i_n} = (-1)^{P+n-|\vec{i}|}\begin{pmatrix} n-1 \\ n+P-|\vec{i}| \end{pmatrix}\prod_m w_{j_{i_m}}^{i_m}, \tag{13}$$

where $\binom{n-1}{n+P-|\vec{i}|}$ is a combination number and w is the weight for the corresponding quadrature point. It was shown that interpolation on a Smolyak grid ensures an error bound for the mean-square error [33]

$$|E_P| = O\left(N_P^r(\log N_P)^{(r+1)(n-1)}\right),$$

where N_P is the number of quadrature points and r is the order of the maximum derivative that exists for the function. The number of quadrature points increases as $O(n^P/(P)!)$.

It can be shown that Smolyak quadrature of at least level P is required for an order P representation. The reason is that the approximation contains order P polynomials for both $x(\xi)$ and $H_j(\xi)$ for some j. So there exists $x(\xi)H_j(\xi)$ with order $2P$, which requires Smolyak quadrature points of at least level P with degree $2P+1$ of exactness.

Therefore, levels 2 and 1 Smolyak quadratures are required for quadratic and linear model, respectively. The numbers of quadrature points are about $2n$ and $2n^2$ for the linear and the quadratic model, respectively. The time cost is about the same as the Taylor-conversion method, while keeping the accuracy of homogenous chaos expansion.

In addition to the Smolyak quadrature technique, we also employ several accelerating techniques summarized as follows:

- When n is too small, the number of Smolyak quadrature points may be larger than that of direct tensor product of Gaussian quadrature. For example, if there are only two variables, the number is 5 and 14 for levels 1 and 2 Smolyak quadratures, compared to 4 and 9 for direct tensor product. In this case, the Smolyak quadrature will not be used.
- The set of quadrature points (12) may contain the same points with different weights. For example, the level 2 Smolyak quadrature point set for three variables contain four instances of the point (0,0,0). Combining these points by summing the weights reduces 3 times of computation of $x(\vec{\gamma}_i)$.

5.3. Random variables transformation and reduction

In our gate-based approach, instead of using grid-based partitioning, as in [1], to reduce the number of channel length variables in presence of the strong spatial correlation, we applied the principal component analysis (PCA) to reduce the number of random variables. Our method starts with the following random variable vectors:

$$\mathbf{L} = [L_1, L_2, \ldots, L_n] + \delta L_{inter}, \quad \mathbf{T_{ox}} = [T_{ox1}, T_{ox2}, \ldots, T_{oxn}] + \delta T_{ox,inter}, \tag{14}$$

where n is the total number of gates on the whole chip, δL_{inter} and $\delta T_{ox,inter}$ represent the inter-die (global) variations. In total, we have $2n+2$ random variables. There exist correlations between L among different gates, represented by the covariance matrix $cov(L_i, L_j)$ computed by (1).

The first step is to perform PCA on L to get a set of independent random variables $\mathbf{L}' = [L'_1, L'_2, \ldots, L'_n]$, where $\mathbf{L} = \mathbf{P}\mathbf{L}'$, and $\mathbf{P} = \{p_{ij}\}$ is the $n \times n$ principal component coefficient matrix. In this process, singular value decomposition (SVD) is used on the covariance matrix, and the singular values are arranged in a decreasing order, which means that the elements in $\mathbf{L}'$ are arranged in a decreasing weight order. Then the number of elements in $\mathbf{L}'$ can be reduced by only considering the dominant part of $\mathbf{L}'$ as $[L'_1, L'_2, \ldots, L'_k]$ (for instance, the weight should be bigger than 1%), where k is the number of reduced random variables. Then every element L'_i in $\mathbf{L}'$ can be represented by orthogonal Gaussian random variable ξ_i with normal distribution:

$$L'_i = \mu_i + \sigma_i \xi_i, \tag{15}$$

where μ_i and σ_i are the mean value and standard deviation of L'_i. And $\mathbf{L}$ can be represented as

$$\mathbf{L} = \begin{pmatrix} \mu_{L1} \\ \mu_{L2} \\ \vdots \\ \mu_{Ln} \end{pmatrix} + \begin{pmatrix} p_{11} & \ldots & p_{1k} \\ p_{21} & \ldots & p_{2k} \\ \vdots & \vdots & \vdots \\ p_{n1} & \ldots & p_{nk} \end{pmatrix}\begin{pmatrix} \sigma_1\xi_1 \\ \sigma_2\xi_2 \\ \vdots \\ \sigma_k\xi_k \end{pmatrix} + \delta L_{inter}. \tag{16}$$

For $[T_{ox1}, T_{ox2}, \ldots, T_{oxn}]$, δL_{inter}, and $\delta T_{ox,inter}$, we can also represent them using the standard Gaussian variables as

$$T_{ox,j} = \mu_{ox,j} + \sigma_{ox,j}\xi_{ox,j}, \quad \delta L_{inter} = \sigma_{L,inter}\xi_{L,inter}, \quad \delta T_{ox,inter} = \sigma_{ox,inter}\xi_{ox,inter}, \tag{17}$$

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where $\xi_{ox,j}$, $\xi_{L,inter}$, and $\xi_{ox,inter}$ are independent orthonormal Gaussian random variables. As a result, we can present **L** and $\mathbf{T_{ox}}$ by $k+n+2$ independent orthonormal Gaussian random variables:

$$\boldsymbol{\xi} = [\xi_1, \xi_2, \ldots, \xi_{k+n+2}]. \tag{18}$$

Then the $I_{sub}(\mathbf{L}, \mathbf{T_{ox}})$ and $I_{gate}(\mathbf{L}, \mathbf{T_{ox}})$ can be modeled as $I_{sub}(\boldsymbol{\xi})$ and $I_{gate}(\boldsymbol{\xi})$, respectively.

But among the $k+n+2$ variables, only $k+2$ variables related to the channel lengths are correlated. In other words, the n variables $T_{ox,i}$ of each gate are independent. As a result, for the j th gate, we only have $k+3$ independent variables, the corresponding variable vector, $\xi_g = \{\xi_{g,j}\}$, is defined as

$$\xi_{g,j} = [\xi_1, \ldots, \xi_k, \xi_{ox,j}, \xi_{L,inter}, \xi_{ox,inter}]. \tag{19}$$

5.4. Computation of full-chip leakage currents

For each gate, we need to present the leakage currents in order-2 Hermite polynomials first as shown below for both subthreshold and gate leakage currents—$I_{sub}(\boldsymbol{\xi}_{\mathbf{g,j}})$ and $I_{gate}(\boldsymbol{\xi}_{\mathbf{g,j}})$:

$$I_{sub}(\boldsymbol{\xi}_{\mathbf{g,j}}) = \sum_{i=0}^{P} I_{sub,i,j} H_i^2(\boldsymbol{\xi}_{\mathbf{g,j}}), \quad I_{gate}(\boldsymbol{\xi}_{\mathbf{g,j}}) = \sum_{i=0}^{P} I_{gate,i,j} H_i^2(\boldsymbol{\xi}_{\mathbf{g,j}}), \tag{20}$$

where $H_i^2(\boldsymbol{\xi}_{\mathbf{g,j}})$' s are order-2 Hermite polynomials. $I_{sub,i,j}$ and $I_{gate,i,j}$ are then computed by the numerical Gaussian quadrature method discussed in Sections 5.1 and 5.2. Let S be the size of Z-dimensional second order (level-2) quadrature point set Θ_Z^2 and $Z = k+3$. Then $I_{sub,i}$ and $I_{gate,i}$ can be computed as follows:

$$I_{sub,i,j} = \sum_{l=1}^{S} I_{sub}(\vec{\gamma}_l) H_i^2(\vec{\gamma}_l) w_l / \langle H_i^2(\boldsymbol{\xi}_{\mathbf{g,j}}) \rangle, \tag{21}$$

$$I_{gate,i,j} = \sum_{l=1}^{S} I_{gate}(\vec{\gamma}_l) H_i^2(\vec{\gamma}_l) w_l / \langle H_i^2(\boldsymbol{\xi}_{\mathbf{g,j}}) \rangle, \tag{22}$$

where $I_{sub}(\vec{\gamma}_l)$ and $I_{gate}(\vec{\gamma}_l)$ are computed using (3) and (4).

As a result, their coefficients for i th Hermite polynomial at j th gate can be added directly as

$$I_{leakage,i,j} = \sum I_{sub,i,j} + \sum I_{gate,i,j}. \tag{23}$$

After the leakage currents are calculated for each gate, we can proceed to compute the leakage current for the whole chip as follows:

$$I_{leakage}(\boldsymbol{\xi}) = \sum_{j=1}^{n} (I_{sub}(\boldsymbol{\xi}_{\mathbf{g,j}}) + I_{gate}(\boldsymbol{\xi}_{\mathbf{g,j}})). \tag{24}$$

The summation is done for each coefficient of Hermite polynomials. Then we obtain the analytic expression of the final leakage currents in terms of the $\boldsymbol{\xi}$.

We can then obtain the mean value, variance PDF and CDF of the leakage current very easily. For instance, the mean value and variance for the full-chip leakage current are

$$\mu_{leakage} = I_{leakage,0th}, \tag{25}$$

$$\sigma_{leakage}^2 = \sum I_{leakage,1st}^2 + 2\sum I_{leakage,2nd,type1}^2 + \sum I_{leakage,2nd,type2}^2, \tag{26}$$

where $I_{leakage,ith}$ is the leakage coefficient for i th Hermite polynomial of second order defined as follows:

$$H_{0th}(\boldsymbol{\xi}) = 1, \quad H_{1st}(\boldsymbol{\xi}) = \xi_i, \quad H_{2nd,type1}(\boldsymbol{\xi}) = \xi_i^2 - 1, \quad H_{2nd,type2}(\boldsymbol{\xi}) = \xi_i \xi_j, \quad i \neq j. \tag{27}$$

5.5. Time complexity analysis

To analyze the time complexity, one typically does not count the pre-characterization cost of step 1 in Fig. 6. For PCA step (step 2), which essentially uses singular value decomposition (SVD) on the covariance matrix, its computation cost is $O(nk^2)$, if we are only interested in the first k dominant singular values. This is the case for strong spatial correlation.

In step 3, we need to compute the weights of level 2 $(k+3)-$dimensional Smolyak quadrature point set. For quadratic model with $k+3$ variables, the number of Smolyak quadrature points is about $(k+3)^2$. So the time cost for generating Smolyak quadrature point set is $O((k+3)^2)$.

In step 4, we need to call (3) and (4) S times for each gate. In each call, we need to compute $k+3$ variables in the Hermite polynomials. The computing cost for the two steps is $(O(n(k+3) \times S))$, where n is the number of gates. After the leakage currents are computed for each gate, it takes $O(n(k+3))$ to compute the full-chip leakage current.

The total computing cost is $O(nk^2 + (k+3)^2 + n(k+3) S + n(k+3))$. For second order Hermite polynomials, $S \propto k^2$, so the time complexity becomes $O(nk^3)$. If $k \ll n$ (for strong spatial correlation), we end up with a linear time complexity $O(n)$. In the sub-90 nm VLSI technologies, the spatial correlation is really strong, and in the down-scaling process, the spatial correlation will become stronger, which makes sure our method can achieve pretty good time complexity.

6. Experimental results

The proposed method is implement in Matlab 7.4.0. For comparison purpose, we also implement the grid-based method in [1] and the pure Monte Carlo method. All the experimental results are carried out in a Linux system with quad Intel Xeon CPUs with 2.99 GHz and 16 GB memory.

The methods for full-chip statistical leakage estimation are tested on circuits in the PDWorkshop91 benchmark set. The circuits are synthesized with Nangate Open Cell Library and the placement is from MCNC [34]. The technology parameters come from the 45 nm FreePDK Base Kit and PTM models [21].

Table 2 shows the detailed parameters for gate length and gate oxide thickness variations. Here we choose two set of σ^2 distributions. The last column of Table 2 shows the standard deviation (σ) of each variation. The 3σ values of parameter variations for L and T_{ox} are set to 12% of the nominal parameter values, of which inter-die variations constitute 20% and intra-die variations, 80% (Case 1); inter-die variations constitute 50% and intra-die variations, 50% (Case 2). The parameter L is modeled as sum of correlated sources of variations, and the gate oxide thickness T_{ox} is modeled as an independent source of variation. The same framework can be easily extended to include other parameters of variations. Both L and T_{ox} in each gate are modeled as Gaussian parameters. For the correlated L, the spatial correlation is modeled based on the exponential special correlation in (1). For [1], we still partition the chip into a number of regular grids and the numbers of grid partitions of spatial correlation model used for the benchmarks are given in Table 2.

For comparison purposes, we perform Monte Carlo (MC) simulations with 500,000 runs, the grid-based method in [1], and the new method on the benchmarks. The large number of MC runs is due to the fact that proposed method is quite accurate. Fig. 7 shows the full-chip leakage current distribution (PDF and CDF) of circuit SC0 with 125 gates, considering variation in gate length and gate oxide thickness as in Table 2 for Case 1, and

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Table 2
Process variation parameter breakdown for 45 nm technology.

	Case 1			Case 2		
	σ^2 distribution		(σ)	σ^2 distribution		(σ)
Gate length (L)	Inter-die	20%	4%$*$ 18 nm	Inter-die	50%	4%$*$ 18 nm
	Intra-die			Intra-die		
	$*$ Spatial correlated	80%		$*$ Spatial correlated	50%	
Gate oxide thickness (T_{ox})	Inter-die	20%	4%$*$ 1.8 nm	Inter-die	50%	4%$*$ 1.8 nm
	Intra-die			Intra-die		
	$*$ Non-correlated	80%		$*$ Non-correlated	50%	

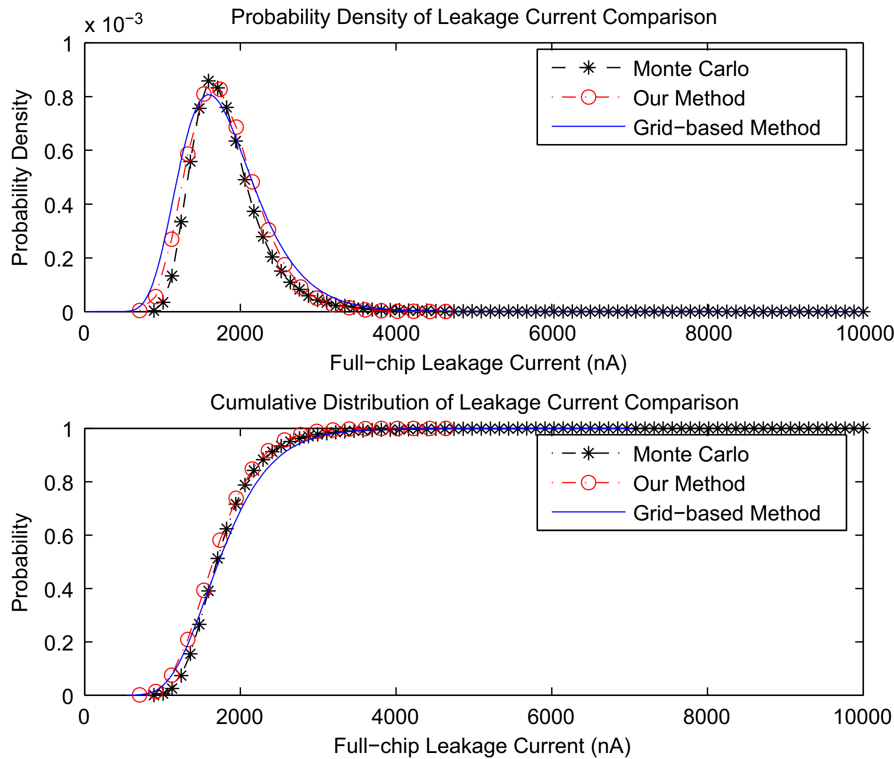

Fig. 7. Distribution of the total leakage currents of the proposed method, the grid-based method and the MC method for circuit SC0 (process variation parameters set as Case1).

Table 3
Comparison of the mean values of full-chip leakage currents among three methods.

Circuit name	Gate #	Grid #	μ of I_{sub} (μA)			Errors (%)		μ of I_{gate} (μA)			Errors (%)		μ of I_{leak} (μA)			Errors (%)	
			MC	[1]	New	[1]	New	MC	[1]	New	[1]	New	MC	[1]	New	[1]	New
Case 1																	
SC0	125	4	0.81	0.72	0.79	−10.5	−1.89	1.03	1.03	1.03	−0.10	−0.03	1.84	1.75	1.82	−4.67	−0.84
SC2	1888	16	11.75	10.70	11.50	−8.9	−0.22	18.23	18.18	18.21	−0.25	−0.10	29.98	28.88	29.70	−3.65	−0.91
SC5	6417	64	38.35	34.49	37.73	−10.1	−1.62	69.52	69.15	69.44	−0.54	−0.11	107.9	103.6	107.2	−3.93	−0.65
Case 2																	
SC0	125	4	0.80	0.72	0.79	−10.5	−1.53	1.04	1.03	1.03	−0.43	−0.36	1.84	1.75	1.82	−4.85	−0.87
SC2	1888	16	11.81	10.70	11.54	−9.38	−2.29	18.21	18.18	18.21	−0.13	−0.01	30.02	28.89	29.75	−3.77	−0.89
SC5	6417	64	107.9	103.6	107.2	−3.9	−0.65	107.9	103.6	107.2	−3.9	−0.65	107.9	103.6	107.2	−3.9	−0.65

the spatial correlation of gate length. It shows that our method fits very well with the MC results, and is more accurate than [1]. Other test cases show the similar comparison results. The results of the comparison of mean values and standard deviations of full-chip leakage currents are shown in Tables 3 and 4. For Case 1, the average errors for mean value and standard deviation of the new gate-based method are 0.8% and 4.04%, respectively. While for the grid-based method in [1], the average errors for mean value and standard deviation are 4.08% and 39.7%, respectively. For Case 2, the average errors for mean value and standard deviation of the new gate-based method are 0.8% and 5.51%, respectively. While for the grid-based method in [1], the average errors for mean

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Table 4
Comparison standard deviations of full-chip leakage currents among three methods.

Circuit name	σ of I_{sub} (μA)			Errors (%)		σ of I_{gate} (μA)			Errors (%)		σ of I_{leak} (μA)			Errors (%)	
	MC	[1]	New	[1]	New	MC	[1]	New	[1]	New	MC	[1]	New	[1]	New
Case 1															
SC0	0.452	0.266	0.449	41.2	−0.55	0.300	0.488	0.296	62.4	−1.35	0.495	0.668	0.524	35.0	−5.77
SC2	8.448	4.407	8.145	−47.8	−3.59	5.165	7.629	5.116	47.71	−0.91	8.606	10.86	8.798	26.2	2.23
SC5	21.15	11.16	21.25	−47.22	−0.47	19.29	28.41	19.03	47.32	−1.35	26.19	41.36	25.11	57.9	−4.12
Case 2															
SC0	0.475	0.248	0.533	−47.8	12.24	0.473	0.450	0.472	−4.86	−0.11	0.632	0.726	0.689	14.9	9.04
SC2	9.159	4.595	9.759	−49.83	6.56	8.211	7.953	8.336	−3.14	1.52	10.71	12.03	11.36	12.33	6.13
SC5	26.19	41.36	25.11	57.9	−4.12	26.19	41.36	25.11	57.9	−4.12	26.19	41.36	25.11	57.9	−4.12

Table 5
CPU time comparison among three methods.

Circuit name	Case 1					Case 2				
	Cost time (s)			Speedup (%)		Cost time (s)			Speedup (%)	
	MC	[1]	New	[1]	New	MC	[1]	New	[1]	New
SC0	378.1	11.35	1.40	8.11	270.1	358.6	7.47	1.41	5.30	254.33
SC2	1.35×10^4	168.51	18.79	30.6	718.5	1.35×10^4	87.94	17.23	5.10	437.96
SC5	2.76×10^5	3335	121.2	27.52	2277	2.06×10^5	7798.3	443.95	17.56	464.33

value and standard deviation are 4.17% and 28.4%, respectively. Our gate-based method is more accurate than the grid-based method, especially for standard deviation value. Since we use 45 nm technology, while the results in [1] is based on 100 nm technology, the error ranges are different (in [1], the average errors for mean value and standard deviation are 1.3% and 4.1%). Results of the grid-based method in [1] will become worse when the technology scales down, since the dominant state assumption is not working any more.

And Table 5 also compares the CPU times of the three methods. From this table we can see that even our method is gate-based, it is still faster than the method in [1], which is grid-based. And the proposed method is much faster than the Monte Carlo method. On average, the proposed method has about 16× speedup over the grid based method in [1]. We notice that method in [1] will become faster with smaller number of grids used. But this can lead to large errors even with strong spatial correlations.

7. Conclusion

In this paper, we have presented a novel method for analyzing the full-chip leakage current distribution of digital circuit. The new method considers both intra-die and inter-die variations with spatial correlations. The new method employs the orthogonal polynomials and multi-dimensional Gaussian quadrature method to represent and compute variational leakage at the gate level, and uses the orthogonal decomposition to reduce the number of random variables exploiting the strong spatial correlations of intra-die variations. The resulting algorithm compares very favorable with the existing grid-based method in terms of both CPU time and accuracy. The new method has about 16× speedup over [1] with constant better accuracy.

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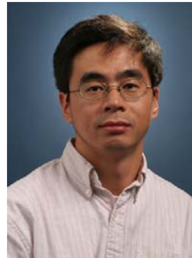

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