Transactions Briefs

Minimum Decoupling Capacitor Insertion in VLSI Power/Ground Supply Networks by Semidefinite and Linear Programs

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Abstract—**Nanometer-scale VLSI design demands reliable on-chip power/ground (P/G) supply. Decoupling capacitors effectively reduce P/G supply fluctuation at the cost of leakage increase and yield loss. Existing P/G supply network decoupling capacitor insertion techniques are based on sensitivity analysis and greedy optimization. In this paper, we propose a semidefinite program and a linear program for minimum decoupling capacitor insertion in a P/G supply network, which are global optimizations with theoretically guaranteed supply voltage degradation bounds. We also propose scalability improvement schemes which enable application of the proposed semidefinite and linear programs to practical industry designs. Our experimental results on industry designs verify that the proposed semidefinite program guarantees supply voltage degradation bound for all possible supply current sources, while the proposed linear program achieves the most accurate supply voltage degradation control for a given set of supply current sources.**

Index Terms—**Design, reliability, verification.**

I. Introduction

VLSI technology scaling has lead to increased voltage drop along power/ground (P/G) supply networks, due to: 1) increased interconnect resistance as a result of interconnect width and thickness scaling; 2) increased supply current density as a result of increased device density on a chip; and 3) increased inductance effect as a result of increased clock frequency. Decreased P/G supply voltage reduces transistor noise margin, degrades transistor and system performance, and leads to logic malfunction and system breakdown in worst cases. Consequently, P/G supply voltage degradation has an increasingly significant effect on VLSI reliability and performance variability. Achieving P/G supply signal integrity is crucial for nanometer-scale VLSI designs.

Decoupling capacitors have been recommended to be inserted as much as possible as a "rule of thumb" for package and IC designers. However, on-chip decoupling capacitors increase leakage current and lead to yield loss due to short circuit defect occurrence. As a result, VLSI designs pursue minimum decoupling capacitor insertion for guaranteed P/G supply signal integrity and maximized manufacturing yield.

An early heuristic proposed to insert decoupling capacitors in a P/G network based on a scaling factor and estimate needed decoupling capacitance based on the injected charge at the violation node and the maximum permissible voltage degradation [16]. We show that this leads to optimistic (insufficient) decoupling capacitance insertion (see Section VII). Later approaches are based on sensitivity analysis, e.g., small (large) change sensitivity is proposed as the voltage sensitivity of a node (all violation nodes) with respect to all decoupling capacitors, and enables a greedy optimization [2]. Voltage "droop," or time domain supply voltage drop integral at all violation nodes, is given by adjoint sensitivity analysis and is fed into a quadratic solver for nonlinear optimization [13]. The work in [9] improved the sensitivity calculation by applying the time domain merged adjoint network method. Sensitivity-based optimization was further enhanced by exploiting the local effects of adding decoupling capacitors using partitioning-based optimization scheme with time domain merged adjoint method [10]. Sensitivity-based optimization approaches require repeated transient simulation of a P/G network at each optimization step, which is quite time consuming in general. Further, the resultant problem is a general nonlinear optimization problem, which does not guarantee a global optimum solution, and is difficult to solve in general.

We observe the equivalence of voltage and timing bounds in a circuit, i.e., upper bounding supply voltage drop by αV_{dd} is equivalent to lower bounding the αV_{dd} delay in the P/G supply network. We apply timing optimization techniques, specifically, a semidefinite program and a linear program, for minimum decoupling capacitor insertion in a P/G supply network, which achieve theoretically guaranteed supply voltage bounds. We propose scalability improvement schemes which enable application of the proposed semidefinite and linear programs to practical industry designs. Our experimental results on an industry design verify that the proposed semidefinite program guarantees supply voltage degradation bound for all possible supply current sources, while the proposed linear program achieves the most accurate supply voltage degradation control for a given set of supply current sources.

The rest of this paper is organized as follows. We present a problem formulation, a semidefinite program, and a linear program for minimum decoupling capacitor insertion in an *RC* P/G supply network in Sections II–IV, respectively. The scalability improvement schemes in Section V enable application of the proposed programs to practical industry design instances, which we show in Section VI. We conclude in Section VII.

II. Problem Formulation

A P/G supply network in the latest technologies is modeled as a distributed *RC* interconnect, including P/G supply pads which are modeled as dc voltage sources, and switching transistors which draw supply currents and are modeled as current sources. Modified nodal analysis (MNA) forms the foundation of circuit analysis techniques. For example, for a signal propagation interconnect in a VLSI design represented in an *RC* network of n nodes and k inductors driven by N voltage sources, MNA is given as follows [12]:

$$\begin{aligned} C\dot{x}_n &= -Gx_n + Bu_N \\ i_N &= L^T x_n \end{aligned} \tag{1}$$

where

$$C = \begin{bmatrix} Q & 0 \\ 0 & H \end{bmatrix} G = \begin{bmatrix} N & E \\ -E^T & 0 \end{bmatrix} x_n = \begin{bmatrix} v \\ i \end{bmatrix}$$

and $G \in R^{(n+k)\times(n+k)}$ is the conductance matrix; $C \in R^{(n+k)\times(n+k)}$ is the susceptance matrix; $B \in R^{n\times N}$ gives the nodes of the N voltage sources as voltage inputs; $L \in R^{n\times N}$ gives the nodes of the N voltage sources as current outputs; $i_N \in R^N$ gives the currents of voltage sources; $u_N \in R^N$ gives the voltages of voltage sources; $x_n \in R^{n+N+k}$ gives the variables of the system; $v \in R^n$ gives the node voltages; $i \in R^{N+k}$ gives the branch currents

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for voltage sources and inductors; $N \in R^{n\times n}$ is the resistance matrix; $Q \in R^{n\times n}$ is the capacitance matrix; and $E \in R^{n\times k}$ consists of ones, minus ones, and zeros, representing the current variables in KCL equations.

However, such MNA circuit equations cannot be applied to a P/G supply network. A P/G supply network includes not only voltage sources but also current sources abstracted from switching transistors. The supply pads have constant nodal voltages which are not unknown variables. Further, to apply most of today's semidefinite programming packages [4], [5] requires symmetry of the matrices in MNA circuit equations.

We propose a specific set of MNA circuit equations for a P/G supply network. We separate nodes in a P/G supply network into two categories: nodes of reference voltage, e.g., P/G pads, and nodes with variable voltages, i.e., free nodes, and include only voltages of free nodes as unknown variables in MNA circuit equations. The conductance and the susceptance matrices are guaranteed to be symmetric, which enables application of semidefinite programming optimization techniques

$$(G + sC)V = Bu + J \tag{2}$$

where $V \in R^{n\times 1}$ is the vector of free node voltages; $u \in R^{1\times 1}$ is the scalar reference P/G supply voltage; $B \in R^{n\times 1}$ gives conductances between each free node and the reference voltage nodes; $J \in R^{n\times 1}$ gives supply currents at each free node; $C \in R^{n\times n}$ gives ground capacitances C_{ii} for each free node i; and $G \in R^{n\times n}$ gives conductances, G_{ij} is the conductance between two free nodes i and j, $G_{ii} = \sum_{j\neq i} G_{ij} + B_i$ includes all conductances between node i and other free or reference nodes.

We adopt this formulation for the rest of this paper, and formulate the P/G supply network decoupling capacitor insertion problem as follows.

1) Problem 1 (P/G Decoupling Capacitor Insertion): Given the following:

a) P/G network G;
b) supply currents J;
c) maximum supply current duration time T;
d) supply voltage degradation bound $\alpha V_{\rm dd}$;

we find the minimum total decoupling capacitance $\sum_i C_{ii}$ such that supply voltage degradation at each node in G is within bound $\alpha V_{\rm dd}$ in time T.

III. Semidefinite Programing

Semidefinite programming is a recently developed powerful optimization technique, which finds wide applications such as in control systems engineering and relaxations of combinatorial optimization problems [1], [7], [15]. A semidefinite program optimizes a linear objective subject to a linear matrix inequality as follows:

$$\begin{aligned} &\text{Minimize} \quad c^T x \\ &\text{Subject to} \quad A(x) \succeq 0 \end{aligned} \tag{3}$$

where $A(x) = A_0 + x_1 A_1 + \cdots + x_m A_m$, $A_i = A_i^T \in R^{n\times n}$. Such a program is a convex optimization problem and can be solved very efficiently using recent interior-point methods [1], [7], [15].

Vandenberghe *et al.* propose that by limiting the poles of an *RC* interconnect, we can bound all possible signal transition times in the system. Because the poles p_i are given by the reciprocals of the eigenvalues of the $G^{-1}C$ matrix [12], bounding the poles of a system can be formulated as a *generalized eigenvalue minimization problem* (GEVP) as follows [14]:

$$\begin{aligned} &\text{Minimize} \quad t \\ &\text{Subject to} \quad tG - C \succeq 0 \end{aligned} \tag{4}$$

where scalar t is an upper bound of the time constants (i.e., reciprocals of the poles) of the interconnect system, and $\succeq$ denotes that the left side matrix $M = tG - C$ is positive semidefinite.

Definition 1: A matrix M is *positive semidefinite* if and only if $x^T Mx \geq 0$ for any vector x.

A positive semidefinite matrix has the following properties:

1) all of its diagonal elements are larger than the sum of elements in the same row or column;
2) all of its eigenvalues are non-negative.

To guarantee the eigenvalues of the $tG - C$ matrix to be non-negative, t needs to be larger than all the eigenvalues of matrix $G^{-1}C$, i.e., the reciprocals of the poles, or all the possible time constants in the interconnect system [14]. By upper bounding the time constants, we bound the maximum possible signal transition time in the interconnect system.

Based on the observation that upper bounding supply voltage degradation is equivalent to lower bounding signal transition times in a P/G supply network, we propose a semidefinite program for minimum decoupling capacitance insertion for bounded supply voltage degradation, by lower bounding the time constants in the interconnect system as follows:

$$\begin{aligned} &\text{Minimize} \quad \sum_i C_{i,i} \\ &\text{Subject to} \quad C - TG \succeq 0 \end{aligned} \tag{5}$$

where scalar T is a predefined time frame, e.g., the clock cycle time or the maximum transient supply current duration time. To guarantee the $C - TG$ matrix to be positive semidefinite, T needs to be smaller than all the eigenvalues of the $G^{-1}C$ matrix, i.e., the reciprocals of the poles, or all the possible time constants in the interconnect system. By lower bounding all time constants in a P/G network, we upper bound the largest possible transient voltage variation in the given time frame T.

Semidefinite programming relaxes the original problem solution space to a convex super-space, by providing a pessimistic bound for all the time constants in a linear system, e.g., semidefinite programming-based decoupling capacitor insertion in a P/G supply network provides a universal bound for all the possible time constants of the nodal voltages and the branch currents. Such a programming is pessimistic because it does not take into account the differences in nodal voltage bounds and supply current variations. Voltage bound can be different for different nodes in a P/G network, e.g., gates in a timing critical path need stricter power supply voltage bound for the timing constraints and the same P/G supply network can be applied to different supply currents, which could result in significantly different nodal voltages. This is because even the poles of a system are fixed, the residuals of a response vary with the inputs and gives different significance of the poles. To achieve tighter bounds, we need to: 1) take inputs into account; 2) differentiate bounds for each node; and 3) adopt a more accurate timing metric. In Section IV, we propose a linear program based on the Elmore delay timing metric which achieves near-optimal decoupling capacitor insertion in a P/G supply network.

IV. Linear Programing

Elmore proposed a general timing metric of a linear system in 1948, which is later called Elmore delay [6], [8]. Given a transfer function $h(s)$ of a linear system, the output of the system is given by Laplace domain multiplication or time domain convolution of the input and the transfer function of the system. For a step input, the output of the system is given by the integral of the transfer function in time domain. Normalizing the step response by its final value gives a response which approaches unity at infinite time. The derivative of this normalized step response has unit integral and resembles a probabilistic density function of a random variable. Elmore proceeded to propose that the median of this function, which is the time for the step response to achieve 50% of its final value, can be approximated by the mean of this function [6], [8].

Consider a ground network (because bounding power supply voltage drop in a power supply network is equivalent to bounding ground supply voltage bounce in the same network as a ground supply network) of resistance G and capacitance C. Substituting $u = 0$ into (2) gives the nodal voltages by

$$V = (I - sG^{-1}C)^{-1}G^{-1}J. \tag{6}$$

For step input supply currents

$$J(s) = \frac{\hat{J}}{s} \tag{7}$$

the nodal voltages and their moments are given by [12]

$$\begin{aligned} V(s) &= M_{-1}s^{-1} + M_0 + M_1 s + \cdots + M_i s^i \\ M_{-1} &= G^{-1}\hat{J} \\ M_0 &= G^{-1}CG^{-1}\hat{J} \\ M_i &= (G^{-1}C)^{i+1}G^{-1}\hat{J}. \end{aligned} \tag{8}$$

The final values of the nodal voltages, i.e., the nodal voltages at infinite time $U = V(t = \infty)$, equal to the nodal voltages in the same resistive network G without capacitance C driven by dc supply current $\hat{J}$, which is M_{-1}

$$U = M_{-1} = G^{-1}\hat{J}. \tag{9}$$

Elmore delay (i.e., the time of a nodal voltage to achieve 50% of its final value) is given by the mean (first moment) of the derivative of the normalized step response, or the zeroth moment of the normalized step response [6], [8]

$$T^{\mathrm{elm}} = \frac{M_0}{M_{-1}} = \frac{G^{-1}CG^{-1}\hat{J}}{G^{-1}\hat{J}}. \tag{10}$$

Elmore delay is widely adopted in today's VLSI design automation community partly because of the following reasons. First, for a tree structure *RC* network, Elmore delay has a simple recursive computation formula and can be computed in linear time and incrementally updated in constant time [8]. Second, for an *RC* network and a monotonic input, the 50% delay is bounded by Elmore delay, i.e., it increases and approaches Elmore delay as the input signal transition time increases and approaches infinity [8]. In other words, the mismatch between a 50% delay and an Elmore delay depends on the input signal transition time. In a VLSI design where signal transition times are bounded by buffer insertion based on design rules, the deviation of an Elmore delay from a 50% delay is also bounded and a scaling ratio can be applied to more accurately estimate the 50% delay [8].

For a single capacitor c driven by a step input through a resistor r, the 50% delay is given by $\lg 2$ times Elmore delay rc. For a sufficiently large *RC* network, signal transition time degrades along with signal propagation, and the 50% delay approaches Elmore delay. We approximate nodal voltages by scaled Elmore delays by

$$V(t) = U\left(1 - e^{-(t/kT^{\mathrm{elm}})}\right) \tag{11}$$

where the scaling factor $\lg 2 \le k \le 1$ can be best chosen based on the size of the P/G supply *RC* network. Consequently, bounding nodal voltages within αV_{dd}

$$V(t) \le \alpha V_{\mathrm{dd}} \quad t \le T \tag{12}$$

is equivalent to bounding their Elmore delays

$$T^{\mathrm{elm}} = \frac{G^{-1}CG^{-1}\hat{J}}{G^{-1}\hat{J}} \ge -\frac{k^{-1}T}{\log\left(1 - \frac{\alpha V_{\mathrm{dd}}}{G^{-1}\hat{J}}\right)}. \tag{13}$$

Note that we do not bound nodal voltages which final values are within the voltage bound, i.e., $G^{-1}\hat{J} < \alpha V_{dd}$. For such nodes, $\log\left(1 - \left(\alpha V_{\mathrm{dd}}/G^{-1}\hat{J}\right)\right) \le 0$ because $\log x = -\infty$ for $x < 0$, and the right-hand side in (13) becomes 0, which virtually yields no constraint.

Taking into account physical constraints on decoupling capacitor insertion, e.g., the maximum allowable decoupling capacitance $\xi_{i,i}$ at each location, a linear program for P/G supply network decoupling capacitor insertion is given as follows:

$$\begin{aligned} &\text{Minimize} && \sum_i C_{i,i} \\ &\text{Subject to} && \frac{G^{-1}CG^{-1}\hat{J}}{G^{-1}\hat{J}} \ge -\frac{k^{-1}T}{\log\left(1 - \frac{\alpha V_{\mathrm{dd}}}{G^{-1}\hat{J}}\right)} \\ &&& 0 \le C_{i,i} \le \xi_{i,i} \ \forall i. \end{aligned} \tag{14}$$

V. Scalability Improvement

To apply the proposed convex programming methods to practical VLSI design instances of millions of components, we select a group of decoupling capacitor insertion (DCI) candidate nodes in a P/G supply network and reduce the P/G supply network to include only the DCI candidate nodes. Such DCI candidate nodes can be selected to be the supply voltage degradation violation nodes or "hot spots," where decoupling capacitor insertion is the most efficient.

Existing block Krylov space-based model order reduction methods include matrix inversion computation [12] and are difficult to handle million component P/G supply network instances. To further improve scalability, we propose a direct measurement method as follows.

We first reduce the resistance matrix G to $\tilde{G}$. Compare MNA equations in the original resistive P/G network

$$V = G^{-1}J \tag{15}$$

and MNA equations in the reduced resistive network

$$\tilde{V} = \tilde{G}^{-1}\tilde{J} \tag{16}$$

where $\tilde{V}$, $\tilde{J}$, and $\tilde{G}^{-1}$ are, respectively, the subspaces of V, J, and G^{-1}, corresponding to the N decoupling capacitor insertion candidate nodes.

1) Observation 1: The ith column of $\tilde{G}^{-1}$ is given by the voltages $\tilde{V}$ of the decoupling capacitor insertion candidate nodes in the presence of a single unit supply current source at node i, i.e., $\tilde{J}_i \ne 0$, $\tilde{J}_{j \ne i} = 0$.

Therefore, we can apply a unit supply current source at node i and find the nodal voltages at the N DCI insertion nodes, which are the ith column of the $\tilde{G}^{-1}$ matrix. Any circuit simulation method can be applied to find the nodal voltages in the network, while SPICE simulation achieves the most accurate results.

Equivalent source currents in the reduced resistive network are then computed such that each node in the reduced resistive network has the same voltage as in the original resistive network, e.g., by solving a linear system as follows:

$$\tilde{V} = \tilde{G}^{-1}\tilde{J} \tag{17}$$

where $\tilde{V}$ gives the voltages at the nodes of the reduced resistive network, which are obtained from V the voltages in the original network.

TABLE I
TOTAL SUPPLY CURRENTS (A) IN PULSE FUNCTIONS OF 1-ns DURATION TIME, TOTAL DECOUPLING CAPACITANCE (pF), DELAY (ns) TO REACH $0.2\ V_{\rm dd}$, AND MAXIMUM VOLTAGE DROP (V), BY LINEAR PROGRAM (LP), SEMIDEFINITE PROGRAM (SDP), AND θ HEURISTIC IN AN INDUSTRY DESIGN

total current (A)	decap method	total decap (nF)	min delay (ns)	max vdrop (V)	run time(s)
5.613	LP	30.002	1.008	0.199	0.001
	SDP	55.892	2.6442	0.101	0.034
	θ	4.196	0.3515	0.275	0.000

Finally, equivalent capacitors in the reduced network can be achieved by solving (2) in the Laplace domain.

We summarize our scalable decoupling capacitor insertion linear program in Algorithm 1.

Algorithm 1: Scalable Decap Insertion Linear Program

Input: P/G network G, supply current J,
duration time T, voltage bound $\alpha V_{\rm dd}$

Output: Optimized P/G network with guaranteed voltage bound αV_{dd}

1. Select n decoupling capacitor insertion candidate nodes.
2. Compute $\tilde{G}^{-1}$
3. Compute $\tilde{J}$ by **(17)**
4. Perform linear program **(14)** with $\tilde{G}^{-1}$ and $\tilde{J}$
5. Find decoupling capacitances $\tilde{C}$

VI. EXPERIMENTAL RESULTS

We apply the proposed semidefinite and linear programs to a 90-nm technology industry design consisting of 34 623 cell instances. The power and the ground supply network includes two rings on the top two metal layers, five stripes on the second layer, and four pads at the center of the chip boundaries, respectively. We run Cadence Fire & Ice and extract a P/G network of 65 403 resistors and 35 118 capacitors, and generate supply current profiles by running VerilogXL. Our goal is to bound supply voltage degradation within 0.2 V in a 1-ns time frame by inserting decoupling capacitors.

We select 16 decoupling capacitor insertion candidate nodes with the largest supply currents, which correspond to 16 supply voltage degradation "hot spots," and reduce the P/G network to include only these 16 nodes by applying SPICE simulation to compute equivalent resistance between any two decoupling capacitor insertion candidate nodes. First, we generate the linear program in AMPL format and apply a commercial linear program solver CPlex to find the optimum decoupling capacitances. Second, we generate the semidefinite program in AMPL format and apply a semidefinite program solver CSDP [4] to find the decoupling capacitances. Last, we apply the θ heuristic [16] for decoupling capacitance insertion.

Table I compares the total decoupling capacitance, minimum delay, and maximum supply voltage degradation given by the three decoupling capacitor insertion methods. We observe that the semidefinite program gives pessimistic decoupling capacitance insertion (which bounds supply voltage degradation for all possible supply current sources), the θ heuristic gives optimistic (insufficient) decoupling capacitance insertion, while the proposed linear program gives the most accurate decoupling capacitance insertion, which lower bounds the minimum delay by 1 ns and upper bounds the voltage degradation by 0.2 V, for the given supply current sources.

Semidefinite and linear programs have superlinear polynomial time complexity and today's solvers handle up to hundreds of variables [4], [5]. For this test case, all three methods take minimum runtime, which are reported on a Linux i686 system with a P4 processor and 512 MB memory, and do not include the P/G network reduction process, which consists of 16 SPICE DC simulation runs, each takes 1.15 s.

VII. CONCLUSION

In this paper, we propose a semidefinite program and a linear program for P/G network decoupling capacitor insertion and a scalability improvement scheme which enables us to apply the proposed semidefinite and linear programs to practical P/G supply network instances. Our experimental results on an industry design verify that the proposed semidefinite program guarantees supply voltage drop bound for all possible supply current sources, while the proposed linear program achieves the most accurate supply voltage degradation control for a given set of supply current sources.

The proposed semidefinite and linear programs achieve optimality in theory. Suboptimality arises in reality because of: 1) inaccuracy in modeling and formulating the problem, in bounding an arbitrary supply current waveform in a step function (tighter bounds include "maximum supply current waveform envelopes" [3]) and in determining the maximum supply current duration time T (which depends on the underlying circuit switching activity) and 2) the physical constraints in locating the decoupling capacitors.

Future research directions include: 1) placement for decoupling capacitor insertion and 2) decoupling capacitor insertion as a means of timing optimization.

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