


Fast Electromigration Stress Evolution Analysis for Interconnect Trees Using Krylov Subspace Method

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Abstract—Electromigration effects are a key failure mechanism for copper-based dual damascene interconnects wires in semiconductor technologies. However, accurately predicting the time-to-failure for a complicated interconnect tree in a VLSI interconnect layout requires detailed knowledge of the stress evolutions over time, and is subject to time-varying currents and temperature. This is a challenging problem as one needs to solve the stress-based partial differential equations (PDEs) in the time domain for confined copper damascene interconnect trees for both void nucleation and void growth phases. To mitigate this problem, we propose a novel Krylov subspace-based method for fast numerical solutions to the stress PDEs. The new approach, which we call *FastEM*, is based on the finite-difference method which is used to first discretize the PDEs into linear time-invariant ordinary differential equations (ODEs). After discretization, a modified Krylov subspace-based reduction technique is applied in the frequency domain to reduce the size of the original system matrices so that they can be efficiently simulated in the time domain. The *FastEM* can perform the simulation process for both void nucleation and void growth phases under piecewise constant linear current density inputs and time-varying stressing temperatures. Furthermore, we show that the steady-state response of stress diffusion equations can be obtained from the resulting ODE system in the frequency domain, which agrees with the recently proposed voltage-based EM analysis method for EM immortality checks. Numerical results show that the proposed method can lead to about 1–2 orders of magnitude speed-up over existing finite-difference time-domain-based methods on large interconnect trees for both void nucleation and growth phases with negligible errors. We further show that for most of the interconnect trees tested; we only need a small number of dominant poles for sufficient accuracy.

Index Terms—Integrated circuit interconnections, integrated circuit reliability.

I. INTRODUCTION

ELECTROMIGRATION (EM) is a key reliability concern for copper-based back end of the line interconnects for

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nanometer VLSIs. A 2015 ITRS report predicts that the EM lifetime of interconnects of VLSI chips will be reduced by half for each generation of technology nodes [1] due to the increasing current density and shrinking wire line cross-sections, which determines the critical sizes for EM effects. EM-related reliability will become much worse for upcoming 10 nm and smaller geometry technologies, and it is urgent to address this “EM crisis” at different levels of design stacks in both design and run time.

Existing mean time to failure EM models based on Black’s equation [2] and Blech limit [3] are still employed in the industry. However, these methods have been subjected to growing criticism as they are empirical fitting-based models which are too conservative and scale poorly over different stressing conditions. They also fail to consider the initial stress, such as thermal and mechanical stress, which can significantly affect the time-to-failure of the interconnect. Furthermore, these models are based on measured data from a single wire segment. Practical VLSI copper damascene interconnects contain multisegment interconnect trees, defined as continuously connected wire segments within a single level of metallization terminated by diffusion barriers at vias and contacts. It was shown, experimentally, that the stress evolutions of wire segments in an interconnect tree are not independent [4]–[6]. As a result, accurately predicting the time-to-failure for a complicated interconnect tree requires detailed knowledge of the stress evolution subject to time-varying currents and temperature. This still remains a challenging problem as one needs to solve the stress-based [partial differential equations (PDEs)] in the time domain for confined interconnect trees for both void nucleation and void growth phases.

To mitigate these problems, more accurate physics-based EM models and assessment techniques have been proposed recently [7]–[10]. In [7] and [8], a compact time-to-failure model based on the hydrostatic stress PDE, known as Korhonen’s equation [11], was proposed. Initially, this EM model worked for only a single wire segment but has been extended to deal with multisegment interconnect trees based on the projected steady-state stress. However, it still cannot provide the time-dependent evolution of hydrostatic stress, which ultimately determines the failure times for multibranch interconnect trees [4], [12]. Recent methods have attempted to develop analytic solutions of the stress diffusion equations [9], [13]. Approaches in [9] were proposed to address EM modeling in multibranch interconnect trees. In this

approach, analytical solutions for stress evolutions of the stress PDE were derived for a few specific interconnect structures, but still cannot be applied to general multisegment interconnect trees. In [13], an integral transformation-based method was proposed to obtain the analytical solution for multisegment wires in a straight line. However, this method needs many terms (a few hundred) to obtain accurate results. Both methods also cannot accommodate time-varying stress current densities and temperatures. Recently, a more general finite-difference time-domain (FDTD)-based numerical analysis method has been proposed to solve the stress PDE [10], [14]. However, this method is still computationally intensive for full-chip level analysis. In [10], a finite-difference-based linear time invariant (LTI) system was formulated and reduction of the resulting system matrices was performed to speed up the time-domain simulation based on the matrix exponential method. However, this paper only presented speed-up results of an overall implementation and did not present accuracy or performance results specifically for the reduction algorithm.

In this paper, we propose a novel fast numerical approach to solve the stress PDEs based on the Krylov subspace method. The new approach, called *FastEM*, is based on the finite-difference method (FDM) for initial discretization of the PDE into linear time-invariant ordinary differential equations (ODEs). Then, a modified Krylov subspace-based reduction technique is applied in the frequency domain to reduce the original system matrices for efficient time-domain solutions. The *FastEM* can perform the Krylov subspace-based simulation process for both void nucleation and void growth phases under piecewise constant linear current density inputs and time-varying stressing temperatures. Furthermore, we show that the steady-state response of the stress diffusion equations can be obtained from the resulting ODE system in the frequency domain, which agrees with the recently proposed voltage-based EM analysis method for EM immortality check [15]. Numerical results show that the proposed method can lead to about 100X speed-up over an existing FDTD-based method on large interconnect trees for both void nucleation and growth phases with negligible errors. We further show that for the interconnect trees tested, we only need a small number of dominant poles for sufficient accuracy.

II. REVIEW OF EM PHYSICS AND STRESS MODELING

EM is a physical phenomenon of the migration of metal atoms along the direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate along the trajectory of conducting electrons. During the migration process, hydrostatic stress is generated inside the embedded metal wire due to momentum exchange between lattice atoms. Void and hillock formation are caused by conducting electrons at the opposite ends of the wire. Indeed, when a metal wire is passivated into a rigid confinement, which is the case for copper dual damascene structures, the wire volume changes (induced by the atom depletion and accumulation due to migration), and creates tension at the cathode end and compression at the anode end of the line. Fig. 1 shows the typical copper dual damascene interconnect structure, which

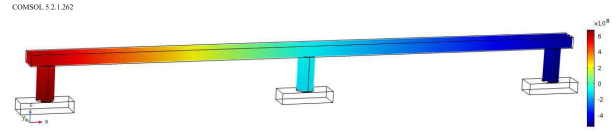


Fig. 1. Two-segment copper damascene wire with steady-state stress due to EM migration.

has three terminal vias connecting to other interconnect wires, and the steady-state stress distributions before void nucleation.

As time goes on, the lasting unidirectional electrical load will increase hydrostatic stress, as well as the stress gradient which acts as a counter-force for atomic migration along the metal line. Generally, when a line is long, this stress can reach a critical level, resulting in void nucleation at the cathode end and/or hillock formation at the anode end of line.

The currently employed method for estimating time to failure is based on Black's equation [2]

$$\text{MTTF} = A j^{-n} \exp\{E_a/k_{BT}\} \quad (1)$$

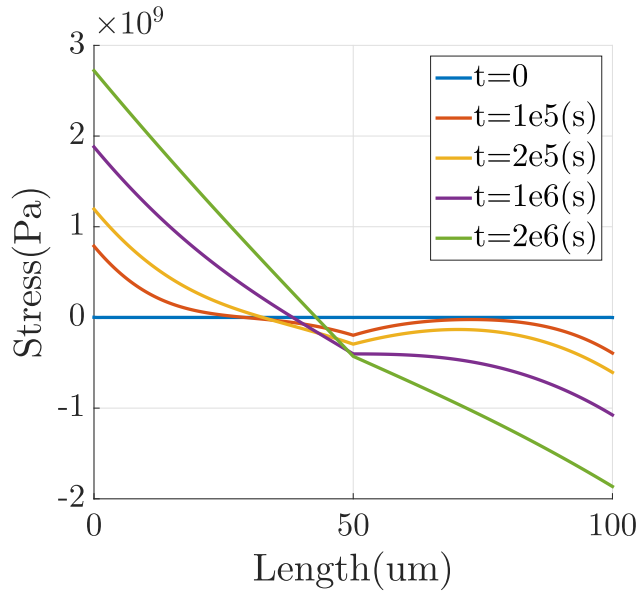
where j is the current density, k_B is the Boltzmann's constant; T is the absolute temperature; and E_a is the EM activation energy. The symbol A is a constant, which depends on a number of factors, including grain size, line structure and geometry, test conditions, current density, thermal history, etc. The current exponent n was found to be 2 for aluminum interconnects in [2]. However, Black's equation is under growing criticism as the extracted parameters, for example, the current exponent n and activation energy E_a , are not constant and are stress condition dependent.

To mitigate this problem, many physics-based EM models have been subsequently developed. A good summary of the published paper can be found in [16]. Among them, the stress-based model by Korhonen *et al.* [11] and metal atom vacancy concentration based model by Clement [17] have become popular. For a general interconnect wire in 2-Ds, transient hydrostatic stress evolution due to EM effects is analyzed in that model and stress $\sigma(x, t)$ is described by Korhonen's PDE with the following zero-flux boundary condition (BC) and initial stress condition (IC):

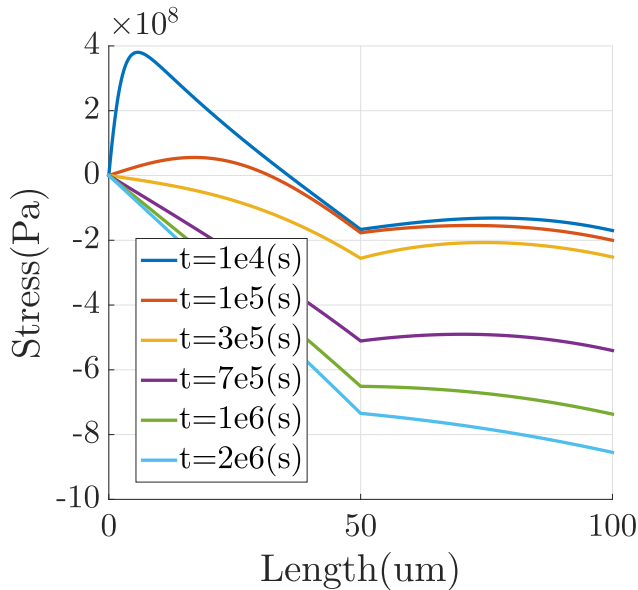
$$\begin{aligned} \text{PDE} : \quad & \frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[\kappa \left(\frac{\partial \sigma}{\partial x} + G_x \right) \right] + \frac{\partial}{\partial y} \left[\kappa \left(\frac{\partial \sigma}{\partial y} + G_y \right) \right] \\ \text{BC} : \quad & \frac{\partial \sigma}{\partial x}(0, t) = G_x, \quad \frac{\partial \sigma}{\partial y}(0, t) = G_y \\ \text{BC} : \quad & \frac{\partial \sigma}{\partial x}(L, t) = -G_x, \quad \frac{\partial \sigma}{\partial y}(L, t) = -G_y \\ & \text{at } 0 < t < t_{\text{nuc}} \\ \text{IC} : \quad & \sigma(0) = [\sigma_1(0), \sigma_2(0), \dots, \sigma_n(0)] \text{ at } t = 0. \end{aligned} \quad (2)$$

Here, $\kappa = D_a B \Omega / k_{BT}$ and $G = (eZ\rho j / \Omega)$, which is a function of current density j .

Once a void has nucleated, which is typically at or near a terminal node, the stress at the void will immediately go to zero. However, the stress around the void will be close to the same stress level as immediately prior to the nucleation [11], [18]. As a result, a very large stress gradient



(a)



(b)

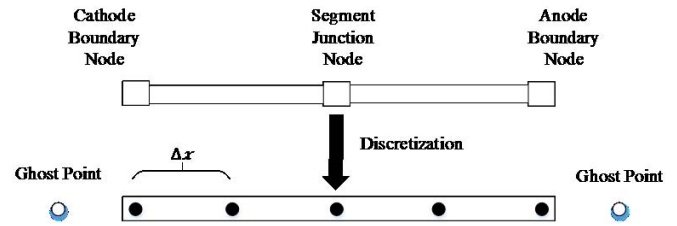
Fig. 2. EM-stress evolution in (a) nucleation phase and (b) growth phase.

will be formed around the voids at nucleation time, which can be described by [11]

$$\frac{\partial \sigma}{\partial x}(x_{\text{nuc}}, t) = \frac{\sigma(x_{\text{nuc}}, t)}{\delta}, \quad \text{at } t_{\text{nuc}} < t < \infty. \quad (3)$$

In (3), x_{nuc} is the location of the void nucleation at a boundary and δ is the width of the void interface [18].

Fig. 2(a) shows stress development over time in a two-segment wire (shown in Fig. 1) with Korhonen's equation for both nucleation phase [Fig. 2(a)] and growth phase [Fig. 2(b)]. For nucleation phase, over time, tensile (positive) stress will be developed at the cathode (left) node and compressive (negative) stress will be developed at the anode (right) node. The built-up stress (its gradient) will serve as the back force for


 Fig. 3. Discretization of the two-segment wire with length L , and segment lengths $(L/2)$.

atomic flux. If the highest stress at the cathode node exceeds the critical stress, voids will be created. The time to reach the critical stress is called nucleation time (t_{nuc}).

After the void is nucleated, it will begin to grow and resistance may increase. Fig. 2(b) shows stress evolution in the same wire for the growth phase. After a void is nucleated, the stress around the void becomes zero and a large stress gradient is generated in the vicinity as mentioned before. This gradient pushes the copper material flux to the anode so that a back force due to stress gradient will be built until the stress reaches steady state (the void growth will saturate in this case) as shown in this figure. However, this process and its PDEs are computationally expensive to solve, and improving upon this is the motivation for this paper.

III. LINEAR TIME INVARIANT ORDINARY DIFFERENTIAL EQUATIONS FOR EM STRESS EVOLUTION

In this section, we show how to perform the finite-difference discretization for the given stress PDE, also known as the Korhonen equation in (2), to create the LTI ODE system.

A two-segment wire example is used throughout the section for demonstration with total length L and separate G values for each segment as shown in Fig. 3. The wire is discretized into five nodes; two edge boundary nodes at each end of the wire, one junction node at the middle of the wire, and two nonboundary nodes, each between the junction, and an edge node.

The FDM is a method of finding a numerical solution to PDEs [19]. The PDE can be discretized using many different methods; in our implementation, a central difference method (4) is used to discretize the spatial variable x (and y in the 2-D case as shown later). We use the central difference method due to the low truncation error compared with other discretization methods, such as the forward and backward differences, at the cost of only adding one term to each equation. Note that this is different from the FDTD in [14], where time is also discretized

$$\frac{\partial \sigma}{\partial t}(x, t) = \kappa \frac{\sigma_{i+1} - 2\sigma_i + \sigma_{i-1}}{\Delta x^2}, \quad \kappa = \frac{D_a B \Omega}{kT}. \quad (4)$$

BCs are discretized depending on location (internal junctions or edges) and EM phase (nucleation or growth). Edge boundaries are introduced during the handling of ghost points in the discretization scheme. These ghost points are terms in the central difference scheme that do not correspond to

physical points on the wire structures. BCs are discretized using the backward difference scheme shown in

$$\begin{aligned} \text{Nucleation: } \frac{\partial \sigma}{\partial x}(0, t) &= \frac{\sigma_i - \sigma_{i-1}}{\Delta x} = G \\ \frac{\partial \sigma}{\partial x}(L, t) &= \frac{\sigma_{i+1} - \sigma_i}{\Delta x} = -G \\ \text{Growth: } \frac{\partial \sigma}{\partial x}(0, t) &= \frac{\sigma_i - \sigma_{i-1}}{\Delta x} = \frac{\sigma(0, t)}{\delta} \\ \frac{\partial \sigma}{\partial x}(L, t) &= \frac{\sigma_{i+1} - \sigma_i}{\Delta x} = -G. \end{aligned} \quad (5)$$

By isolating the ghost point term to one side of the equation, we can replace the ghost point in the original central difference equation (4) which allows us to eliminate the nonexistent point while also introducing the boundary condition. The following equation demonstrates the new central difference equation when the ghost point is eliminated at the cathode:

$$\frac{\partial \sigma}{\partial t}(0, t) = \frac{\kappa}{\Delta x^2} (G_1 \Delta x - \sigma_i + \sigma_{i+1}). \quad (6)$$

Internal junctions require no ghost point replacement and instead use the fact that flux is continuous at wire junctions to introduce the BCs as in

$$\frac{\partial \sigma}{\partial t} \left(\frac{L}{2}, t \right) = \frac{\kappa}{\Delta x^2} (\sigma_{i-1} - 2\sigma_i + \sigma_{i+1} + (G_2 - G_1)). \quad (7)$$

In (7), G_1 and G_2 belong to the two respective wire segments that meet at the junction. In addition, $L/2$ indicates that the example is a single wire with two segments where the junction boundary occurs at half the length of the whole wire.

As previously mentioned, we preserve the continuity of the time-domain term which allows us to rewrite these equations as an ODE and LTI dynamic system. Using the previously derived equations (4), (5), and (7) for boundary and internal nodes, we can rewrite these equations into the matrix format

$$\begin{aligned} \begin{bmatrix} \dot{\sigma}_1 \\ \dot{\sigma}_2 \\ \dot{\sigma}_3 \\ \dot{\sigma}_4 \\ \dot{\sigma}_5 \end{bmatrix} &= \frac{\kappa}{\Delta x^2} \begin{bmatrix} -1 & 1 & 0 & 0 & 0 \\ 1 & -2 & 1 & 0 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 1 & -2 & 1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix} \\ &\times \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \end{bmatrix} + \begin{bmatrix} \frac{\kappa \beta \rho}{\Delta x} & 0 \\ 0 & 0 \\ -\frac{2\kappa(\beta \rho)}{\Delta x} & \frac{2\kappa(\beta \rho)}{\Delta x} \\ 0 & 0 \\ 0 & -\frac{\kappa \beta \rho}{\Delta x} \end{bmatrix} \begin{bmatrix} j_1 \\ j_2 \end{bmatrix} \end{aligned} \quad (8)$$

where $\beta = (eZ/\Omega)$.

For the growth phase, the void is nucleated at the cathode node. Then, the resulting LTI system for the two-segment wire

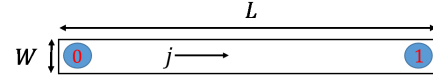


Fig. 4. Two-terminal wire with the electron flow indicated by the arrow.

case becomes

$$\begin{aligned} \begin{bmatrix} \dot{\sigma}_1 \\ \dot{\sigma}_2 \\ \dot{\sigma}_3 \\ \dot{\sigma}_4 \\ \dot{\sigma}_5 \end{bmatrix} &= \frac{\kappa}{\Delta x^2} \begin{bmatrix} (-\frac{\Delta x}{\delta} - 1) & 1 & 0 & 0 & 0 \\ 1 & -2 & 1 & 0 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 1 & -2 & 1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix} \\ &\times \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -\frac{2\kappa(\beta \rho)}{\Delta x} & \frac{2\kappa(\beta \rho)}{\Delta x} \\ 0 & 0 \\ 0 & -\frac{\kappa \beta \rho}{\Delta x} \end{bmatrix} \begin{bmatrix} j_1 \\ j_2 \end{bmatrix}. \end{aligned} \quad (9)$$

As a result, in both the void nucleation and growth phases, we can write the LTI ODE for stress evolution in the following general form:

$$\begin{aligned} \mathbf{C} \dot{\boldsymbol{\sigma}}(t) &= \mathbf{A} \boldsymbol{\sigma}(t) + \mathbf{B} \mathbf{j}(t) \\ \boldsymbol{\sigma}(0) &= [\sigma_1(0), \sigma_2(0), \dots, \sigma_n(0)]. \end{aligned} \quad (10)$$

In the case of (8), \mathbf{A} is the 5×5 coefficient matrix, \mathbf{C} is a 5×5 identity matrix, \mathbf{B} is 5×2 input matrix, and $\mathbf{j}(t)$ is the 2×1 column vector containing the current density of each wire segment for the respective time t .

We note that the presented example only requires equations for the 1-D case. However, to handle more general cases, these equations can simply be extended to the 2-D domain as shown in

$$\begin{aligned} \frac{\partial \sigma}{\partial t}(x, y, t) &= \kappa \frac{\sigma_{i+1,j} - 2\sigma_{i,j} + \sigma_{i-1,j}}{\Delta x^2} \\ &+ \kappa \frac{\sigma_{i,j+1} - 2\sigma_{i,j} + \sigma_{i,j-1}}{\Delta y^2}. \end{aligned} \quad (11)$$

A. Steady-State Analysis for Nucleation Phase

In this section, we show that the ODE for the nucleation phase which we derived from Korhonen's equation shown in (8) has the same steady-state stress result as the recently proposed voltage-based EM method in [15]. We demonstrate this using one simple example, a two-terminal wire as shown in Fig. 4.

We let the total length be L . We then use this wire segment length as the spatial step size and use the backward difference method shown in (5) for boundary derivation. The resulting system of equations for the two-terminal case is presented in

$$\begin{bmatrix} \dot{\sigma}_0 \\ \dot{\sigma}_1 \end{bmatrix} = \frac{\kappa}{L^2} \begin{bmatrix} -1 & 1 \\ 1 & -1 \end{bmatrix} \times \begin{bmatrix} \sigma_0 \\ \sigma_1 \end{bmatrix} + \begin{bmatrix} \frac{\kappa G}{L} \\ -\frac{\kappa G}{L} \end{bmatrix}. \quad (12)$$

We then rewrite these equations into the following format:

$$\begin{aligned}\dot{\sigma}(t) &= \mathbf{A}\sigma(t) + \mathbf{B}, \\ y(t) &= \mathbf{E}\sigma(t).\end{aligned}\quad (13)$$

In (13), $\mathbf{E} = (1, 0)$, meaning we select node 0, the cathode, as the output node for which we are obtaining the steady-state stress. Then, a Laplace transform can be applied and the resulting transfer function becomes

$$\mathbf{F}(s) = \mathbf{E}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}.\quad (14)$$

Then, we go back to (12), the resulting transfer function for the single-wire case becomes

$$F(s) = \frac{\kappa GL}{(sL^2 + 2\kappa)}.\quad (15)$$

Under step response, which is $1/s$ in frequency domain, we can then use the final value theorem to obtain the stress at $t = \infty$, which is the steady-state result of the system under step response as

$$\sigma_{\text{steady}} = \lim_{t \rightarrow \infty} f(t) = \lim_{s \rightarrow 0} sF(s) \frac{1}{s} = \frac{GL}{2}.\quad (16)$$

We then can compute the steady-state stress based on the voltage-based method [15]

$$\sigma_{\text{steady}} = V_E \frac{eZ}{\Omega} = \frac{jL\rho eZ}{2\Omega} = \frac{GL}{2}\quad (17)$$

where $V_E = jL\rho/2$ is the *EM voltage* at the cathode node (node 0) [15]. As we can see, the results from the two methods are identical.

In general, this is the case for general multisegment interconnects and the steady-state EM stress can be computed by either method. Furthermore, the voltage-based EM method [15] can provide an important relationship for stress values at different nodes as shown in (18) in Section IV.

IV. PROPOSED KRYLOV FAST EM STRESS ANALYSIS

In this section, we will present our new Krylov subspace-based fast EM stress analysis method. The following section contains several steps necessary for explanation of the proposed method and are outlined below:

- 1) We first show that the linear time-invariant system describing the dynamic stress evolution must be pre-processed to handle the inherent singularity of the \mathbf{A} matrix.
- 2) We then compare the steady-state response of the LTI system with a recently proposed steady-state method for EM stress evolution using frequency domain methods.
- 3) Next, we show the proposed Krylov-based model reduction technique using a modified Arnoldi process.
- 4) The temperature dependence of the EM effect and our method for handling time-varying temperatures is presented.
- 5) At last, we outline our method for normalization of the results to maintain numeric stability during model reduction and simulation.

A. Singularity Mitigation for EM ODE Matrices

Before we introduce our Krylov subspace-based method, we notice that the EM matrix \mathbf{A} in (8) or in (10) in general is

singular for our case. We notice that this is typically true for the nucleation phase; however, this will cause problems for the Krylov subspace-based method, which requires computing the inverse of \mathbf{A} to obtain the Krylov subspace. The reason is that the stress variables for the wire nodes are not independent as there is no ‘‘ground’’ stress node. As a result, one more independent equation is required to make this matrix nonsingular, and we will show the mitigation method below. We note that this singularity issue has also been observed in [10].

To mitigate this problem, we need to introduce one more independent equation (to replace one dependent equation) into the stress LTI system (10).

It turns out that such an independent stress equation can be found in the dynamic and steady-state stress of the LTI system (10) as a result of mass conservation and stress-strain relationship, and it has been shown in [20] and [15] that

$$\sum_k a_k \sigma_k = 0\quad (18)$$

where a_k is the total area of branches connected to the node k . This equation represents the conservation in the stress kinetics. Equation (18) is independent of any rows in the A matrix. As an example, for the two-segment wire in Fig. 3 with the same width for all the segments, we have

$$\sigma_1 + 2\sigma_2 + 2\sigma_3 + 2\sigma_4 + \sigma_5 = 0.\quad (19)$$

Therefore, we can use this equation to replace a dependent row (for example, the middle row of the \mathbf{A} matrix). With the new row, the A matrix becomes an invertible matrix. As an example, the modified equation, where the second equation or row is replaced, is shown in the following:

$$\begin{aligned}& \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \dot{\sigma}_1 \\ \dot{\sigma}_2 \\ \dot{\sigma}_3 \\ \dot{\sigma}_4 \\ \dot{\sigma}_5 \end{bmatrix} \\ &= \frac{\kappa}{\Delta x^2} \begin{bmatrix} -1 & 1 & 0 & 0 & 0 \\ 1 & 2 & 2 & 2 & 1 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 1 & -2 & 1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix} \\ &\times \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \end{bmatrix} + \begin{bmatrix} \frac{\kappa\beta\rho}{\Delta x} & 0 \\ 0 & 0 \\ -\frac{2\kappa(\beta\rho)}{\Delta x} & \frac{2\kappa(\beta\rho)}{\Delta x} \\ 0 & 0 \\ 0 & -\frac{\kappa\beta\rho}{\Delta x} \end{bmatrix} \begin{bmatrix} j_1 \\ j_2 \end{bmatrix}.\quad (20)\end{aligned}$$

We notice that \mathbf{A} for the growth phase is not singular any more and no mitigation is required for growth phase analysis.

B. Fast Krylov Subspace-Based Stress Analysis

In this section, we present our Krylov subspace-based complexity reduction and simulation method, which is based on the similar principles in the traditional model order reduction methods [21], [22]. After the stress evolution, PDE has been

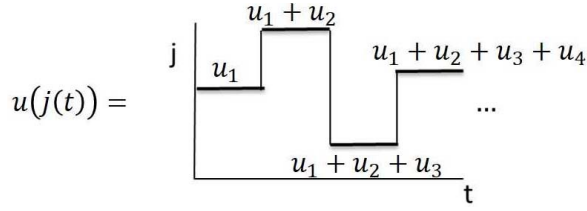


Fig. 5. Example piecewise constant current density \mathbf{j} input as a function of time t .

discretized into the ODE as shown in (4)–(6), it can be written into the following linear time-invariant (LTI) dynamic system:

$$\begin{aligned} \mathbf{C}\dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{j}(t), \\ \mathbf{x}(0) &= [x_1(0), x_2(0), \dots, x_n(0)] \end{aligned} \quad (21)$$

where the stress vector is represented by $\mathbf{x}(t)$, $\mathbf{x}(0)$ is the initial stress at $t = 0$ due to thermal-mechanical interaction. \mathbf{C} and \mathbf{A} are $n \times n$ matrices and \mathbf{B} is the $b \times p$ input matrix, where p is the number of inputs or the size of driving current density sources, $\mathbf{j}(t)$, which can be time-varying and is represented by the piecewise constant linear waveform as shown in Fig. 5. The piecewise constant linear input current density $\mathbf{j}(t)$ can be represented by

$$\mathbf{u}(t) = \mathbf{u}_1(t) + \mathbf{u}_2(t - t_1) + \mathbf{u}_3(t - t_2) + \dots + \mathbf{u}_N(t - t_{N-1}). \quad (22)$$

We transform the problem domain into the frequency domain using the Laplace transformation of the state equation (21), which can be rewritten as

$$s\mathbf{C}\mathbf{X}(s) - \mathbf{C}\mathbf{x}(0) = \mathbf{A}\mathbf{X}(s) + \frac{1}{s}\mathbf{B}\mathbf{J}_1 \quad (23)$$

where the Laplace transformation of $\mathbf{j}(t)$ is computed as

$$J(s) = \frac{1}{s} \left(\sum_{i=1}^N u_i e^{t_i-1} \right) = \frac{1}{s} J_1 \quad (24)$$

$$J_1 = \left(\sum_{i=1}^N u_i e^{t_i-1} \right). \quad (25)$$

It may be noted that in contrast to traditional model order reduction of the LTI systems, where the inputs are the impulse function, and we perform reduction on the transfer functions [23], here, the input is piecewise constant linear (or any arbitrary waveform represented by the piecewise linear function¹). As a result, we have to consider the input signal subspace during the reduction process. Essentially the reduction process is no longer the traditional model order reduction, but is just the reduction step for a given signal input and is the preprocess step of the whole simulation. Notice that the extended Krylov subspace (EKS) method has been previously proposed for fast power grid network analysis [24]. In this paper, we follow a similar idea, but we use a simple Arnoldi-like orthonormalization process to

¹For the EM-induced stress analysis, piecewise constant linear current density input is sufficient as most of the power models of a real chip can be modeled as a piecewise constant linear waveform.

Algorithm 1 Modified Arnoldi Method for Orthonormalization of Moment Space.

- 1: Modified Arnoldi process ()
 - 2: input: $(\mathbf{G}, \mathbf{b}, \mathbf{x}(0), q)$
 - 3: output: $(\mathbf{V}_q, \mathbf{H}_q)$
 - 4: $\mathbf{v}_1 = \mathbf{b} / \|\mathbf{b}\|_2$
 - 5: **for** ($j = 1; j \leq q; j++$) **do**
 - 6: **if** ($j == 1$) **then**
 - 7: $\mathbf{w} = \mathbf{G}(\mathbf{v}_j - \mathbf{x}(0))$
 - 8: **else**
 - 9: $\mathbf{w} = \mathbf{G}\mathbf{v}_j$
 - 10: **end if**
 - 11: **for** ($i = 1; i \leq j - 1; i++$) **do**
 - 12: $h_{i,j} = \mathbf{w}^T \mathbf{v}_i$
 - 13: $\mathbf{w} = \mathbf{w} - h_{i,j} \mathbf{v}_i$
 - 14: **end for**
 - 15: $h_{j+1,j} = \|\mathbf{w}\|_2$
 - 16: **if** ($h_{j+1,j} \neq 0$) **then**
 - 17: $\mathbf{v}_{j+1} = \mathbf{w} / h_{j+1,j}$
 - 18: **end if**
 - 19: **end for**
 - 20: $\mathbf{V}_q = [\mathbf{v}_1 \dots \mathbf{v}_q]$
 - 21: $\mathbf{H}_q = (h_{i,j}), i, j = 1, \dots, q$
-

compute the Krylov subspace of the response space instead of using the more complicated EKS method. Specifically, let $\tilde{\mathbf{X}}(s) = s\mathbf{X}(s)$, then the above equation becomes

$$s\mathbf{C}\tilde{\mathbf{X}}(s) - s\mathbf{C}\mathbf{x}(0) = \tilde{\mathbf{A}}\tilde{\mathbf{X}}(s) + \mathbf{B}\mathbf{J}_1. \quad (26)$$

We then expand the $\tilde{\mathbf{X}}(s)$ using Taylor's series at $s = 0$, to get

$$\begin{aligned} s\mathbf{C}(m_0 + m_1s + m_2s^2 + \dots) - s\mathbf{C}\mathbf{x}(0) \\ = \mathbf{A}(m_0 + m_1s + m_2s^2 + \dots) + \mathbf{B}\mathbf{J}_1. \end{aligned} \quad (27)$$

We then obtain the recursive response moment computation formula as follows:

$$\begin{aligned} \mathbf{m}_0 &= -\mathbf{A}^{-1}\mathbf{B}\mathbf{J}_1 \\ \mathbf{m}_1 &= \mathbf{A}^{-1}\mathbf{C}(\mathbf{m}_0 - \mathbf{x}(0)) \\ \mathbf{m}_2 &= \mathbf{A}^{-1}\mathbf{C}\mathbf{m}_1 \\ &\vdots \\ \mathbf{m}_{q-1} &= \mathbf{A}^{-1}\mathbf{C}\mathbf{m}_{q-2}. \end{aligned} \quad (28)$$

For the Krylov subspace method, instead of computing the raw moments as shown in (28), a modified Arnoldi process is used to compute the orthonormalized response moment space. We let $\mathbf{G} = \mathbf{A}^{-1}\mathbf{C}$ and $\mathbf{b} = -\mathbf{A}^{-1}\mathbf{B}\mathbf{J}_1$, and the modified Arnoldi process is shown in Algorithm 1.

We call this a modified Arnoldi process, as the computed space \mathbf{V}_q is not strictly a Krylov subspace which is defined as

$$K_q(\mathbf{G}, \mathbf{b}) = \text{span}(\mathbf{b}, \mathbf{G}\mathbf{b}, \mathbf{G}^2\mathbf{b}, \dots, \mathbf{G}^{q-1}\mathbf{b}). \quad (29)$$

However, due to lines 4 and 6–8 [23], our algorithm does not satisfy this. Instead, the subspace \mathbf{V}_q is the response signal space for $\tilde{\mathbf{X}}(s)$ as it considers the initial condition $\mathbf{x}(0)$ and the input signal vector $J(s)$. In this paper, we call it the

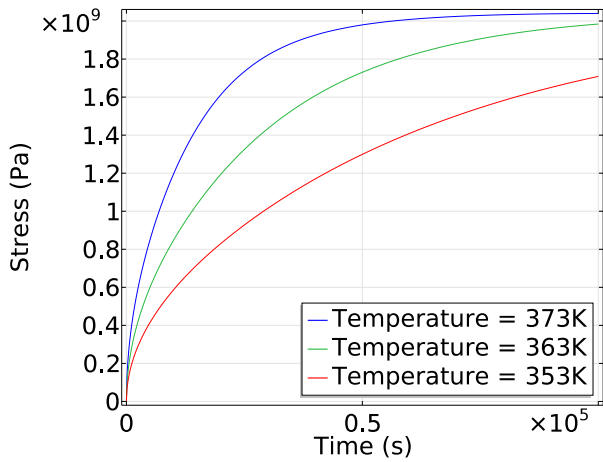


Fig. 6. Cathode stress over time for multiple wire temperatures.

response Krylov subspace. In our case, the signal space in the frequency domain only has the $(1/s)$ moment term, but in general, a piecewise linear input has nonzero component coefficients in all moments. Hence, lines 7 and 9 will be changed accordingly in this case. Due to the orthonormalization process in Algorithm 1, the moment computation process will become much more numerically stable than the raw moment computation as shown in (28).

Once we obtain the projection matrix \mathbf{V}_q , the original circuit matrix \mathbf{A} , \mathbf{C} , and \mathbf{B} , and initial stress $\mathbf{x}(0)$ in (21) can be order-reduced to the following matrices by the congruence transformation:

$$\hat{\mathbf{A}} = \mathbf{V}_q^T \mathbf{A} \mathbf{V}_q, \quad \hat{\mathbf{C}} = \mathbf{V}_q^T \mathbf{C} \mathbf{V}_q, \quad \hat{\mathbf{B}} = \mathbf{V}_q^T \mathbf{B}, \quad \text{and} \quad \hat{\mathbf{x}}(0) = \mathbf{V}_q^T \mathbf{x}(0)$$

where $\hat{\mathbf{A}}$ and $\hat{\mathbf{C}}$ are $q \times q$ matrices and $\hat{\mathbf{B}}$ is the reduced $q \times p$ input matrix. $\hat{\mathbf{x}}(0)$ is reduced initial condition $q \times 1$ vector. Then, the resulting reduced ODE LTI stress evolution system with the initial condition can be written as

$$\begin{aligned} \hat{\mathbf{C}} \dot{\hat{\mathbf{x}}}(t) &= \hat{\mathbf{A}} \hat{\mathbf{x}}(t) + \hat{\mathbf{B}} j(t) \\ \hat{\mathbf{x}}(0) &= [\hat{x}_1(0), \hat{x}_2(0), \dots, \hat{x}_q(0)]. \end{aligned} \quad (30)$$

Then, transient simulations in the time domain using backward-Euler time integration method can be performed on (30), which will be much more efficient to simulate than the original ODE LTI system in (21). After the reduced response is obtained $\hat{\mathbf{x}}(t)$, then, the original response can be obtained by $\mathbf{x}(t) = \mathbf{V}_q \hat{\mathbf{x}}(t)$.

C. EM Simulation Under Time-Varying Temperature

To accommodate the time-varying temperature impact on the stress evolution in the Korhonen equation (2), which can effectively accelerate or decelerate the stress build-up as shown in Fig. 6, we need to consider the time-varying diffusion parameter $\kappa(T)$ as it is a function of temperature T . As a result, the elements of matrix \mathbf{A} in the resulting LTI system in (10) will be a function of the temperature. As a result, the response Krylov subspace computation has to be carried out for each different temperature value, which will not be a viable solution in our case.

Fortunately, there is a better way to deal with this situation. Specifically, Let $\sigma_i(x, t, \kappa(T_1))$ and $\sigma_i(x, t, \kappa(T_2))$ ($i = 1, 2$) be the solutions to the stress evolution equation (10) with the diffusivities $\kappa(T_1)$ and $\kappa(T_2)$, due to different temperature T_1 and T_2 , for the same initial and boundary conditions, respectively. Let Δt be the time period, then, we can have following relationship [25], [26]:

$$\sigma_i(x, \Delta t, \kappa(T_2)) = \sigma_i\left(x, \frac{\kappa(T_2)}{\kappa(T_1)} \Delta t, \kappa(T_1)\right). \quad (31)$$

From (31), we can see that the temperature impact on the stress $\sigma(T, t)$ during the period Δt can be translated to the time period change for a metal wire. In other words, stress development in a metal wire over a period Δt under temperature T_2 will be equal to stress development for a metal wire over a period $(\kappa(T_2)/\kappa(T_1))\Delta T$ under temperature T_1 , where $\Delta T = T_2 - T_1$. As a result, we convert the temperature-varying stress computation problem into a constant temperature problem.

Going back to our problem, when we perform the time-domain stress simulation on the reduced model described in (30), a constant temperature T_0 is used for all the response Krylov subspace generation and reduction steps. Then, during the simulation, we first create a virtual i th time step τ_i

$$\tau_i = \sum_{i=1}^i \frac{\kappa(T_i)}{\kappa(T_0)} \Delta t_i \quad (32)$$

to perform the analysis under different temperatures T_i over the virtual time. However, the real time step for the simulated stress results are still $t_i = \sum_{i=1}^i \Delta t_i$.

D. Scaling Schemes for Numerical Stability

One important implementation issue is that the parameters used in the Korhonen equation can differ by a few orders of magnitude. As a result, direct application of modified Krylov subspace-based method on the resulting PDE may not be stable. This problem can be mitigated by parameter scaling. After the scaling, calculated stress and time should be scaled back to obtain the real stress condition and time information. In the following, we discuss two scaling schemes:

1) *Stress Scaling Scheme*: For the stress scaling, steady-state stress is used as a reference. As mentioned in (17), the steady-state stress is proportional to GL . The equation $G = (eZ\rho j/\Omega)$, in (2) is one of the dependents for the steady-state stress and is scaled to 1 when current density j is set to 5 MA/cm². In other words, $G_{\text{scale}} = j/j_0$ after scaling where $j_0 = 5$ MA/cm², and we can call the corresponding G value G_0 when $G_{\text{scale}} = 1$.

The scaled length of the branch is given by $L_{\text{scale}} = L/L_0$ where L_0 is 100 μm in our example case. After the scaled stress value σ_{scale} is calculated, the real stress $\sigma = \sigma_{\text{scale}} G_0 L_0$.

2) *Time Scaling Scheme*: The time scale is dependent on $(\kappa/\Delta x^2)$ as shown in (4). That is, time is proportional to $(\Delta x^2/\kappa)$. Δx is one segment of the branch and is scaled using the length L_0 , which means $\Delta x = \Delta x_{\text{scale}} L_0$. In addition, κ is scaled to 1 in our analysis, and the relationship between time and scaled time is $t = t_{\text{scale}} L_0^2/\kappa$.

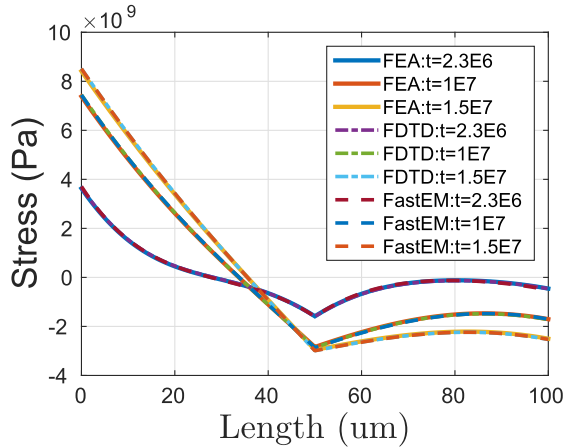


Fig. 7. Nucleation stage validation for two wire segments. *FastEM* solved using $q = 7$ with 0.0155% average error.

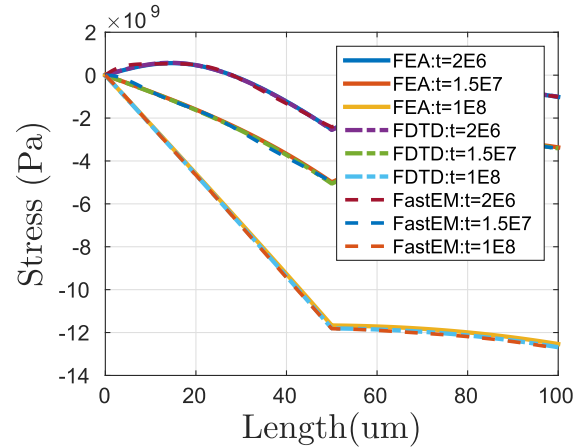


Fig. 8. Growth stage validation for two wire segments. *FastEM* solved using $q = 7$ with 0.0123% average error.

V. NUMERICAL RESULTS AND DISCUSSION

We have implemented the proposed *FastEM* method in MATLAB and this section presents the numerical results for accuracy of the proposed fast Krylov subspace-based EM analysis method and speed-up over the FDTD method, which was also implemented in MATLAB. The experiments were carried out on a Linux server with dual 3.3-GHz Xeon processors and 316-GB memory, with each processor having 2×22 cores (44 threads each). We want to stress that both *FastEM* and FDTD were implemented in MATLAB. As a result, their performance comparison based on the same numerical package and computing server is fair.

A. Accuracy Study

In our numerical analysis, a netlist for the interconnect tree is first discretized to form the LTI ODE system which is then used as input for the solver. In addition to constant current density, we also show the results from the piecewise constant current density inputs as well as simulation under dynamic temperature variations. To validate our proposed method, the two-segment case is simulated with the *FastEM* method and compared with the finite-element analysis (FEA) and the FDTD method proposed in [14]. This two-wire structure contains two $50\text{-}\mu\text{m}$ wire segments connected in series as presented in Section II. Each simulation is conducted using seven poles for reduction ($q = 7$). All FEA simulations are performed using COMSOL Multiphysics software using 2-D structures.

In Fig. 7, the nucleation stage stress under asymmetrical current density distribution ($1E10\text{ A/m}^2$ in segment 1 and $8E10\text{ A/m}^2$ in segment 2) for three time steps is shown. The results show agreement between all three methods with less than 0.02% error. We use the stress results from the nucleation phase to generate a critical stress profile (the stress in the wire when $\sigma(0, t) \leq 500\text{ MPa}$) which is then used as the initial condition for the growth phase simulation while also applying the same current density distribution. Validation of the three methods in the growth phase is shown in Fig. 8 for three

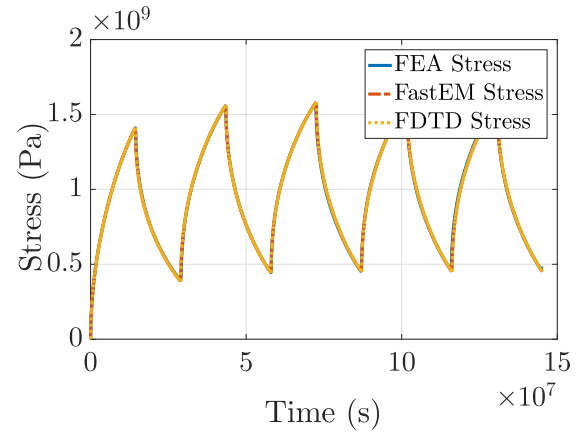


Fig. 9. Cathode stress comparison under piecewise constant current density input.

time steps. Again, the methods agree almost perfectly with negligible errors.

The results for both the nucleation and growth phases show good agreement with the other methods under constant asymmetric current density conditions, which validates our *FastEM* method. To validate the time-dependent current density handling, a periodic piecewise constant current density input, oscillating from $1E10$ to 0 A/m^2 , is applied and cathode stress during the nucleation phase is compared for the three methods and presented in Fig. 9. The three methods again agree with negligible error. Simulation results are also compared for the temperature-dependent modeling. Results show that both FDTD and *FastEM* agree with the COMSOL result using different temperatures during the simulation and are presented in Fig. 10.

B. Eigenvalue Analysis

The modified Krylov subspace-based method relies on the computation of several eigenvalues for reduction. To better understand how many poles q need to be computed in the *FastEM* method, we compute and plot the eigenvalues in Fig. 11.

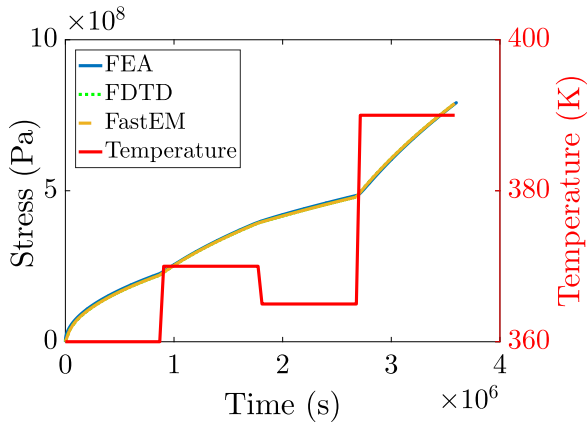


Fig. 10. Cathode stress under varying temperature $T = 360$ K, $T = 370$ K, $T = 365$ K, and $T = 390$ K.

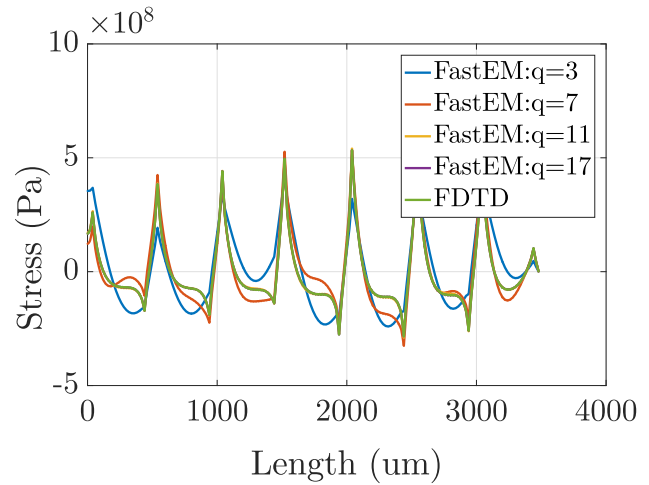
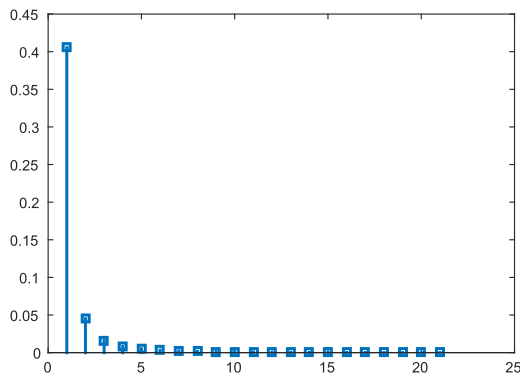
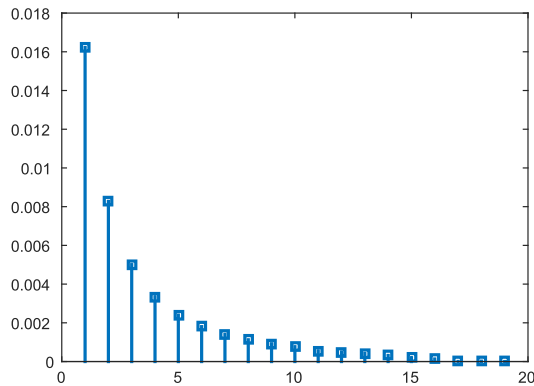


Fig. 12. Stress near nucleation time for 174-segment tree with different numbers of computed poles.



(a)



(b)

Fig. 11. Eigenvalue plot with (a) showing all eigenvalues and (b) without the two largest values.

In Fig. 11(a), we can see that the first Eigenvalue, the smallest pole of our system, determines the time constant of the system, and thus, the trend of the stress development. In addition, we see that only the first few Eigenvalues, and thus, poles have an effect on the system. Fig. 11(b) omits the first two Eigenvalues allowing us to better see the values that follow.

Additionally, the driving current and the structure of the tree being analyzed will also affect the number of poles needed.

In this paper, we use an ad-hoc method of determining the poles required by seeing how many dominant poles exist in our system. This type of analysis would need to be performed for each structure under test, however; we find that no more than 17 poles were ever needed for the trees that we tested in this paper.

For demonstration, we show the stress simulation for a large 174-segment tree with nonuniform current density distribution in Fig. 12, using different numbers of computed poles. Using 7 and 9 poles proves inaccurate as the large number of different current densities and segments require more poles for accurate simulation. However, the use of 11 and 17 poles leads to accurate results, with the 17 computed poles having less than 1% error.

C. Performance Analysis

To demonstrate the performance of our proposed method, we use both a real power grid benchmark and also arbitrary n -segmented trees. The International Business Machines Corporation (IBM) power grid benchmark *ibmpg3* structure [27] is first used for a realistic simulation using three different trees extracted from the *ibmpg3* benchmark. Second, we perform FDTD and *FastEM* simulations using increasingly large n -segmented trees in order to demonstrate the scalability of our method.

For the power-grid simulation, we choose a small tree (tree 1) with 58 segments, a medium-sized tree (tree 2) with 109 segments, and the largest tree (tree 3) with 174 segments for the simulation structures. Both methods discretize each branch in the trees into 21 nodes and compute the stress for 1000 time steps. The proposed method used 17 poles to compute each simulation. We perform the simulation with all 88 threads available and also while enforcing single-threaded computation. We do this to provide a better idea of the performance the simulation can achieve on various platforms as multithreaded computation performance will be system specific.

The results in Table II show the average computation time of the two methods using the three different *ibmpg3* trees.

TABLE I
PERFORMANCE COMPARISON BETWEEN FDTD AND *FastEM* METHODS FOR THREE DIFFERENT TREES
EXTRACTED FROM IBM POWER GRID BENCHMARK IBMPG2 USING MULTITHREADED EXECUTION
AND SINGLE-THREADED EXECUTION. RESULTS ARE AVERAGES OF EXECUTION TIMES

ibm Tree	FDTD (seconds)		<i>FastEM</i> (seconds)						Speed- up M.T.	Speed- up S.T.
	Single Thread	Multi- Thread	Single Thread			Multi-Thread				
			MOR	BE	Total	MOR	BE	Total		
tree1	16.985	14.670	0.1562	0.0312	0.1890	0.1530	0.0279	0.1809	90x	81x
tree2	63.727	53.914	0.6664	0.0345	0.7009	0.6512	0.0337	0.6849	90x	78x
tree3	185.224	150.963	1.8681	0.1960	1.9117	1.7437	0.0416	1.7575	97x	86x
M.T.: Multi-Thread, S.T.: Single Thread										

TABLE II
SCALABILITY PERFORMANCE RESULTS COMPARING FDTD AND *FastEM* USING INCREASINGLY LARGE N-SEGMENT TREES

n- segments	FDTD (seconds)	<i>FastEM</i> (seconds)			Speed-up
		MOR	BE	Total	
20	6.26	0.0354	0.0309	0.663	94.41x
50	8.613	0.0820	0.0233	0.1053	81.79x
100	37.445	0.4058	0.0203	0.4261	87.87x
200	205.504	2.5983	0.0335	2.6318	78.08x
400	1519.715	20.2112	0.0407	20.2519	75.04x
500	2376.478	34.0633	0.0481	34.1114	69.66x
750	7609.128	107.6036	0.0501	107.6537	70.68x
1000	15354	252.8880	0.0958	252.9838	60.69x
1250	28840	460.5587	0.1167	460.6754	62.60x
1500	52096	791.4289	0.1372	791.5661	65.81x
1750	80542	1240.455	0.1451	1240.455	64.92x
2000	110810	1815.1380	0.1624	1815.3	61.04x
3000	363660	6023.0290	0.1711	6022.3	60.37x
4000	8.61E5	14236.81	0.01876	14237	60.45x
5000	1.7339E6	27729.8	0.1951	27730	62.52x

The results show significant speed up of over 90x and reaching close to 100x. We can also see from this table that the *FastEM* method is broken down into the time for the model order reduction (MOR) algorithm, the backward-Euler solver (BE), and the total time.

The results show that the MOR portion of the proposed method dominates the computation time while the backward-Euler solver takes much less time. We remark that MOR is dependent on the size of the input system and the number of poles used for model reduction while BE is dependent on both. However, because we perform MOR, the input to BE will always be a matrix of $q \times q$ where q is the number of poles. Since we have set the number of poles to 17 in this test, the BE computation time will remain about constant with only negligible increases in duration due to congruence transformations at the beginning and the end of BE. Furthermore, we compute mean errors of 0.0678%, 0.0251%, and 0.0362% for test trees 1, 2, and 3, respectively. As a result, the error caused by the reduction is basically negligible when compared to the FDTD method.

In addition to the benchmark test, performance scalability is studied by simulating increasingly larger n-segmented trees. Each tree is a straight wire, with n segments. Each segment is discretized into 11 nodes, and *FastEM* is computed

with 17 poles. We can see from Table I that *FastEM* maintains the performance improvement even with very large systems achieving a 60–94x performance increase over FDTD. We also observe that as the number of segments increases, performance gain converges to around 60x.

VI. CONCLUSION

In this paper, we have proposed a novel fast numerical approach to solve the PDEs for EM-induced stress evolution in confined copper interconnect wires based on the Krylov subspace method. The new method, *FastEM*, first discretizes the PDE into linear time-invariant ODE. Then, we applied a modified Krylov subspace-based reduction technique in the frequency domain to reduce the original system matrices into smaller ones so that they can be simulated very efficiently in the time domain. *FastEM* can perform reduction and simulation process for both void nucleation and void growth phases under piecewise constant linear current density inputs and time-varying stressing temperatures, which represents the typical chip working conditions. Furthermore, we showed through two examples that the steady-state response of stress diffusion equations can be obtained from the resulting ODE system in the frequency domain, which agrees with the recently

proposed voltage-based EM analysis method for EM immortality check. When compared to the existing FDTD-based method, numerical results showed that *FastEM* can achieve a 60–100x performance gain on large interconnect trees for both void nucleation and growth phases with negligible errors. We further showed that we only need a small number of poles for sufficient accuracy for large interconnect trees.

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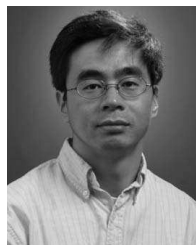
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