EM-Aware and Lifetime-Constrained Optimization for Multisegment Power Grid Networks

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***Abstract*— This paper proposes a new power–ground (P/G) network sizing technique based on the recently proposed fast electromigration (EM) immortality check method for general multisegment interconnect wires and a new physics-based EM assessment technique for more accurate time to failure analysis. This paper first shows that the new P/G optimization problem, subject to the voltage IR drop and new EM constraints, can still be formulated as an efficient sequence of linear programing problem, where the optimization is carried out in two linear programing phases in each iteration. The new optimization will ensure that none of the wires fail if all the constraints are satisfied. However, requiring all the wires to be EM immortal can be overconstrained. To mitigate this problem, the first improvement is by means of adding reservoir branches to the mortal wires whose lifetime cannot be made immortal by wire sizing. This is a very effective approach as long as there is a sufficient reservoir area. The second improvement is to consider the aging effects of interconnect wires in the P/G networks. The idea is to allow some short-lifetime wires to fail and optimize the rest of the wires while considering the additional resistance caused by the failed wire segments. In this way, the resulting P/G networks can be optimized, such that the target lifetime of the whole P/G networks can be ensured and will become more robust and aging-aware over the expected lifetime of the chip. Numerical results on a number of IBM and self-generated power supply networks demonstrate that the new method can effectively reduce the area of the networks while ensuring immortality or enforcing target lifetime for all the wires, which is not the case for the existing current-density-constrained optimization methods.**

***Index Terms*— Electromigratiion, integrated circuit reliability, interconnections, on-chip power grid networks.**

I. Introduction

ON-CHIP power supply or power–ground (P/G) networks provide power to the circuit modules in a chip from the external power supplies. Fig. 1 shows a typical mesh-structured P/G network with multilayer power grids. Since power grid wires experience the largest current flows on a chip, they are more susceptible to long-term reliability issues and functional failures. These reliability issues and failures typically come from metal electromigration (EM), excessive IR drops, and ΔI (Ldi/dt) noise along with the recently emerging back-end-of-line time-dependent dielectric breakdown [2]–[5].

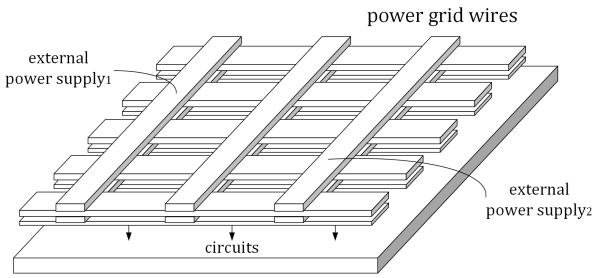

Fig. 1. Small portion of a typical power supply network [7].

As technology scales into smaller features with increasing current densities, EM-induced reliability deteriorates (the EM lifetime was projected to be reduced by half for each new technology node by ITRS 2015 [6]). As a result, EM still remains one of the top killers of copper-based damascene interconnects in 10 nm and beyond technologies. This introduces additional challenges for designing robust power supply networks to satisfy the demanding design requirements.

An important step for power supply synthesis in the typical EDA design flow is to size the wire width of the power grid stripes, after the topology of the power supply network has been determined, so that the minimum amount of chip area will be used while avoiding potential reliability failures due to electromigration and excessive IR drops. Numerous works have been proposed for the power supply network optimization in the past, primarily based on the nonlinear or sequence of linear programing (SLP) methods [8]–[14]. To satisfy the EM reliability, all the existing methods use the current density of individual wires as the constraint, which is mainly based on the Black's EM model [2]. However, recent studies show that the time-to-failure (TTF) predicted by the Black's EM model is too conservative, and thus, more accurate physics-based EM models have been proposed [15], [16]. More importantly, practical VLSI interconnects (especially the global networks such

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Fig. 2. Example of a multisegment wire.

as power supply and clock networks) have many multisegment wires, as shown in Fig. 2. A multisegment interconnect wire consists of continuously connected high-conductivity metal within one layer of metallization.

The study and experimental data show that the current-induced stress developed in those segments is not independent [17], [18]. In other words, if we just look at the current density for each segment individually, it may appear as if all wire segments are immortal, but the whole interconnect tree could still be mortal. The reason is that the stress in one segment of an interconnect tree depends on other segments, which are not independent [19]. This issue has been resolved by the recently proposed fast EM immortality check method for the general multisegment interconnect wires [20]. Here, the immortality is determined by checking all the segments, which is nicely represented by the so-called *EM voltage*. Immortality can be determined by comparing the *EM voltage* against the *critical EM voltage*. However, this new multisegment EM immortality check has not been further applied to optimize the P/G networks, which is one of the focuses of this paper.

Furthermore, all the existing power supply optimization methods mainly consider wire sizing, which impacts the lifetime of wires, without considering other more effective optimizing knobs (i.e., adding or relocating reservoirs or sinks which belong to multisegment interconnect wires). These methods also need more complicated physics-based EM models or numerical analysis methods to estimate the TTF. With recent advancements in the physics-based EM models and numerical analysis techniques such as three-phase EM models [19], [21]–[23], it is possible to provide more accurate TTF estimation for multisegment interconnects.

Another important issue with the existing P/G network optimization methods is that they fail to consider the aging effects. In other words, they can hardly optimize a P/G network at the target lifetime when some wires are nucleated and even fail completely (with open circuit) while the whole P/G network may still work. The difficulty for such optimization lies in the need for very accurate TTF and transient wire resistance change estimation methods, which become possible with the recent advanced physics-based EM models and numerical analysis techniques.

In this paper, we mitigate the above-discussed difficulties and propose a new P/G network sizing technique based on the recently proposed voltage-based EM immortality check method for general multisegment interconnect wires and the recently proposed physics-based EM assessment technique for fast TTF analysis. Our contribution lies in the following.

1) First, we show that the new P/G network optimization problem subject to the voltage IR drop and new EM constraints can still be formulated as an efficient SLP problem [12], where the optimization was carried out in two linear programing phases in each iteration. The new optimization ensures that none of the EM wires fail as long as all the constraints are satisfied.
2) To mitigate the overconservation of the first optimization formulation in which all the wires are required to be immortal, we propose to insert proper reservoirs. The newly inserted reservoirs are small zero-current wire segments added to the interconnect trees that are likely to fail. Then, we perform the immortality-constrained P/G network optimization. This method essentially trades off chip area for robustness.
3) The second method to mitigate the overconservation is by means of considering the aging effects of interconnects at the target lifetime. Specifically, the new method allows a part of short-lifetime wires to fail but optimize the rest of the wires in the presence of wire resistance increase in the second optimization formulation. In this way, the original P/G networks can be optimized, and the resulting networks become more robust and aging-aware over the lifetime of the chip.
4) Numerical results on a number of IBM and self-generated power supply networks demonstrate that the new method can effectively reduce the area of the networks while ensuring immortality or enforcing target lifetime for all the wires, which is not possible with the existing current-density-constrained optimization methods.

The preliminary results of this work have been published in [1]. This paper is organized as follows. Section II reviews the recently proposed EM model and the fast EM lifetime estimation method used in this paper. Section III introduces our EM immortality-constrained P/G network optimization problem and its programing-based solution. Section IV discusses the impact of reservoirs and the EM immortality-constrained P/G network optimization with reservoir insertion. Section V presents our EM lifetime-constrained P/G optimization method, which considers the EM-induced aging effect. Experimental results on some P/G networks and the comparison with the current-density-constrained method are summarized in Section VI. Section VII concludes this paper.

II. Review of Electromigration Fundamentals and Existing Models

EM is a major reliability concern for interconnect wires with increasing current densities and advanced technology nodes. It is a physical phenomenon of material migration caused by an electrical field. Wind force, which is produced by the current flowing through a conductor, acts in the direction of the current flow and is the primary cause of EM [24]. During the migration process, hydrostatic stress is generated inside the embedded metal wire due to momentum transfer between lattice atoms. Void and hillock formation are caused by conducting electrons at the opposite ends of the wire. The void can cause either early failure or late failure of the wire [25]. Early failure typically happens in a via-to-via structure, as shown in Fig. 3(a). When the void forms in a via-above line and reaches critical size [26], [27], which equals the via's diameter, the via will be blocked by the void, and thus,

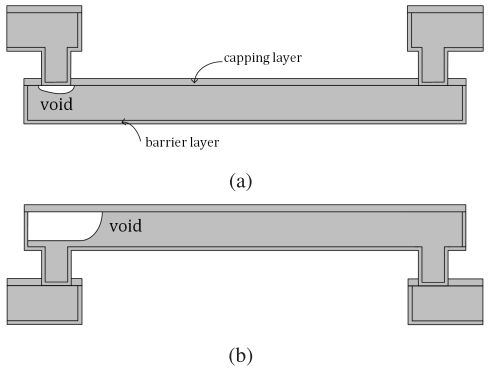

Fig. 3. Side view of void formation. (a) Void in a via-above line (early failure mode). (b) Void in a via-below line (later failure mode).

the connection to the upper layer will also be blocked (capping layer is fabricated with dielectrics, such as Si_3N_4, which does not shunt current flow). Late failure typically happens in the so-called via-below structure, as shown in Fig. 3(b). When the void forms in a via-below line and reaches a critical size, current can still go through the barrier layer (barrier layer is fabricated with Ta whose resistivity is much higher than Cu), and the resistance will increase over time. Sometimes, early failure can happen in a via-below structure, and the late failure can happen in a via-above structure. Although the void can grow at these positions, the possibility is very low.

In order to mitigate this problem, many physics-based models were developed in the past. Some models focus on an immortality analysis. These methods ensure that the steady-state stress, which is the maximum stress the nodes experience, does not exceed the critical stress so that the void would never nucleate. We call these kinds of models the steady-state EM-induced stress models. Other models focus on TTF where the transient analysis based on partial differential equations (PDE) is applied and three phases, including the nucleation phase, incubation phase, and growth phase, are considered. If the estimated TTF is longer than the constraint, the wire is acceptable. Otherwise, the optimization methods should be employed in order to meet the EM constraint. Some details of the steady-state stress models and the transient stress models are reviewed in Section II-A.

A. Steady-State EM-Induced Stress Modeling

Steady-state EM-induced stress modeling helps to find the immortality information of the interconnect wire quickly, as no complex calculations are required. For these kinds of models, stress on the cathode at steady state (σ_{steady}) is compared with critical stress (σ_{crit}). If σ_{steady} is lower than σ_{crit}, the wire is considered as immortal. One of the well-known steady-state analysis methods is *Blech product* [28], but it is only suitable for a single (one-segment) wire. Recently, a voltage-based EM immortality analysis method for multisegment interconnect structures has been proposed [20], [22]. In this method, an *EM voltage* (V_E) which is proportional to stress at the ground node

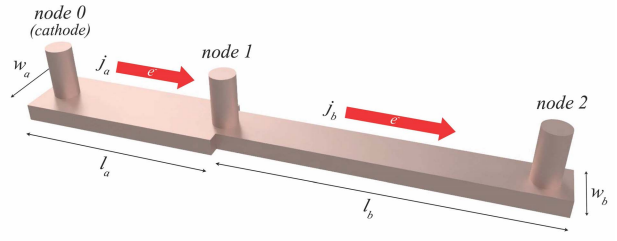

Fig. 4. Interconnect example of the EM analysis for a straight three-terminal wire.

(σ_g) is calculated as

$$V_E = \frac{1}{2A}\sum_{k\neq g} a_k V_k \tag{1}$$

where V_k is the normal nodal voltage (with respect to cathode node g) at node k, a_k is the total area of branches connected to node k, and A is the total area of the wire. With the voltage of node i (V_i), steady-state stress at that node (σ_i) can be calculated as $\sigma_i = \beta(V_E - V_i)$, where $\beta = (eZ/\Omega)$, e is the elementary charge, Z is the effective charge number, and Ω is the atomic lattice volume. A *critical EM voltage* $V_{\text{crit,EM}}$ is defined by

$$V_{\text{crit,EM}} = \frac{1}{\beta}(\sigma_{\text{crit}} - \sigma_{\text{init}}) \tag{2}$$

where σ_{init} is the initial stress. In order to check whether the interconnect wire is immortal or not, we need to check the following condition:

$$V_{\text{crit,EM}} > V_E - V_i. \tag{3}$$

If this condition is met for all the nodes, EM failure will not happen. Since, generally, the cathode node has the lowest voltage within an interconnect wire, we may just check the cathode node instead of all the nodes, which means

$$V_{\text{crit,EM}} > V_E - V_{\text{cat}} \tag{4}$$

where V_{cat} is the voltage at the cathode. Note that (4) can be applied to both the power and ground networks.

The method can be illustrated using the following example. Fig. 4 shows a three-terminal wire. In this wire, node 0 is treated as the ground node. Current densities in two segments are j_a and j_b, which may not be the same because they will be determined by the rest of the circuit. The EM stress equations become

$$\begin{aligned} &V_0 = 0, \quad a_0 = l_a w_a, \sigma_0 = \beta V_E \\ &V_1 = j_a l_a \rho, \quad a_1 = l_a w_a + l_b w_b, \ \sigma_1 = \beta(V_E - V_1) \\ &V_2 = j_b l_b \rho + j_a l_a \rho, \ a_2 = l_b w_b, \ \sigma_2 = \beta(V_E - V_2). \end{aligned} \tag{5}$$

Then, the *EM voltage* can be obtained easily

$$V_E = \frac{a_0 V_0 + a_1 V_1 + a_2 V_2}{2A} = \frac{a_1 V_1 + a_2 V_2}{2A} \tag{6}$$

where

$$A = \frac{a_0 + a_1 + a_2}{2}. \tag{7}$$

We can compare V_E and $V_{\text{crit,EM}}$ to see if this wire is immortal.

B. Transient EM-Induced Stress Estimation

Sometimes, the steady-state methods are overly conservative, and therefore, more complete models of transient hydrostatic stress evolution are needed. In general, the failure process is divided into the nucleation phase, the incubation phase, and the growth phase. In the nucleation phase, the stress at the cathode increases. When it reaches critical stress, a void will be nucleated. The time to reach the critical stress is called nucleation time (t_{nuc}). After the nucleation phase, the void starts to grow (t_{inc}) and eventually leads to wire failure after a period of time (t_{growth}). The TTF or the lifetime of the wire can be described as

$$\text{TTF} = t_{\text{life}} = t_{\text{nuc}} + t_{\text{inc}} + t_{\text{growth}}. \tag{8}$$

We will discuss how to compute t_{nuc}, t_{inc}, and t_{growth} next.

1) Nucleation Phase Modeling: It is well known that the nucleation phase was accurately modeled by Korhonen's equation [29]

$$\frac{\partial \sigma(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma(x,t)}{\partial x} + \Gamma\right)\right] \tag{9}$$

where $\kappa = (D_a B\Omega/k_B T)$, $D_a = D_0 \exp(-(E_a/k_B T))$, and $\Gamma = (eZ/\Omega)\rho j$. B is the effective bulk elasticity modulus, Ω is the atomic lattice volume, k_B is Boltzmann's constant, T is the temperature, Z is the effective charge number, x is the coordinate along the line, t is the time, and j is the current density.

Korhonen's equation describes the stress distribution accurately, and this PDE-based model is hard to solve directly using the numerical methods and has very low efficiency for tree-based EM assessment analysis. Recently, a few numerical methods have been proposed, such as the finite difference methods [30], [31] and analytical-expressions-based approaches [32], [33]. In this paper, an integral transformation method for straight multisegment wires [33] is employed. Suppose we have n segments in a multisegment wire, as shown Fig. 2. After discretizing Korhonen's equation, the stress can be expressed as

$$\sigma(x,t) = \sum_{m=1}^{\infty} \frac{\psi_m(x)}{N(\lambda_m)} \bar{\sigma}(\lambda_m, t) \tag{10}$$

where the norm of eigenfunctions $N(\lambda_m)$ is

$$N(\lambda_m) = \int_{\chi=0}^{L} [\psi_m(\chi)]^2 d\chi \tag{11}$$

and $\bar{\sigma}(\lambda_m, t)$ is the transformed solution of stress, which is

$$\bar{\sigma}(\lambda_m, t) = \bar{F}(\lambda_m) e^{-\kappa\lambda_m^2 t} + \frac{1}{\lambda_m^2}(1 - e^{\kappa\lambda_m^2 t}) \cdot \sum_{k=1}^{n} \Gamma_k \cdot \left(\cos\frac{x_{k-1}}{L} m\pi - \cos\frac{x_k}{L} m\pi\right) \tag{12}$$

where F is

$$\bar{F}(\lambda_m) = \int_{\chi=0}^{L} \psi_m(\chi) \cdot \sigma_0(\chi) d\chi \tag{13}$$

λ_m and $\psi(x)$ are the eigenvalues and eigenfunctions, which are the solutions of the Sturm–Liouville problem corresponding to the diffusion equation (9) and the boundary conditions

$$\lambda_m = \frac{m\pi}{L}, \quad \psi_m(x) = \cos\frac{x}{L} m\pi \tag{14}$$

where $m = 1, 2, \cdots, \infty$. Γ_k is

$$\Gamma_k = \frac{eZ\rho}{\Omega} j_k, \quad k = 0, 1, \ldots, n. \tag{15}$$

With (10), given critical stress σ_{crit}, the nucleation time t_{nuc} can be obtained quickly by using the nonlinear equation solving methods, such as Newton's method or bisection method.

We remark that when the compressive stress at the anode continues to be built up, hillocks or extrusion may be formed, which will lead to a resistance decrease [34] and can potentially cause short-circuit failure. However, the void nucleation is still the dominant EM failure effect [35]. In this paper, we only focus on the void-induced EM failure.

2) Incubation Phase Modeling: After the void is nucleated, the incubation phase starts. In this phase, the resistance of the interconnect remains almost unchanged since the cross section of the via is not covered by the void and the current can still flow through the copper.

In power grid networks, the interconnect trees are generally multisegment wires. All segments connected with the void can contribute to the void growth since electron wind at each segment can accelerate or slow down the void growth based on their directions. In this phase, void growth rate v_d is estimated to be [36]

$$v_d = \frac{D_a eZ\rho}{kTW_m} \sum_i j_i W_i \tag{16}$$

where j_i and W_i are the current density and width of the ith segment, respectively. W_m is the width of the main segment where the void is formed.

Then, the incubation time (t_{inc}) can be expressed as

$$t_{\text{inc}} = \frac{\Delta L_{\text{crit}}}{v_d} \tag{17}$$

where ΔL_{crit} is the *critical void length*.

3) Growth Phase Modeling: After the incubation phase, the void fully covers the via, initiating the growth phase. In this phase, the resistance starts increasing. It is important to note that early failure and late failure have different failure mechanisms.

For early failure, the wire fails once the void covers the via, which means that the wire fails at the end of the incubation phase and there is no growth phase ($t_{\text{growth}} = 0$). Hence, the failure time is the sum of t_{nuc} and t_{inc}.

For late failure, as shown in Fig. 3(b), after the void size reaches the critical size, there will be no open circuit since the current can still flow through the barrier layer. In this case, the void growth will lead to a resistance increase. When the resistance increases to the critical level, the interconnect wire is considered to be failed. The time period between the void covering the via and wire failure is called growth time.

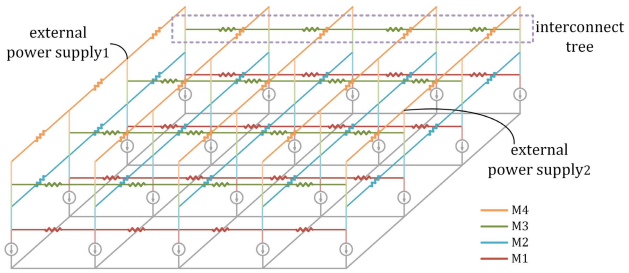

Fig. 5. Equivalent circuit of a small portion of a typical power grid.

The growth time for late failure is

$$t_{\text{growth}} = \frac{\Delta r(t)}{v_d \left[\dfrac{\rho_{Ta}}{h_{Ta}(2H+W)} - \dfrac{\rho_{Cu}}{HW} \right]} \tag{18}$$

where ρ_{Ta} and ρ_{Cu} are the resistivities of tantalum (the barrier liner material) and copper, respectively, W is the line width, H is the copper thickness, and h_{Ta} is the liner layer thickness.

However, the void may saturate before reaching the *critical void length*. The saturation length is expressed in [16] as

$$L_{ss} = L_{\text{line}} \times \left[\frac{\sigma_T}{B} + \frac{eZ\rho j L}{2B\Omega} \right] \tag{19}$$

where L_{ss} is the void saturated length, L_{line} is the total length of the wire, and σ_T is the thermal stress. Void growth may stop before the calculated t_{growth} value because the void is saturated. In this case, we can treat the wire as immortal or its lifetime is larger than the target lifetime.

III. EM Immortality-Constrained Optimization for Multisegment Interconnects

In this section, we propose the EM immortality-constrained power grid wire sizing optimization method considering the multisegment interconnect wires. We notice that the new EM constraint will ensure that all the wires are EM immortal, so we call this method EM immortal power supply optimization (we will discuss the EM mortal optimization later).

Before optimization, we first describe the modeling assumptions for this paper. First, we focus on the dc problem, which means that we are only interested in the resistance of the power grid networks. The transient behavior of the P/G networks will be addressed with decoupling capacitor allocation and other optimization techniques, which are out of the scope of this paper. Second, the P/G network is composed of an orthogonal mesh of wires and contains multiple segments/branches, which are typical P/G structures. Finally, to simplify the problem, the circuits are modeled with shorted vias, which means that the via resistance is ignored and vias will not be sized. Fig. 5 shows the equivalent circuit of the power grid network in Fig. 1.

A. Problem Formulation

Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, \ldots, n\}$ and b branches $B = \{1, \ldots, b\}$. Each branch i in B connects two nodes i_1 and i_2 with current flowing from i_1 to i_2. l_i and w_i are the length and width of branch i, respectively. ρ is the sheet resistivity. The resistance r_i of branch i is

$$r_i = \frac{V_{i_1} - V_{i_2}}{I_i} = \rho \frac{l_i}{w_i}. \tag{20}$$

1) Objective Function: We can express the total routing area of a power grid network in terms of voltages, currents, and lengths of branches as follows:

$$f(V, I) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i1} - V_{i2}}. \tag{21}$$

We notice that the objective function is linear for branch current variables $\mathbf{I}$ and nonlinear for node voltage variables $\mathbf{V}$.

The EM immortality-constrained optimization in the objective function (21) does not depend on temperature. In other words, the immortality condition of a wire is temperature-independent. But if a wire will fail, the nucleation time will depend on the temperature, which will be addressed by the lifetime-constrained optimization shown later.

2) Constraints: The constraints that need to be satisfied for a reliable, working P/G network are shown as follows.

a) Voltage IR drop constraints: In order to ensure proper logic operation, the IR drop from the P/G pads to the nodes should be restricted. For each node, we must specify a threshold voltage

$$V_j > V_{\min} \text{ for power network.} \tag{22}$$

In the modern high-performance processor design, usually 10% or so of the overall wiring resources on all wiring levels are dedicated to power delivery.

b) Minimum width constraints: The widths of the P/G segments are technologically limited to the minimum width allowed for the layer where the segment lies in. Thus, we have

$$w_i = \rho \frac{l_i I_i}{V_{i1} - V_{i2}} \geq w_{i,\min}. \tag{23}$$

c) New electromigration constraints for multisegment interconnects: As described before, for a multisegment interconnect m, the EM constraint should be satisfied

$$V_{\text{crit,EM}} > V_{E,m} - V_{\text{cat},m} \tag{24}$$

where $V_{E,m}$ is the *EM voltage* for the mth interconnect tree, which is computed using (1). $V_{\text{cat},m}$ is the cathode nodal voltage of that tree. Unlike the previous methods whose branch currents are monitored and used as constants, in our new method, voltages are used as constraints. Only the cathode node voltage for a whole interconnect tree needs to be monitored, and no other complex calculations are required.

d) Equal width constraints: For typical chip layout designs, certain tree branches should have the same width. The constraint can be written as $w_i = w_k$. In terms of nodal voltages and branch currents, we have

$$\frac{V_{i1} - V_{i2}}{l_i I_i} = \frac{V_{k1} - V_{k2}}{l_k I_k}. \tag{25}$$

e) Kirchhoff's current law: For each node j, we have

$$\sum_{k\in B(j)} I_k = 0 \tag{26}$$

where $B(j)$ is the set of branches incident on node j.

The power grid optimization aims to minimize the objective function (21) subjected to constraints (22)–(26). It will be referred as problem *P*. Problem *P* is a constrained nonlinear optimization problem.

B. Relaxed Two-Step Sequence of Linear Programing Solution

In the aforementioned constrained nonlinear optimization problem, we notice that the newly added EM constraint (24) is still linear in terms of nodal voltage. As a result, we can follow the relaxed two-phase iterative optimization process [10], [12] and apply the SLP technique [12] to solve the relaxed problem in each phase. Specifically, we have two phases: the voltage solving phase (*P-V* phase) and the current solving phase (*P-I* phase).

1) P-V Optimization Phase: In this phase, we assume that all branch currents are fixed, and then, the objective function can be rewritten as

$$f(V) = \sum_{i\in B} \frac{\alpha_i}{V_{i1} - V_{i2}} \tag{27}$$

where $\alpha_i = \rho I_i l_i^2$, subject to constraints (22), (24), and (25). We further restrict the changes of nodal voltages, such that their current directions do not change during the optimization process

$$\frac{V_{i1} - V_{i2}}{I_i} \geq 0. \tag{28}$$

Problem *P-V* is nonlinear; however, it can be converted to an SLP problem [12]. By taking the first-order Taylor's expansion of (27) around the initial solution V^0, the linearized objective function can be written as

$$g(V) = \sum_{i\in B} \frac{2\alpha_i}{V_{i1}^0 - V_{i2}^0} - \sum_{i\in B} \frac{\alpha_i}{\left(V_{i1}^0 - V_{i2}^0\right)^2}(V_{i1} - V_{i2}). \tag{29}$$

Besides, an additional constraint will be added [12]

$$\xi \text{sign}(I_i)\left(V_{i1}^0 - V_{i2}^0\right) \leq \text{sign}((I_i)(V_{i1} - V_{i2}) \tag{30}$$

where $\xi \in (0, 1)$ is a restriction factor, which will be selected by some trials and experience, and $\text{sign}(x)$ is the sign function.

2) P-I Optimization Phase: In this phase, we assume that all nodal voltages are fixed, so the objective function becomes

$$f(I) = \sum_{i\in B} \beta_i I_i \tag{31}$$

where $\beta_i = (\rho l_i^2 / V_{i1} - V_{i2})$, subject to constraints (23), (25), and (26). Similarly, we restrict the changes of current directions during the optimization process

$$\frac{I_i}{V_{i1} - V_{i2}} \geq 0. \tag{32}$$

As can be seen, problem *P-I* is a linear programing problem.

Algorithm 1 New EM Immortality-Constrained P/G Wire Sizing Algorithm

Input: Spice netlist G_I containing a P/G network.
Output: Optimized P/G network parameters.

```
/*Problem Setup*/
k := 0.
Compute the initial V^k, I^k from G_I.
repeat
    /*P-V Phase*/
    Construct constraints (24), (25), (28) and (30) with I^k.
    m := 1.
    Compute V_m^k := arg min g(V^k) subject to constraints
    (22), (24), (25), (28) and (30).
    while f(V_m^k) > f(V_{m-1}^k) do
        Determine the direction d := V_{m-1}^k - V_m^k.
        Line search. Use golden section method to find α.
        V_{m+1}^k := V_m^k + αd.
        m := m + 1.
    end while
    V^{k+1} := V_m^k.
    /*P-I Phase*/
    Construct constraints (23), (25) and (32) with V^{k+1}.
    Compute I^{k+1} := arg min f(I^k) subject to (23), (25),
    (26), and (32) constraints.
    k := k + 1.
until |f(V^k, I^k) - f(V^{k-1}, I^{k-1})| < ε
Return f(V, I).
```

C. New EM Immortality-Constrained P/G Optimization

The new EM immortality-constrained P/G optimization starts with an initial feasible solution. We iteratively solve *P-V* and *P-I*. The procedure for solving problem in *P-V* phase can be transformed to the problem of choosing ξ and solving a linear programing problem, and then repeating this process until the optimal solution is found. We summarize the entire EM immortality-constrained power grid network optimization procedure as Algorithm 1.

In practice, only a few linear programings are needed to reach the optimum solution. Thus, the time complexity of our method is proportional to the complexity of linear programing. It is known that the linear programs can be solved in polynomial time using the interior point method [12], [37], which will be represented as $f_{\text{SLP}}(n, b)$ from now where n and b are the number of nodes and number of branches, respectively, in the given P/G network.

We remark that in Algorithm 1, the nodal voltages and branch currents will not change dramatically from one iteration to another for a similar value of the objective function (21). The reason is that the branch voltages and node voltages are uniquely related in the power and ground networks where the reference voltages are given. If the voltage difference (branch voltage) for a wire will not change dramatically from one iteration to another during the optimization, which typically is the case for the late stages of P-V optimization, then the nodal voltages will not change dramatically as well. Moreover, the nodal voltages will be uniquely determined by those branch

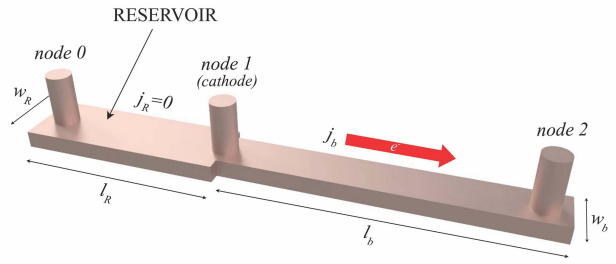

Fig. 6. Three-dimensional view of a two-segment wire with a reservoir.

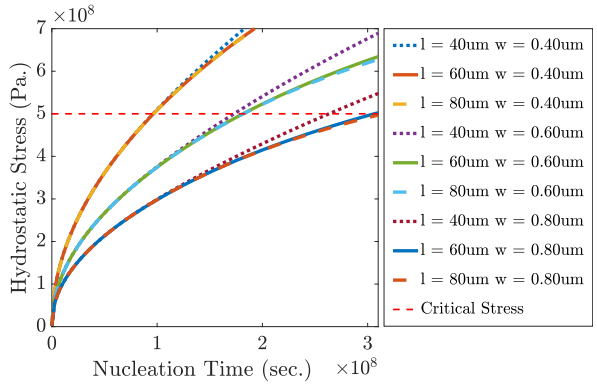

Fig. 7. Impact of length and width of the reservoir on the TTF of a wire.

and reference voltages. This is also true for the P-I phase, as the branch current solution needs to satisfy the Kirchhoff's current law first. On top of this, if the branch voltages do not change too much in the P-V phase based on the previous analysis, the branch currents will not change significantly as well for a similar value of the objective function.

IV. EM Immortality-Constrained P/G Wire Sizing With Reservoir Insertion

As mentioned earlier, EM immortality requirement for all the interconnect trees can be overconstrained. This happens when the initial P/G grids are designed so that we may not be able to find a solution from the wire sizing method in Algorithm 1. To mitigate the problem, we propose a novel reservoir insertion-based method.

The reservoir is a zero-current metal segment added to the cathode of a metal wire so that the wire's lifetime can be increased. Fig. 6 shows a two-segment wire in which the left segment is a reservoir. Adding a reservoir branch will reduce the steady-state tensile stress of the cathode node, which may make the mortal wire immortal. In other words, it can significantly increase the lifetime of the wire. The area of the reservoir will determine the final steady-state stress at the cathode node. Fig. 7 shows how the different widths and lengths of the reservoir will affect the TTF of the reservoir-enabled wires. As we can see, increasing the length or width of the reservoir will benefit the lifetime. Doubling the length increases nucleation time by around 13.7%, while doubling the width increases nucleation time by 89.5%.

With impact on TTF shown in Fig. 7, we can adjust the width or length of a reservoir to change the lifetime of the wire. However, there will be an opposite impact on the lifetime when a zero-current wire is added to the anode.

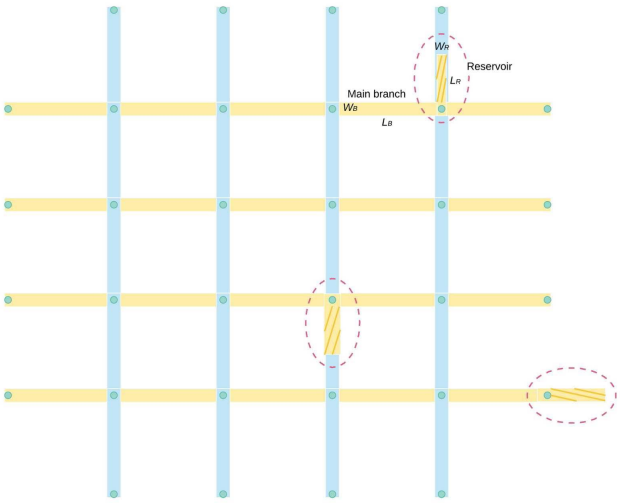

Fig. 8. Inserted reservoirs in the power grid network.

Fig. 8 shows the placement of reservoirs in a practical P/G layout where the shaded yellow branches in the power grids are reservoirs. If the cathode is at the terminal of a multibranch wire, then the reservoir can be placed either at the top, bottom, left or right of the wire. In general, reservoirs should be placed as close to the cathode as possible to have the maximum effect. But in a practical layout, the reservoir placement is subject to the routing and area constraints.

After the location of the reservoir is determined, we need to decide its size and shape. As we know, the width of the reservoir has a higher impact on the lifetime, to be more specific, on the nucleation time. The wider the width, the longer the lifetime, as it leads to slower stress growth. As a result, width is a preferred parameter over length to improve the EM lifetime. Take Fig. 6 as an example, assume node 1 is the ground (cathode) node, and then, j_R should be 0. We can obtain the following equations:

$$V_E = \frac{a_2 V_2}{2A} = \frac{(l_b w_b)\cdot V_2}{(l_b w_b)+(l_b w_b)}$$
$$V_{E,\text{new}} = \frac{a_2 V_2}{2A_{\text{new}}} = \frac{(l_b w_b)\cdot V_2}{(l_R w_R)+(l_R w_R + l_b w_b)+(l_b w_b)} \quad (33)$$

where A and A_{new} are the areas of the wire before and after reservoir insertion, respectively.

According to (4), to make the interconnect immortal, we should have

$$V_{\text{crit,EM}} > V_{E,\text{new}} - V_{\text{cat},m}. \quad (34)$$

Here, $V_{\text{cat},m}$ will be zero for ground networks, but will not be zero for power networks for the mth interconnect. Then, A_{new} can be calculated easily by making the inequality equal

$$A_{\text{new}} = \frac{A\cdot V_E}{V_{\text{crit,EM}} + V_{\text{cat},m}} \quad (35)$$

and $A_{\text{reservoir}}$ can also be obtained

$$A_{\text{reservoir}} = A_{\text{new}} - A. \quad (36)$$

Algorithm 2 EM Immortality-Constrained P/G Wire Sizing Algorithm With Reservoir Insertion

Input: Spice netlist G_I containing a P/G network.
Output: Optimized P/G network parameters.

```
repeat
    Perform Algorithm 1 using G_I.
    if fail due to the EM constraints then
        Find all the mortal wires.
        Insert reservoir segments (also properly sized) at or
        around the cathodes of these wires so that all of those
        wires become immortal.
    else
        Break.
    end if
until optimize successfully
Return f(V, I).
```

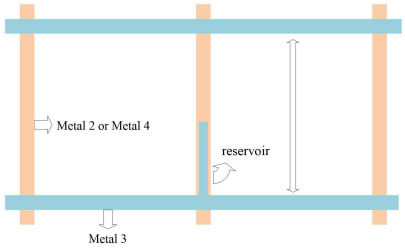

Fig. 9. Design rule check for reservoir segment placement.

$A_{\text{reservoir}}$ is actually the minimum area added to the cathode node to make the mortal wire immortal. For power grid network optimization, adding reservoir branches helps to increase the lifetime of the wire greatly, at the cost of some chip area. In other words, for the wires that are hard to optimize the EM immortality-constrained optimization, we can trade some chip area for longer P/G wire lifetime. The modified wire sizing algorithm is summarized as Algorithm 2.

When compared with Algorithm 1, Algorithm 2 needs to do the EM condition check and reservoir insertion, whose computing cost is quite small and thus can be ignored. As a result, Algorithm 2 has the same time complexity as Algorithm 1: $f_{\text{SLP}}(n, b)$.

Note, once a reservoir is inserted to a power grid network, it does not participate in sizing, but just provides a smaller *EM voltage*. The reason being, the reservoir is a zero-current branch, and in the objective function, we represent branch area by branch current in the numerator.

Adding reservoirs may be subject to some design rules in the practical layout. We first try to add the reservoir branch along the preferred routing direction, which is perpendicular to the current flow direction of the main branch. The maximum allowable length for the reservoir branch is the grid distance minus the minimum space requirement, as shown in Fig. 9. Otherwise, we can add the reservoir branch in the nonpreferred direction if the design rule is still allowed. If neither is possible, then the EM lifetime-constrained P/G optimization method (to be presented next) will be applied.

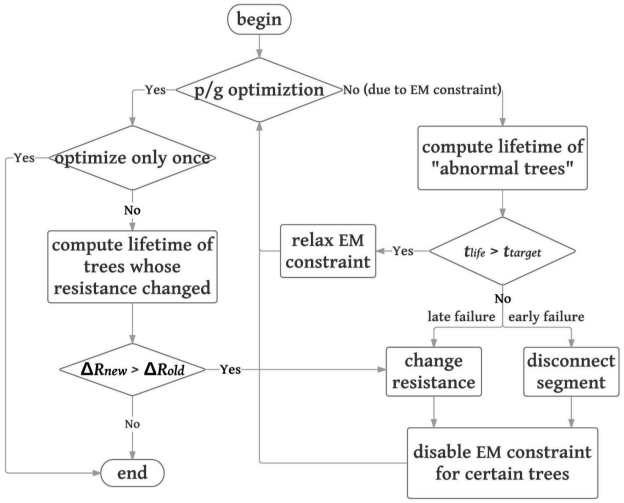

Fig. 10. Flowchart of the EM lifetime-constrained P/G optimization process.

V. EM Lifetime-Constrained Optimization

In Section IV, we discussed the power grid sizing optimization ensuring none of the interconnect trees fail based on the voltage-based EM immortality check. However, such EM constraint may be conservative because some wires can have EM failures as long as the power grid networks can still work (its IR drop is still less than the given threshold) in the target lifetime (e.g., ten years).

A. New EM Lifetime-Constrained Optimization Flow

In this section, we propose a new EM lifetime-constrained P/G wire sizing optimization method in which some segments of multisegment interconnect wires will be allowed to fail or to age. The impacts of these segments in terms of resistance change or even wire openings will be explicitly considered and modeled. Such aging-aware EM optimization essentially takes the EM aging-induced impacts or guard bands into account so that the designed P/G networks can still work in the target lifetime. In this paper, we only consider the void formation, which is the dominant EM failure effect and will lead to an increase in resistance. On the other hand, hillocks or extrusion will cause resistance decrease or even short circuit, i.e., $\Delta R < 0$. In terms of voltage and current, $\Delta R < 0$ means a decrease in voltage or IR drop, or an increase in current, or both. As a result, hillocks can have positive (reduced IR drop) or negative impacts (increased current density) on the P/G network.

The new optimization flow is shown in Fig. 10. In this new flow, we first check whether a given power supply network can be optimized using the EM immortality P/G optimization given in Algorithm 1. If the optimization does not succeed, it means that the EM condition may be overconstrained (perhaps, the overconstraints are due to IR drop constraints instead of EM constraints; in this case, topology changes will be needed and it falls out of the scope of this paper). After this step, the lifetime of all the interconnect trees will be computed based on the EM lifetime estimation method discussed in Algorithm 3.

We have several scenarios to discuss before we perform the optimization again. Let us define $t_{\text{life},m}$ as the lifetime of the mth interconnect tree and t_{target} as the target lifetime.

1) *If* $\boldsymbol{V_{E,m} - V_{\text{cat},m} > V_{\text{crit,EM}}}$ *and* $\boldsymbol{t_{\text{life},m} < t_{\text{target}}}$*:* The mth interconnect wire will be marked as a *failed wire*. Then, we have the following changes for the wire before the next round of optimization.
   If it is an early failure case, the cathode node of the wire segment connected by the failed via will be disconnected, which is called *wire disconnection*. The failure cases will depend on the current directions around the cathode node. Also the disconnection will depend on whether the void growth can eventually reach the critical void size or not as discussed in Section II-B.
   If it is a late failure case, the wire segment associated with the cathode node will have a *resistance change*. The specific resistance change for each failed segment will be calculated based on the target lifetime using our EM lifetime estimation method.
   If an interconnect tree is marked as a failed one, then its EM constraint will be disabled as we do not need to consider its immortality anymore.
2) *If* $\boldsymbol{V_{E,m} - V_{\text{cat},m} > V_{\text{crit,EM}}}$ *and* $\boldsymbol{t_{\text{life},m} > t_{\text{target}}}$*:* The lifetime of the interconnect wire still meets the target lifetime even though it will have void nucleation and resistance change. This also includes the case in which the void growth saturates before its size reaches the critical void size. The wire still works since the current can flow through the barrier layer.
   In this case, we use the existing $V_{E,m} - V_{\text{cat},m}$ value as the new EM constraint (defined as $V_{E,m,\text{next}} - V_{\text{cat},m,\text{next}}$) for this wire only ($m$th wire): $V_{E,m} - V_{\text{cat},m} < V_{E,m,\text{next}} - V_{\text{cat},m,\text{next}}$. This is called *constraint relaxation*. The rational behind this is that we expect the EM status of this wire to become worse during the next optimization so its lifetime will not change too much and still meet the given lifetime after the follow-up optimizations.

After *resistance change* or *wire disconnection* or *constraint relaxation*, a new round of SLP programing optimization, which is similar to Algorithm 1, is carried out.

When the P/G optimization is successfully finished, one has to check if all the wires, which are marked as failed ones, meet their failure conditions. For instance, if a failed wire (its failed segment) has 20% resistance change at the target 10-year lifetime before the optimization, and however, after the optimization, it has 30% resistance change at 10 years, then the final IR drop condition may not meet at 10 years. As a result, more iterations need to be carried out until such process is converged.

Another way to avoid such iterations is to set up some guard bands. Specifically, we can increase the target lifetime from 10 to 15 years when computing the resistance change for all the failed wires. After optimization, we check whether all the failure conditions are satisfied against the real 10-year target. In this way, we may just need one iteration at the cost of more routing areas used for the power supply networks.

Algorithm 3 Lifetime or Resistance Change Analysis for an Interconnect Tree

Input: A given interconnect wire and its electrical conditions, target lifetime t_{target}.
Output: Lifetime of the wire t_{life} and resistance change ΔR at t_{target}.

```
Compute the initial current density and the corresponding EM driving force.
/*Nucleation Phase*/
Compute the transient hydrostatic stresses σ_{x,t} inside the interconnect tree.
if σ_{max,t} > σ_{crit} then
    Solve the nucleation time t_{nuc} using bisection search method.
    /*Incubation Phase*/
    if L_{ss} < ΔL_{crit} then
        t_{inc} := ∞ and ΔR := 0.
    else
        Compute t_{inc} using Eq. (17).
        /*Growth Phase*/
        if early failure mode is true then
            t_{growth} := 0 and ΔR := ∞.
        else
            Compute t_{growth} using Eq. (18) assuming ΔR = 0.1 * R or compute the wire resistance change ΔR so that t_{nuc} + t_{inc} + t_{growth} = t_{target}.
        end if
    end if
    t_{life} := t_{nuc} + t_{inc} + t_{growth}.
else
    t_{life} := ∞ and ΔR := 0.
end if
Return t_{life} and ΔR.
```

The time complexity of the new EM lifetime-constrained optimization flow shown in Fig. 10 is $O(l * f_{\text{SLP}}(n, b)) + O(b)$, where l is the number of iterations in Algorithm 1 and $O(b)$ comes from Algorithm 3 discussed in the following. Since $f_{\text{SLP}}(n, b)$ is nonlinear with respect to b, the total time complexity can be further reduced to $O(l * f_{\text{SLP}}(n, b))$.

B. Transient EM Analysis for a Multisegment Interconnect Wire

One important aspect of the proposed lifetime-constrained power supply network optimization is to calculate the lifetime of a given wire and its electrical conditions. Another process we need is to compute the resistance change for a given target lifetime. Based on the EM models and fast assessment techniques presented in Section II, the two functions can be described by the following transient EM analysis algorithm: Algorithm 3. In this algorithm, if the increased resistance of the nucleated branch exceeds 10%, the interconnect tree is marked as failed.

In Algorithm 3, to compute the lifetime t_{life} of a given wire, we need to make sure that the wire is mortal and (4) is not satisfied. If the target lifetime t_{target} is given, then Algorithm 3 will return the resistance change ΔR at the target lifetime.

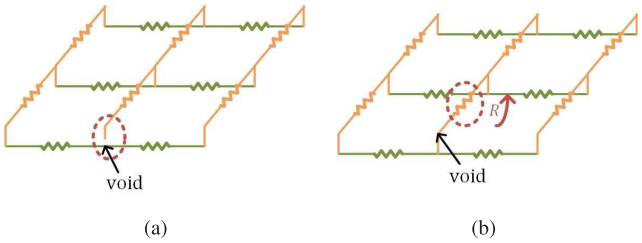

Fig. 11. Electrical impact of different failure mechanisms on the interconnect wires. (a) Early failure mode. (b) Late failure mode.

For those mortal wires, we start with time $t = 1000$ years and use the bisection method to find t_{nuc}. The transient hydrostatic stress will be computed by (10) at the given time. Once the stress of one segment hits the critical stress, the wire is deemed as nucleated.

First, we discuss the case that the wire is void incubation phase immortal, that is, the void saturated length is less than the critical length. Then, the incubation time (eventually the lifetime) becomes infinite, and the resistance remains unchanged.

Otherwise, the failure mode of the wire should be determined by looking at the current direction in the cathode node based on the patterns in Fig. 3(a) and (b).

If the wire is in the early failure mode, then the wire will become an open circuit. In this case, the whole interconnect tree will be disconnected from another interconnect wire, as shown in Fig. 11(a). For the wire, in the late failure mode, we have another solution. The wire resistance change will be incurred, and the growth time will be computed when the resistance change reaches 10%, as shown in Fig. 11(b). If the target lifetime is given, then the wire resistance changes by ΔR at the target lifetime.

In Algorithm 3, it is clear that finding out the void nucleation time t_{nuc} is the most time-consuming part. Specifically, the time complexity of calculating hydrostatic stress for one multisegment wire can be expressed as $O(s_i)$, where s_i is the number of segments of that wire. Once we obtained the stress, the cost of using the bisection method to find t_{nuc} is very small and can be ignored. Overall, the time complexity of Algorithm 3, which is to find the nucleation time for a wire i, is $f_{Alg3,i} = O(s_i)$. If in the worst case, all the wires are calculated, then the total time complexity becomes $O(b) = \sum_i^b f_{Alg3,i}$, where b is the number of wire segments of the whole P/G network.

VI. Experimental Results and Discussion

The proposed EM-aware and lifetime-constrained power grid optimization is implemented in C/C++. We carried out the optimization on a workstation with 2 Intel Xeon E5-2698, which has 128-GB memory. Both the IBM power grid networks [7] and self-generated networks are used to test this paper. From the annotated SPICE format IBM benchmarks, current source, voltage source, and resistance values can be obtained easily. Node location and layer information are also provided, and therefore, the geometric structure of a certain benchmark is known. Since there is no wire length and width information, we made some assumptions, including wire length and layer height for the experiments. Within the IBM power grid benchmarks, there are both power networks and ground networks. Only power networks are used to test our method, and their current source values are scaled to ensure that the initial voltage drop of each node is small enough. We assume that the material of the multisegment interconnect wire is Cu and the barrier layer is Ta. The maximum allowable IR drop is assumed to be 10% V_{dd}, and the minimum allowable width is 0.1 μm. Some important parameters used in our experimental setup are listed in Table I.

TABLE I
Parameters Used in the Optimization Process

Parameters	Value	Parameters	Value
σ_{crit}	500MPa	Ω	$1.182 \times 10^{-29}\text{m}^3$
V_{crit}	3.69×10^{-3}V	E_a	0.8eV
T	323K	D_0	$5.55 \times 10^{-8}\text{m}^2/\text{s}$
B	140GPa	ρ_{Cu}	$1.9 \times 10^{-8}\Omega \cdot \text{m}$
Z	10	ρ_{Ta}	$1.35 \times 10^{-7}\Omega \cdot \text{m}$

A. EM Immortality-Constrained Power Supply Optimization Results

Table II compares the results of the new optimization method using immortal EM constraint with the results of the existing P/G optimization method using the current-density-only EM constraint [12], [38]. Although many EM models have been proposed, including the new physics-based models [19], the current-density-based EM models based on the Black's equation and Blech's product [2], [28] are still widely used in today's industry even though they are subject to growing criticism. For the full-chip EM analysis, most EDA tools only check the current density to see if it meets the requirements provided by the manufacturer. Therefore, comparing the proposed method against the SLP method based on the current-based model is still meaningful. The proposed new EM immortality model [20], [22] used in the new SLP algorithm can be viewed as the extension of Blech's product to general multisegment interconnects. As a result, essentially, we compare and evaluate the impact of the EM immortality model against the Blech's product-based traditional EM model.

In our optimization processes, we assume that all the branches have the same width on one tree but different trees can have different widths. For a fair comparison, we only allow the difference in the EM constraints. In Table II, columns 1–4 list the P/G network benchmarks (*circuit*), the number of nodes in the P/G network (*# node*), the number of branches (*# bch*), and the original area [*area (mm^2)*]. Columns 5 and 7 show the CPU time of the two methods in minutes [*CPU time (min)*]. Columns 6 and 8 report the reduced chip area ratio [*area reduced (%)*] with respect to the original area for the two methods with voltage-based EM constraint (*voltage based (VB)-EM constraint*) and current-density-based EM constraint (*current density based (CD)-EM constraint*), respectively. Column 9 presents the minimum lifetime in years [$t_{\text{life-min}}$ *(yr)*] from current-density-based EM P/G optimization, as we

TABLE II
EM IMMORTALITY-CONSTRAINED P/G OPTIMIZATION RESULTS FOR IBM P/G NETWORKS

circuit	# node	# bch	area (mm^2)	VB-EM constraint		CD-EM constraint		
				CPU time (min)	area reduced (%)	CPU time (min)	area reduced (%)	$t_{life-min}$ (yr)
ibmpg1	11572	5580	158.43	0.06	35.66	0.06	72.29	13.57
ibmpg2	61797	61143	60.38	3.13	77.55	1.65	91.35	8.16
ibmpg3	407279	399201	697.71	131.00	22.60	28.57	57.98	9.64
ibmpg4	474836	384709	210.44	186.20	18.42	112.38	29.70	7.61

TABLE III
EM IMMORTALITY-CONSTRAINED P/G OPTIMIZATION WITH RESERVOIR INSERTION RESULTS FOR IBM P/G NETWORKS

circuit	# tree	# nucleated wires	area (mm^2)	w/o reservoir insertion	with reservoir insertion	
				finish successfully?	CPU time (min)	area reduced (%)
ibmpg1a	689	249	633.56	no	0.06	21.25
ibmpg2a	462	91	120.65	no	3.15	28.64
ibmpg3a	7388	329	1032.55	no	131.85	15.22
ibmpg4a	9458	0	210.44	yes	186.20	18.42

may have mortal wires after the optimization. Usually, the optimization process can be completed within three iterations.

As we can see, for the *ibmpg2* example, which has 61 797 nodes, 120 voltage sources, and 18 963 current sources, the original area is 60.38 mm^2. After two iterations, the area can be reduced to 13.55 mm^2, which means that 77.55% area has been reduced. Although the previous work [12] has about 91.35% reduction, better performance in terms of area reduction, our detailed analysis shows that there exist many mortal wires. For instance, one wire has a lifetime of 7.8 years. In contrast, the new work ensures that none of the wires fail.

It can be observed that the new method typically leads to less area reduction compared with the current-density-based method. But we want to emphasize that the two methods are not equal, as the existing current density method [38] was based on Black's equation, which cannot ensure EM immortality. Table II basically shows that the proposed method can guarantee the immorality of the whole P/G network, while the existing method cannot and some of the optimized results can even lead to the violation of 10-year lifetime constraint (such as the *ibmpg2, ibmpg3, ibmpg4*) even though they may have better area reduction ratio. Essentially, the current-based EM optimization trades lifetime for better area reduction.

As for CPU time, since all interconnect trees need to be calculated at least once in the new P/G optimization method, it takes some time to build the new EM constraint; as a result, the new method is a bit slower than the *CD-EM constraint* method. Furthermore, the interconnect trees with more branches usually need more time to get the EM voltage.

B. EM Immortality-Constrained Power Supply Optimization With Reservoir Insertion Results

Next, we show the results from the reservoir insertion and EM immortality-constrained SLP programing for P/G optimization. Instead of directly using the original IBM P/G networks, we made some modifications on them. We mainly increased the lengths of wires while keeping the original mesh structures. Additionally, a few branches of the benchmarks have been added or deleted. The goal is to make the power grid more vulnerable to EM failure.

The only exception is *ibmpg4a*, which is the same as *ibmpg4*. In this case, we show that if a power grid network can be optimized successfully without reservoir insertion, then performing Algorithm 2 is equivalent to performing Algorithm 1.

In the optimization process, we assume that all the reservoirs are added in two directions, e.g., on the top of a horizontal interconnect tree and on the left of a vertical interconnect tree. If one wire is determined to be mortal, we first add a reservoir of the calculated size at the cathode node to make the wire immortal and then perform the two-phase optimization process. The inserted reservoir and the interconnect tree should be in the same layer. The length of the reservoir will be limited to be less than its perpendicular branch length.

Table III shows the results of the new optimization method with reservoir insertion feature. In Table III, columns 2 and 3 show the number of total trees (*# tree*) and the number of trees that may fail (*# nucleated wires*). Columns 5 tells if the first optimization (*w/o reservoir insertion*) can be finished successfully. Columns 6 and 7 give the CPU time and the reduced chip area ratio with respect to the original area when the reservoir insertion option is turned on.

As we can see, the CPU time results are similar to those with the *VB-EM constraint* method in Table II, which means that the reservoir insertion does not have much computing overhead. In Table III, the P/G networks are quite different from those in Table II because of the EM concern. So the area reduction results of the two networks are different even using the same SLP algorithm.

From the results, we can see that by adding reservoir branches, the mortal power grid networks can be made immortal without consuming much extra running time, and the area can still be optimized successfully using the SLP. In every iteration, nodal voltages and branch currents are changed. We remark that cathode node voltage may change, but the cathode node typically does not change. After adding a reservoir onto an interconnect, a new EM voltage $V_{E,\text{new}}$ in (33) will be used for P/G optimization. Then, the area of

TABLE IV
EM LIFETIME-CONSTRAINED P/G NETWORKS FOR SELF-GENERATED P/G NETWORKS

circuit	# tree	# nucleated wires	before optimization	after optimization		CPU time (s)	area reduced (%)
			$t_{life-min}$ (yr)	$t_{life-min}$ (yr)	$V_{crit-max}$ (V)		
pg5×10	15	1	-	immortal	-	1.84	76.51
pg10×10	20	5	80.68	77.39	4.307×10^{-3}	11.95	38.29
pg30×50	80	11	5.53	19.88	5.61×10^{-2}	96.39	26.68
pg20×100	120	8	> 100	> 100	7.22×10^{-2}	117.52	46.62

the resulting interconnect will be optimized (reduced or no change) while the EM immortality constraint can still hold after the optimization.

C. EM Lifetime-Constrained Power Supply Optimization Results

Table IV shows the lifetime-constrained P/G optimization with our self-generated P/G networks. We remark that the IBM P/G circuits may not have the desired immortal wires suitable for the demonstration, and it is more convenient to use the self-generated power supply grids because we need to test our optimizer under different testing conditions. These network topologies are simple, the name pg10 × 10 means that the circuit consists of 10 rows and 10 columns power grid strips, and in other words, there are 20 interconnect trees in total. So the size of the circuit in terms of nodes is approximately equal to # of rows × # of columns. In Table IV, column 3 shows the number of nucleated trees that stall the optimization. Note that the nucleated wires can be the failed wires or wires have potential to fail (its final lifetime may be longer than the target lifetime even though its $V_E - V_{\text{cathode}}$ is larger than the critical voltage). If we have to relax the EM constraint, the maximum V_{crit} value will be presented in column 6 [$V_{\text{crit}-\text{max}}$ *(V)*]; meanwhile, the shortest lifetime after optimization is presented in column 5 [$t_{\text{life}-\text{min}}$ *(yr)*].

From Table IV, we can see that if there are no violations for the initial P/G networks, the optimization can be easily carried on. Sometimes, even with some violations, after a few *P-V* and *P-I* iterations, the violations can be eliminated, and we can still obtain EM immortal solution. Note that the area improvement strongly depends on the original layouts; thus, the absolute values of the reduced area are not that important. We notice that there are several nucleated wires in each case, which means that we do not check their EM during the optimization process, as we treat them as failed wires. For instance, for *pg5 × 10* case, there exists a nucleated wire before optimization. We would not check the lifetime until the optimization finishes, and however, after optimization, no lifetime calculation is needed, as the network becomes immortal.

As for *pg30 × 50* case, before optimization, the shortest lifetime $t_{\text{life}-\text{min}}$ is 5.53 years, which violates the lifetime constraint. After the optimization, the lifetime was improved to 19.88 years. As we can see from this example, the lifetime can be extended while the area can still be saved. The reason is that we let some wires fail or relax, but the failure of those wires (resistance change or open circuits) will be compensated by properly sizing of other wires to meet the lifetime requirement due to the redundant structure design of the P/G networks. It may lead to a wider width, but the overall area of all the wires can be reduced. This further demonstrates the superior advantage of the lifetime-constrained method over the immortality-constrained method.

For other cases, even though they have a few nucleated wires, their lifetime is very long. After optimization, this is still the case. For most cases, if $V_E - V_i \gg V_{\text{crit}}$ in the initial condition, it is difficult to optimize successfully for the first time. With our lifetime-constrained optimization flow, the optimization results can always be achieved after several iterations so that the lifetime target can be met.

VII. CONCLUSION

In this paper, we first proposed the new P/G network sizing technique based on the recently proposed voltage-based EM immortality check method for general multisegment interconnect wires and the physics-based EM assessment technique for the fast TTF analysis. We showed that the new P/G optimization problem subject to the voltage IR drop and new EM constraints can still be formulated as an efficient SLP problem. The new optimization method will ensure that none of the wires fail if all the constraints are satisfied. In addition, we improved the optimization method with reservoir branch insertion, which helps to make the initial P/G network more robust. To mitigate the overly conservative nature of the optimization formulation, we further considered the EM-induced aging effects on power supply networks for a target lifetime and then proposed an EM lifetime-constrained optimization method, which allows some short-lifetime wires to fail and optimizes the rest of the wires. Numerical results on a number of IBM and self-generated power supply networks showed that the new methods can effectively reduce the area of the power grid networks while ensuring the reliability in terms of immortality or target lifetime, which is not the case for the existing current-density-constrained P/G optimization methods.

REFERENCES

[1] H. Zhou, Y. Sun, Z. Sun, H. Zhao, and S. X.-D. Tan, "Electromigration-lifetime constrained power grid optimization considering multi-segment interconnect wires," in *Proc. 23rd Asia South Pacific Design Automat. Conf. (ASP-DAC)*, Jan. 2018, pp. 399–404.
[2] J. R. Black, "Electromigration—A brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. 16, no. 4, pp. 338–347, Apr. 1969.
[3] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*. Reading, MA, USA: Addison-Wesley, 1990.
[4] Q. K. Zhu, *Power Distribution Network Design for VLSI*. Hoboken, NJ, USA: Wiley, 2004.

[5] F. Chen *et al.*, "A comprehensive study of low-k SICOH TDDB phenomena and its reliability lifetime model development," in *Proc. IEEE Int. Rel. Phys. Symp.*, Mar. 2006, pp. 46–53.
[6] (2015). *International Technology Roadmap for Semiconductors (ITRS) Interconnect, 2015 Edition*. [Online]. Available: http://public.itrs.net
[7] S. R. Nassif, "Power grid analysis benchmarks," in *Proc. Asia South Pacific Design Automat. Conf. (ASPDAC)*, Mar. 2008, pp. 376–381.
[8] S. Chowdhury and M. Breuer, "Minimal area design of power/ground nets having graph topologies," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 12, pp. 1441–1451, Dec. 1987.
[9] S. Chowdhury and M. A. Breuer, "Optimum design of IC power/ground nets subject to reliability constraints," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. CAD-7, no. 7, pp. 787–796, Jul. 1988.
[10] S. Chowdhury, "Optimum design of reliable IC power networks having general graph topologies," in *Proc. 26th ACM/IEEE Design Automat. Conf.*, Jun. 1989, pp. 787–790.
[11] R. Dutta and M. Marek-Sadowska, "Automatic sizing of power/ground (P/G) networks in VLSI," in *Proc. 26th Design Autom. Conf. (DAC)*, Jun. 1989, pp. 783–786.
[12] S. X. D. Tan, C. J. R. Shi, and J.-C. Lee, "Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 22, no. 12, pp. 1678–1684, Dec. 2003.
[13] S. X. D. Tan and C. J. R. Shi, "Efficient very large scale integration power/ground network sizing based on equivalent circuit modeling," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 22, no. 3, pp. 277–284, Mar. 2003.
[14] K. Wang and M. Marek-Sadowska, "On-chip power-supply network optimization using multigrid-based technique," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 3, pp. 407–417, Mar. 2005.
[15] V. Sukharev, "Beyond Black's equation: Full-chip EM/SM assessment in 3D IC stack," *Microelectron. Eng.*, vol. 120, pp. 99–105, Sep. 2014.
[16] X. Huang, A. Kteyan, X. Tan, and V. Sukharev, "Physics-based electromigration models and full-chip assessment for power grid networks," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 11, pp. 1848–1861, Feb. 2016.
[17] C. V. Thompson, S. P. Hau-Riege, and V. K. Andleigh, "Modeling and experimental characterization of electromigration in interconnect trees," in *Proc. AIP Conf.*, vol. 491, 1999, pp. 62–73.
[18] S. P. Hau-Riege and C. V. Thompson, "Experimental characterization and modeling of the reliability of interconnect trees," *J. Appl. Phys.*, vol. 89, no. 1, pp. 601–609, 2001.
[19] S. X.-D. Tan, H. Amrouch, T. Kim, Z. Sun, C. Cook, and J. Henkel, "Recent advances in EM and BTI induced reliability modeling, analysis and optimization," *Integration*, vol. 60, pp. 132–152, Jan. 2018.
[20] Z. Sun, E. Demircan, M. D. Shroff, T. Kim, X. Huang, and S. X.-D. Tan, "Voltage-based electromigration immortality check for general multi-branch interconnects," in *Proc. Int. Conf. Comput. Aided Design (ICCAD)*, Nov. 2016, pp. 1–7.
[21] X. Wang, Y. Yan, J. He, S. X.-D. Tan, C. Cook, and S. Yang, "Fast physics-based electromigration analysis for multi-branch interconnect trees," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2017, pp. 169–176.
[22] Z. Sun, E. Demircan, M. D. Shroff, C. Cook, and S. X.-D. Tan, "Fast electromigration immortality analysis for multisegment copper interconnect wires," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 12, pp. 3137–3150, Dec. 2018.
[23] C. Cook, Z. Sun, E. Demircan, M. D. Shroff, and S. X.-D. Tan, "Fast electromigration stress evolution analysis for interconnect trees using krylov subspace method," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 969–980, May 2018.
[24] J. Lienig and M. Thiele, *Fundamentals of Electromigration-Aware Integrated Circuit Design*. New York, NY, USA: Springer, 2018.
[25] S. M. Alam, C. L. Gan, C. V. Thompson, and D. E. Troxel, "Reliability computer-aided design tool for full-chip electromigration analysis and comparison with different interconnect metallizations," *Microelectron. J.*, vol. 38, nos. 4–5, pp. 463–473, 2007.
[26] C.-K. Hu *et al.*, "Effects of overlayers on electromigration reliability improvement for Cu/low K interconnects," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2004, pp. 222–228.
[27] L. Zhang, "Effects of scaling and grain structure on electromigration reliability of cu interconnects," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. Texas Austin, Austin, TX, USA, 2010.
[28] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *J. Appl. Phys.*, vol. 47, no. 4, pp. 1203–1208, Apr. 1976.
[29] M. A. Korhonen, P. Bo-Rgesen, K. N. Tu, and C.-Y. Li, "Stress evolution due to electromigration in confined metal lines," *J. Appl. Phys.*, vol. 73, no. 8, pp. 3790–3799, 1993.
[30] C. Cook, Z. Sun, T. Kim, and S. X.-D. Tan, "Finite difference method for electromigration analysis of multi-branch interconnects," in *Proc. 13th Int. Conf. Synth., Modeling, Anal. Simulation Methods Appl. Circuit Design (SMACD)*, Jun. 2016, pp. 1–4.
[31] S. Chatterjee, V. Sukharev, and F. N. Najm, "Power grid electromigration checking using physics-based models," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 7, pp. 1317–1330, Jul. 2018.
[32] H.-B. Chen, S. X.-D. Tan, X. Huang, T. Kim, and V. Sukharev, "Analytical modeling and characterization of electromigration effects for multibranch interconnect trees," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 11, pp. 1811–1824, Nov. 2016.
[33] X. Wang, H. Wang, J. He, S. X.-D. Tan, Y. Cai, and S. Yang, "Physics-based electromigration modeling and assessment for multi-segment interconnects in power grid networks," in *Proc. Design, Automat. Test Eur. Conf. Exhib. (DATE)*, Mar. 2017, pp. 1727–1732.
[34] A. H. Verbruggen, M. J. C. van den Homberg, L. C. Jacobs, A. J. Kalkman, J. R. Kraayeveld, and S. Radelaar, "Resistance changes induced by the formation of a single void/hillock during electromigration," in *Proc. AIP Conf.*, 1998, vol. 418, no. 1, pp. 135–146.
[35] C.-K. Hu, M. B. Small, and P. Ho, "Electromigration in Al(Cu) two-level structures: Effect of Cu and kinetics of damage formation," *J. Appl. Phys.*, vol. 74, no. 2, pp. 969–978, 1993.
[36] Z. Sun, S. Sadiqbatcha, H. Zhao, and S. X.-D. Tan, "Accelerating electromigration aging for fast failure detection for nanometer ICs," in *Proc. 23rd Asia South Pacific Design Automat. Conf. (ASP-DAC)*, Jan. 2018, pp. 623–630.
[37] M. S. Bazaraa, H. D. Sherali, and C. M. Shetty, *Nonlinear Programming: Theory and Algorithms*. Hoboken, NJ, USA: Wiley, 2013.
[38] X.-D. Tan, C.-J. R. Shi, D. Lungeanu, J.-C. Lee, and L.-P. Yuan, "Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings," in *Proc. Design Autom. Conf. (DAC)*, Jun. 1999, pp. 78–83.

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