Recovery-Aware Proactive TSV Repair for Electromigration Lifetime Enhancement in 3-D ICs

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***Abstract*— Electromigration (EM) becomes a major reliability concern in 3-D integrated circuits (3-D ICs). To mitigate this problem, a typical solution is to use through-silicon via (TSV) redundancy in a reactive manner, maintaining the operability of a 3-D chip in the presence of EM failures by detecting and replacing faulty TSVs with spares. In this paper, we explore an alternative, more preferred approach to enhance the EM-related lifetime reliability of TSV grid, in which redundancy is used proactively to allow nonfaulty TSVs to be temporarily deactivated. In this way, EM wear-out can be extended by exploiting its recovery property. The proposed solution is based on two consecutive stages, in which TSV redundancy allocation and TSV repair are finalized at both design-time and runtime, respectively. Applied to 3-D benchmark designs, the recovery-aware proactive repair approach increases EM-related lifetime reliability (measured in mean-time-to-failure) of the entire TSV grid by up to 12× relative to the conventional reactive method, with similar area overhead. In addition, a runtime dynamic recovery approach is proposed to further improve EM-related lifetime reliability to account for stress variation across different chips and over the operational lifetime.**

***Index Terms*— Electromigration (EM), healing process, mean-time-to-failure (MTTF), three-dimensional integrated circuits (3-D ICs), through-silicon via (TSV).**

I. Introduction

THREE-DIMENSIONAL integrated circuits (3-D ICs) promise to overcome interconnect bottlenecks in CMOS scaling by leveraging fast, dense interdie vias [1]. Typically, a complete 3-D IC implementation is envisioned as a stack of active chips using through-silicon vias (TSVs) to connect through each chip down to a package substrate. By utilizing such vertical connection, 3-D ICs can provide abundant interconnect bandwidth with improved performance and less communication-energy consumption. However, concerns related to TSV reliability are key obstacles in the commercial exploitation of TSV-based 3-D IC technology [2].

As one of the critical challenges for TSV reliability, electromigration (EM) refers to the diffusion of metal atoms induced by electric current [2]. Due to increased current density, higher temperature, and thermal mechanical stress, EM reliability of TSVs[1] in a 3-D IC becomes further exacerbated compared to the conventional interconnects in its 2-D counterpart. The gradual transport of metal atoms caused by EM leads to void nucleation and growth on the line under TSV during field operation. This will significantly increase resistance of the circuit, and may eventually cause open/short defects, which can drastically reduce the mean-time-to-failure (MTTF) of a 3-D IC [3].

In order to extend EM-related lifetimes of TSVs, a typical solution is to add spare TSVs (referred to s-TSVs in this paper) in the design to repair defective functional TSVs (referred to f-TSVs) at runtime. To this end, various TSV redundancy allocation techniques and their corresponding repair algorithms have been proposed in the literature [3], [4]. TSV defects induced by EM can be effectively tolerated by in-field reconfigurable repair solutions. However, the transient recovery effect in EM-induced stress evolution was ignored completely in all these existing *ad hoc* methodologies. Here, the "recovery effect" refers to the EM stress relaxation in the interconnect, which occurs when there is no/lower/reverse current passing. Consequently, this effect can be considered as a healing process extending the lifetime of an interconnect as it will take longer time for the stress to reach to the critical threshold for void nucleation [5], [6]. Such phenomena have been observed in many previous experimental works [7], [8]. According to these experiments, this healing process possesses positive temperature dependence and directional property: on the one hand, higher temperatures lead to faster and more complete recovery of EM stress and on the other hand, this recovery phenomenon is more visible when the interconnect is stressed by bidirectional current waveforms compared with unidirectional ones. Therefore, since most of the f-TSVs in 3-D ICs experience very high temperatures and carry bidirectional currents [9], they exhibit significant recovery effect, which can be leveraged for EM-related lifetime enhancement.

In this paper, a recovery-aware proactive TSV repair solution is proposed to enhance the EM-related lifetime reliability of regular f-TSV grids in which TSVs are placed uniformly. In this repair approach, TSV redundancy is used proactively to allow nonfaulty f-TSVs to be temporarily deactivated and be able to recover from certain EM wear-out well before failing. To this purpose, the implementation of the proposed

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[1] In this paper, we limit our scope only to the signal TSVs. Therefore, the term "TSV" in this paper refers to signal TSV unless otherwise specified.

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methodology consists of two stages.

1) Design-time TSV grouping: After identifying the f-TSVs vulnerable to EM failures, we partition them into groups and then assign s-TSV(s) to each group with appropriate placement. This grouping is implemented based on lifetime reliability as well as signal rerouting constraints.
2) Runtime TSV repair: In each group, the logic signals carried by the f-TSVs take turn being transmitted through the assigned spare(s), which allows all the TSVs [including the redundant one(s)] to be deactivated on a rotating basis and recover from EM wear-out.

Some preliminary results of this paper are published in [10]. Overall, our contributions are summarized as follows.

1) In order to reduce the delay and area overheads introduced by the proposed repair solution, we proposed a set of design-time optimization techniques to determine optimal TSV grouping in the post placement/prerouting stage. Moreover, a greedy group-merge algorithm is proposed to further reduce the area overhead and achieve a better tradeoff between lifetime reliability and hardware cost.
2) A runtime repair scheme is proposed in this paper, consisting of a lightweight reconfigurable rerouting mechanism and two effective recovery schedules. In particular, a static scheduling approach is used when the workloads can be estimated *a priori*. However, in order to handle a more realistic operation condition with dynamic workload changes, a dynamic recovery scheduling approach is also proposed in this paper.

Our simulation results demonstrate the following.

1) Applied to 3-D benchmark designs, our proactive repair approach increases EM-related lifetime reliability (measured in MTTF) of the f-TSV network by up to 12× compared to the conventional reactive method [3] with similar overhead.
2) The proposed greedy group-merge algorithm can further reduce the area overhead by up to 15% under the constraints of timing performance, and achieve a better tradeoff between lifetime reliability and hardware cost.
3) By considering the workload changes and the status of circuit aging, the proposed repair approach with dynamic recovery scheduling can achieve a higher MTTF (up to 4.5×) of the TSV grid compared to the static scheduling.

The rest of this paper is organized as follows. Preliminaries and related prior work are presented in Section II. The motivation and basic idea of the proposed proactive repair approach are presented in Section III. Sections IV and V describe the methodology in detail. In Section VI, we report simulation results. Finally, the conclusion is drawn in Section VII.

II. Preliminaries and Related Work

A. EM Recovery Effect

Until now, a number of previous works have studied EM issues in 3-D ICs, and showed that TSVs are susceptible to EM wear-out [3], [4]. Once the EM-induced hydrostatic tensile stress exceeds a critical value, a void would be formed on the line under TSV, which can increase its resistance, causing path delay fault, and eventually open/short defect [3]. However, this time-varying stress can be reduced when the current density in the stressing current goes down (or even negative) temporarily, which is the so-called "EM recovery effect." This recovery effect can be quite significant when the interconnect is stressed by symmetric bidirectional (bipolar) pulse current waveforms. Moreover, temperature can also affect it, and higher temperatures lead to faster recovery. Due to the recovery property, it takes a longer time for the EM-induced stress to reach the critical value, and thus, results in a longer lifetime of an interconnect [5].

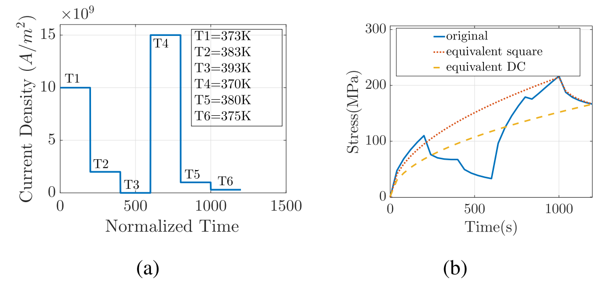

Fig. 1. (a) Original input driving current density. (b) Calculated EM dc equivalent current density with two different methods.

In order to leverage the recovery effect for lifetime reliability improvement at the system-level, an EM recovery model with "two-step" equivalent dc current was proposed in [11], which can consider transient recovery effect for the EM stress evolution using existing simple EM models. The generation of the equivalent dc current can be divided into two steps: First, an arbitrary waveform with time-varying current and temperature stress [as shown in Fig. 1(a)] is converted to an equivalent square waveform [red dotted line in Fig. 1(b)] by matching at both the highest peak stress and final stress in each period, instead of only matching the endpoint in the simple "equivalent dc" method [yellow dashed line in Fig. 1(b)]. Afterward, the generated current is further parameterized in terms of current density, duty cycle, temperature, and time period to define the waveform. As shown in Fig. 2, compared with the conventional equivalent dc method, the proposed technique in [11] has smaller errors in terms of time-to-failure estimation. By using this new recovery-aware EM dc current model, lifetime can be easily computed for a interconnect wire given the stressing current waveforms.

After void formed, the resistance starts to increase and this period of time is called growth phase. In the growth phase, we use the average current for simulation since the drift velocity is proportional to current density [6]. As shown in Fig. 3, the resistance change over time of cases with ac current and its average current are very close. So average current can be applied on the growth phase evaluation.

B. Related Prior Works

A number of s-TSV allocation techniques and their corresponding repair algorithms have been proposed in the literature [3], [12], [13]. However, all of them only

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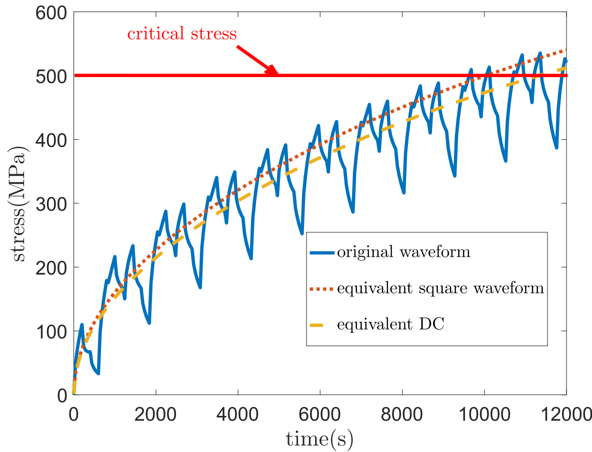

Fig. 2. Comparing the nucleation time of two different methods and original stress.

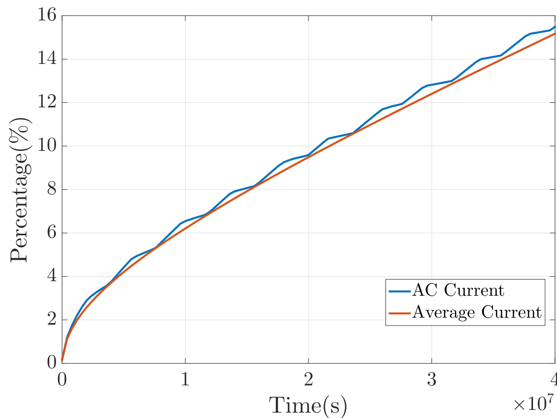

Fig. 3. Comparing resistance increase with ac current and average current.

target at tolerate manufacturing defects instead of runtime failures (e.g., EM wear-out). To tackle this problem, several in-field repair methodologies were proposed for the post manufacturing TSV faults [3], [4].

A typical in-field TSV repair scheme is as follows. First, s-TSVs are allocated in the design along with a reconfiguration infrastructure that enables signal rerouting. Afterward, on-line testing will be triggered periodically or by events. Once a particular f-TSV is detected to be faulty, it would be replaced by a standby s-TSV through the reconfigurable routing network. Therefore, such reactive repair allows as many TSV defects to be tolerated as there are nonfaulty s-TSVs. A TSV grid is regarded as being irreparable until the s-TSV resource is exhausted, and its lifetime reliability improvement is highly dependent on the number of allocated s-TSVs.

Due to this "detect-and-replace" scheme, the conventional reactive approach has the following shortcomings.

1) For conducting reactive in-field repair, it is imperative to implement an on-chip sensor network in order to test and diagnose faulty f-TSVs, which results in significant hardware cost.
2) Ignoring the EM recovery effect, the reactive approach cannot fully utilize the s-TSV resource, which makes the generated repair solution inefficient.

In this paper, we propose an alternative, more preferred proactive repair approach to address these drawbacks by exploiting the recovery property of EM wearout.

III. Motivation and Basic Idea

As opposed to replace f-TSVs after they become faulty, the proposed proactive approach allows f-TSVs to recover from EM wear-out before failing. By temporarily deactivating nonfaulty f-TSVs, the onset of EM failure can be delayed due to EM recovery effect, which significantly extends TSV lifetime. Therefore, such proactive repair approach has the following advantages over a reactive one.

1) Since f-TSVs can recover from EM wear-out before they fail, it is unnecessary to implement the entire on-chip sensor network for TSV defect detection and monitoring, which saves the associated hardware cost.
2) In the reactive repair approach, the number of tolerated f-TSV failures is limited by the amount of preallocated spares. By contrast, by exploiting the EM recovery effect, proactive approach can extend the lifetimes of multiple f-TSVs even using one single spare, taking full advantage of the limited redundancy resources.

Note that, the conventional reactive repair approach is completely compatible with the proposed one since s-TSVs can still be used if a real f-TSV failure occurs.

The proposed proactive repair approach is based on two consecutive stages. At design-time, the identified EM-vulnerable f-TSVs are partitioned into groups according to their lifetimes, and then s-TSV(s) is (are) subsequently assigned to each group under routing constraints. The corresponding algorithms will be discussed in Section IV. Afterward, the assigned s-TSVs are used proactively, which allows partitioned EM-vulnerable f-TSVs in each group to be temporarily deactivated according to different scheduling approaches and recover from EM wear-out before failing. The detailed implementation will be presented in Section V.

IV. Design-Time TSV Grouping

Due to the clustering effects of TSV faults [3], we may run into the situation that some faulty f-TSVs lack TSV redundancy while others have excessive one. Although allocating more s-TSVs can tackle this problem, it also results in significant hardware cost. Therefore, here we propose the following.

1) To identify the f-TSVs which are vulnerable to EM wear-out at design-time, and limit the use of s-TSVs to them only.
2) To adopt the "shared s-TSV" technique [14], which partitions the set of EM-vulnerable f-TSVs into groups and subsequently assign s-TSV(s) to each of them.

Therefore, the "design-time TSV grouping" problem can be consequently divided into the following subproblems: 1) vulnerable f-TSV identification; 2) f-TSV partitioning; and 3) s-TSV assignment.

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A. EM-Vulnerable f-TSV Identification

As a series system, the EM-related lifetime of a TSV grid is dominated by the f-TSVs which are susceptible to EM failures. Therefore, in order to reduce hardware cost, it is more efficient to provide TSV redundancy to the f-TSVs having lower EM-related lifetimes rather than all of them, and here we use the MTTF of an f-TSV to evaluate its vulnerability. Given a set of representative workloads [15], we can generate the power/thermal characteristics of each f-TSV, and then estimate its MTTF [11]. Note that, since we look into large time scales for EM recovery periods in this paper (details in Section V), here a steady-state temperature analysis is sufficient. Then, after comparing with a user-defined threshold value, the f-TSVs with lower MTTF will be identified as EM-vulnerable.

For the f-TSVs with zero or very small timing slacks, a TSV fault is not necessarily a catastrophic open/short defect, but often a timing failure due to EM-induced resistance increase. Therefore, the failure criteria of each TSV (i.e., EM-induced resistance variation) should be considered during timing analysis at design-time, and needs to be determined according to different timing slack of each EM-vulnerable f-TSV. In this paper, a 10% increase from the initial resistance value of the TSV is used as the EM failure criterion, as in [2] and [4].

B. f-TSV Partitioning

After identifying the EM-vulnerable f-TSVs, the next step is to partition them into groups for spare sharing. However, in order to obtain an effective repair solution, it should avoid apportioning the f-TSVs with the lowest MTTF into the same group. Therefore, this problem can be formulated as follows.

1) *Input:* a) A set of EM-vulnerable f-TSVs $\mathbf{F} = \{f_i\}$ in which each f-TSV f_i has its MTTF value $\text{LT}(f_i)$ and b) the f-TSV number in each partitioned group N_{gf}.
2) *Output:* A set of groups $\mathbf{G} = \{g_j\}$ that partitions $\mathbf{F}$.
3) *Constraint:* $\mathbf{F}$ is partitioned into $\lceil |\mathbf{F}|/N_{gf} \rceil$ groups with the most size N_{gf}.
4) *Objective:*

$$\text{Min} : \max_{\forall g_j \in \mathbf{G}} S(g_j)$$

where $S(g_j) = \sum_{\forall f_i \in g_j} \text{LT}(f_i)$.

Here, the objective can guarantee that the difference of total MTTF value between the maximal and minimal f-TSV groups is minimized, which leads to a uniform partition of vulnerable f-TSVs according to their lifetimes. Then, this f-TSV partitioning problem can be reduced to the balanced multiway number partitioning problem [16]. Using the proposed heuristic in [16], we can solve this problem in $O(n\log n)$ time, where $n = |\mathbf{F}|$.

C. s-TSV Assignment

For each partitioned f-TSV group, we need to subsequently assign s-TSV(s) to provide proactive redundancy, which allows f-TSVs to be temporarily deactivated and recover from EM wear-out. However, in order to maintain the normal operation of circuit, the logic signals carried by the f-TSVs should be capable of being rerouted during field operation. To this purpose, it is necessary to implement a reconfigurable network for signal rerouting, which inevitably introduces delay overhead. Therefore, the assigned s-TSV(s) for each group should be appropriately chosen among a given set in order to minimize the delay overhead introduced by the in-field repair solution. This issue becomes more critical for high-speed signals (such as memory bus signals), and thus should be accounted properly during TSV repair.

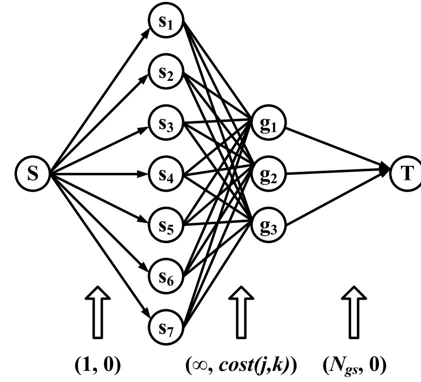

Fig. 4. Min-cost flow problem for s-TSV assignment.

The formal problem statement is as follows.

1) *Input:* a) A set of f-TSV groups $\mathbf{G} = \{g_j\}$ that partitions $\mathbf{F} = \{f_i\}$; b) a set of placed s-TSVs $\mathbf{S} = \{s_k\}$; and c) the assigned s-TSV number N_{gs} for each group.
2) *Output:* The mapping between $\mathbf{G}$ and the set of assigned s-TSVs $\mathbf{S}^* \subseteq \mathbf{S}$.
3) *Constraint:* The assigned s-TSV number of each group is equal to N_{gs}.
4) *Objective:* During in-field repair, the total delay overhead of all groups is minimized. Here, the delay overhead of a group is the maximum overhead of all its f-TSVs.

Generally, the delay overhead during repair comes from: 1) rerouting logic circuitry and 2) rerouting wire. The first aspect is determined by a given grouping ratio $\text{GR} = N_{gf}{:}N_{gs}$ (details are given in Section V). Therefore, the objective of this step is to minimize the delay overhead introduced by rerouting wire, and the additional wire length during rerouting is used as a metric to evaluate it, as in [17].

Here, we can formulate the s-TSV assignment as a min-cost flow problem. As illustrated in Fig. 4, a network $G = (V, E)$ is constructed, whose node set includes all the partitioned f-TSV groups $\{g_j\}$, all the placed s-TSVs $\{s_k\}$, a pseudo source node S, and a pseudo sink node T. There are three kinds of edges in the edge set E, where each edge will be assigned with a $(capacity, cost)$ pair as follows.

1) The source node S has supply of $N_{gs} \times |\mathbf{G}|$, and connect to $|\mathbf{S}|$ s-TSVs $\{s_k\}$. Each edge (S, s_k) has capacity 1 and cost 0.
2) There are $|\mathbf{S}| \times |\mathbf{G}|$ edges from the placed s-TSVs $\{s_k\}$ to the partitioned groups $\{g_j\}$. The capacity of edge (s_k, g_j) is infinity. Its cost, $cost(j, k)$, is the additional wire length during rerouting when assigning s_k to g_j. In other words, $cost(j, k) = \max_{\forall f_i \in g_j} L(f_i, s_k)$, where

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$L(f_i, s_k)$ is the Euclidean distance between f_i and s_k.

3) Every group g_j connects to the sink node T, where each edge (g_j, T) has a capacity of N_{gs} and a cost of 0.

In this min-cost flow problem, the generated solution indicates the optimal assignment of each placed s-TSV to the partitioned group, in the sense of the rerouting additional wire length, and can be solved in polynomial time [18].

D. Nonuniform TSV Grouping

Until now, we assumed that the grouping ratio value GR = $N_{gf}{:}N_{gs}$ of each TSV group is the same and deterministic. However, in order to fully use the assigned spare TSVs, a nonuniform TSV grouping with varying GR for each group seems to be more efficient when targeting a given MTTF. To this purpose, here we propose a greedy group-merge algorithm, as shown in Algorithm 1. Here, the initial f-TSV group $\mathbf{G}_0$ can be obtained by partitioning $\mathbf{F}$ with $N_{gf} = 1$, and then N_{gs} spare(s) is(are) assigned to each group $g_j \in \mathbf{G}_0$ for its MTTF estimation. Note that, since the locations of the assigned spares are determined during s-TSV assignment, their experienced temperatures cannot be obtained at this stage, which are the critical factors affecting EM-related TSV lifetime. In order to guarantee the achieved MTTF of the entire EM-vulnerable, f-TSV network can still satisfy the criteria that $\text{MTTF}_{\text{network}} \geq \text{MTTF}_{\text{target}}$ after the subsequent s-TSV assignment stage, here we assume that all the assigned spares experience the highest temperature among all the candidates.

Afterward, the nonuniform TSV group can be determined iteratively. In each iteration, the two "available" TSV groups with the highest MTTFs are merged together which results in the deletion of N_{gs} spare(s) in the merged group. Note that, here the MTTF of each group is the average lifetime of all f-TSVs in the same group. The term "available" means that the timing slack of each merged EM-vulnerable f-TSV f_i [Slack(f_i)] should satisfy the constraint

$$\text{Slack}(f_i) - \Delta D(f_i) \geq 0 \tag{1}$$

after merging them together. Here, $\Delta D(f_i)$ is the delay overhead of f_i induced by repair mechanism, which can be introduced by: 1) rerouting wire and 2) rerouting logic circuitry. For the first aspect, since the optimal mapping between f-TSVs and s-TSVs has already been determined by the proposed s-TSV assignment in Section IV-C, here we only need to make sure to:

1) delete the N_{gs} spare(s) resulting in more rerouting wire-induced delay overhead in each iteration;
2) avoid merging groups which are too far from each other.

Regarding the second aspect, due to the increase delay overhead of rerouting logic circuitry with the group size (discussed in Section V-C1), it should be avoided to repartition too many TSVs into the same group.

This iteration can be performed until $\text{MTTF}_{\text{network}}$ decreases to $\text{MTTF}_{\text{target}}$, and then all EM-vulnerable f-TSVs are repartitioned by the generated $\mathbf{G}'$ during group merging, in which each group has different f-TSV count. Based on this new f-TSV partition, the proposed s-TSV assignment approach is conducted to obtain a nonuniform TSV group, which can achieve the targeted MTTF using less s-TSVs.

Algorithm 1 Iterative Method for Nonuniform TSV Grouping

Input: $\mathbf{G}_0$, $\mathbf{S}$, $\text{MTTF}_{\text{target}}$, N_{gs}, $\Delta D_{\max}$
Output: $\mathbf{G}'$

```
1:  G' = ∅;
2:  repeat
3:      sort G0 based on MTTF in descending order;
4:      select the first two available groups in G0;
5:      delete the selected groups in G0;
6:      merge the selected groups together as g'_j;
7:      delete N_gs spare(s) in g'_j;
8:      re-calculate the MTTF of g'_j;
9:      G0 = G0 ∪ {g'_j};
10:     update MTTF_network
11:     G' = G' ∪ {g'_j};
12: until MTTF_network ≥ MTTF_target
13: output G';
```

E. Discussion

For generality, all f-TSVs can be divided into three categories according to the signal transportation direction, i.e., the inbound f-TSV, the outbound f-TSV, and the bidirectional f-TSV. In this paper, we only target to the unidirectional f-TSVs (i.e., the inbound and outbound ones). Since the opposite direction of current in the bidirectional f-TSVs can compensate EM degradation to some degree, the unidirectional f-TSVs are normally more vulnerable to EM stress compared with the bidirectional ones. In addition, for the f-TSVs with extremely imbalanced bidirectional current, the conventional redundancy approach proposed in [19] can be used to extend their EM-related lifetimes.

V. RUNTIME TSV REPAIR

After obtaining the TSV groups, the next step is to extend the EM-related lifetime of each EM-vulnerable f-TSV during field operation. In this paper, a runtime TSV repair approach is proposed, consisting of: 1) recovery schedule and 2) repair architecture. By the repair architecture, all nonfaulty TSVs in each group, which include the assigned spare(s), are allowed to be temporarily deactivated and later reactivated according to a recovery schedule. This means that the repair architecture provides a configurable routing using the set of TSVs in each group. Therefore, the signals in each group are routed with a subset of TSVs, while the rest can recover from EM wear-out well by exploiting the recovery property. The detailed information is presented in this section.

A. Recovery Schedule

In this paper, two recovery scheduling approaches are considered: static scheduling and dynamic scheduling. If the workload can be estimated *a priori* or the changes in the workloads are limited, a static optimization can be utilized for achieving longer TSV lifetime at runtime. However, in many systems, the workload changes dynamically, and the set of running workloads might differ from one chip to other. This

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means that the amount of EM stress can change over time and from chip to chip. In this case, an on-line approach is desired to manage EM reliability.

1) Static Scheduling: In the static recovery scheduling, EM recovery can occur according to a predefined order at design-time. In this paper, a periodic recovery schedule is used, in which each TSV is deactivated at regular time intervals, these intervals remain the same over the lifetime operation of the chip. Consequently, according to the grouping ratio, each repair cycle can be split into multiple subcycles with the same duration $T_{\text{unit}}^{\text{stat}}$, which is a user-defined parameter. Generally, for a $(N_{gf}{:}N_{gs})$ group, the repair cycle of each TSV is divided into $(N_{gf} + N_{gs})$ subcycles, including active time $T_{\text{active}} = N_{gf} T_{\text{unit}}^{\text{stat}}$ and recovery time $T_{\text{recovery}} = N_{gs} T_{\text{unit}}^{\text{stat}}$. In each subcycle, N_{gs} TSV(s) is (are) deactivated for recovery, while the carried signal(s) (if any) will be rerouted through the nondeactivated s-TSV(s).

2) Dynamic Scheduling: The limitation of static scheduling is that it has to be designed for worst case workload over the entire lifetime and all instances of the chip if the running workloads cannot be estimated at design time. Typically, workload characteristics vary dynamically during operational lifetime, and from chip to chip, making it hard to predict workload, and the amount of EM stress, ahead of time. Then a static approach with constant recovery time in each repair cycle would not produce an optimal recovery schedule, tailored to the specific characteristics of the current running workload and the associated EM stress. To overcome this drawback, dynamic management of recovery time is required to achieve higher TSV lifetime and to reduce the reliability challenges caused by EM degradation.

Intuitively, the recovery time in each repair cycle should be dynamically changed according to the degree of EM wear-out of each TSV, which is highly dependent on the running workloads. For a fresh TSV, a larger duration of recovery time in each repair cycle (i.e., $T_{\text{unit}}^{\text{stat}}$) is more desirable, and the slower switching between activated and deactivated modes can reduce the performance degradation introduced by the repair mechanism. In contrast, with the increased amount of EM wear-out over time, the switching between the two modes should be speeded up (i.e., smaller $T_{\text{unit}}^{\text{stat}}$) in order to achieve a more complete EM recovery during current reversal [5]. In this paper, the EM-induced resistance increase is used as the wear-out indicator for each TSV, which can be monitored by the on-chip sensors at runtime [4], [20]. This way, the recovery time of each TSV is almost never constant, and varies with running workload as well as with the EM stress build-up of TSV. Since these sensors measure the change in the TSV resistance due to EM, they act in large time scales [2], [4]. This means that the update in the recovery schedule happens in very coarse time scales (e.g., weeks to months). Therefore, the long-term impact of workload stress can be compensated with this approach.

B. Repair Architecture

In this section, the repair architecture of the proposed runtime TSV repair solution is presented in detail, consisting of: 1) a reconfigurable routing network and 2) a recovery selector. For both static and dynamic scheduling, a reconfigurable logic circuitry should be included within each TSV group for signal rerouting. On the other hand, the recovery selector is specifically designed for different scheduling approaches.

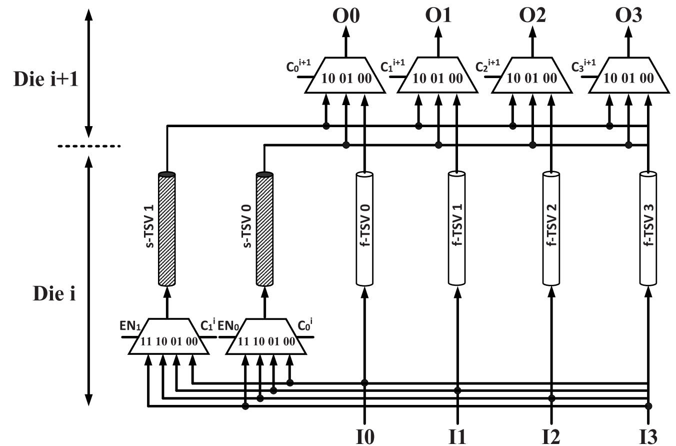

Fig. 5. Illustration of the reconfigurable routing network for a (4:2) TSV group consisting of four f-TSVs and two s-TSVs.

1) Reconfigurable Routing Network: In order to leverage the recovery effect for EM reliability improvement, each TSV needs to be provided with dedicated shut-off time in the field. Therefore, the signal carried by the deactivated f-TSV should be rerouted to its final destination through another nondeactivated TSV in the same group for maintaining the normal operation. In this paper, the assigned s-TSV(s) in each group is (are) served as an alternative signal path(s) for the deactivated f-TSV(s), and thus a reconfigurable logic for signal path rerouting should be included within each group.

In order to realize s-TSV sharing and routing reconfiguration, the proposed redundant scheme in [19] is implemented in each group. Here, a (4:2) TSV group is illustrated in Fig. 5 as an example, in which two dedicated s-TSVs are assigned to a partitioned group consisting of four f-TSVs. As a symmetric scheme, each group needs to be configured both at the receiver and transmitter. To this end, reconfiguration circuitries (i.e., MUXes) are added to the two ends of each TSV, and every single input of the group can be selected and transmitted over the dedicated lines provided by the assigned s-TSVs when its original f-TSV is deactivated. In this way, all TSVs (including the assigned s-TSVs) can operate either in active mode or in recovery mode, and transition between them according to a recovery schedule.

2) Recovery Selector: As shown in Fig. 5, the selection of deactivated TSVs in each repair subcycle is determined by the control signal of each MUX. In other words, the so-called "recovery schedule" in this context is a set of MUX control signals, which can be changed during field operation.

The static recovery schedule can be fixed at design-time based on the worst case workload analysis. For example, for the (4:2) group illustrated in Fig. 5, we list its corresponding static schedule, as shown in Table I. Here, "EN" is the enable pin of all the MUXes at receiver. When EN is set to 0, the MUX is disabled, and the corresponding s-TSV will operate in recovery mode. Otherwise, different f-TSVs

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TABLE I

STATIC RECOVERY SCHEDULE FOR A (4:2) TSV GROUP. HERE, A: ACTIVE MODE, R: RECOVERY MODE, FI: F-TSV I, SJ: S-TSV J

TSV	Subcycle_1	Subcycle_2	Subcycle_3	Subcycle_4	Subcycle_5	Subcycle_6
f0	A	**R**	**R**	A	A	A
f1	A	A	**R**	**R**	A	A
f2	A	A	A	**R**	**R**	A
f3	A	A	A	A	**R**	**R**
s0	**R**	A	A	A	A	**R**
s1	**R**	**R**	A	A	A	A
Control signals of MUXes						
EN_0	0	1	1	1	1	0
EN_1	0	0	1	1	1	1
C_0^i	XX	00	00	01	10	XX
C_1^i	XX	XX	01	10	11	11
C_0^{i+1}	00	01	01	00	00	00
C_1^{i+1}	00	00	10	01	00	00
C_2^{i+1}	00	00	00	10	01	00
C_3^{i+1}	00	00	00	00	10	10

will be deactivated according to the control signals. This way, each TSV is deactivated at regular time intervals and provided with uniform recovery time. Moreover, since it is unnecessary to control the MUXes from outside for the static scheduling, the recovery selector here is nothing but a small finite-state machine (FSM), which generates the control signal for each MUX internally. Since we assume that all TSV groups receive the same control signals, the FSM can be shared between different groups across the entire chip for reducing area overhead.

In order to realize a dynamic recovery schedule, a metric for quantifying the amount of EM stress on a TSV is necessary. As discussed in Section V-A2, the EM-induced resistance increase is used in this paper to determine the recovery time of each repair cycle. Here, the duration of repair subcycle for dynamic repair approach $T_{\text{unit}}^{\text{dyn}}$ can be varied with the EM-induced resistance increase as follows[2]:

$$T_{\text{unit}}^{\text{dyn}} = T_{\text{unit}}^{\text{stat}} \times \left[1 + \alpha(M-1)\left(\lfloor \frac{\Delta R_{\text{TSV}}^{\text{EM}}(t)}{R_{\text{TSV}}^{\text{FC}}} \rfloor - \frac{1}{2}\right)\right] \quad (2)$$

where $R_{\text{TSV}}^{\text{FC}}$ is the EM failure criterion of TSV (discussed in Section IV-A). In this paper, the entire range of EM-induced TSV resistance increase between 0 and $R_{\text{TSV}}^{\text{FC}}$ is divided by M predefined threshold values into $M-1$ intervals, and the difference of $T_{\text{unit}}^{\text{dyn}}$ between two neighboring intervals is $\alpha \times T_{\text{unit}}^{\text{stat}}$, where α is a user-defined parameter. This way $T_{\text{unit}}^{\text{dyn}}$ can be varied with the EM-induced resistance increase over time (i.e., $\Delta R_{\text{TSV}}^{\text{EM}}(t)$).

In order to obtain $\Delta R_{\text{TSV}}^{\text{EM}}(t)$, the on-chip aging sensor [4], [20] can be equipped with f-TSV at design-time. However, as a long-term reliability issue, $\Delta R_{\text{TSV}}^{\text{EM}}(t)$ becomes observable only after a long time period (e.g., weeks to months) [2]. In addition, the resolution of such EM-based sensors [4], [20] is limited, and thus, only a pretty significant change can be detected by them. As a result, the update of recovery schedule (i.e., the update of $T_{\text{unit}}^{\text{dyn}}$ in each repair cycle) occurs in a large time scale. Since only EM-vulnerable f-TSVs are targeted in this paper, all TSVs would be at the similar stage of EM-induced resistance evolution during each update. Therefore, it is unnecessary to monitor each f-TSV for capturing this long-term effect and distinguishing EM stress differences across the f-TSV grid. In contrast, only one sensor is equipped with the entire chip in order to monitor the degree of EM degradation on-line. A few more sensors can be used to avoid variations and improve information accuracy. In addition, for a block-level 3-D design, a "one sensor per block" strategy can be adopted to handle the scenario that the utilization rate of each intellectual property (IP) block is significantly different. However, for both of the two design granularities, the area overhead introduced by dynamic repair approach is negligibly small due to the limited number of equipped aging sensors.

C. Overhead Analysis

For both the static and dynamic scheduling approaches, the delay and hardware overheads introduced by the proposed repair solution are analyzed as follows.

1) Delay Overhead: For both the static and dynamic scheduling, the delay of control signal generation is negligible (either using small FSM or using off-chip co-processor). Moreover, due to the fact that TSV latency is very small [21], here delay overhead is mainly determined by rerouting wire and reconfiguration circuitries (i.e., MUXes). Although the former one can be minimized by optimal s-TSV assignment based on the given placement of s-TSVs, the inserted MUXes can introduce more significant delay overheads. For an f-TSV f_i in a $(N_{gf}:N_{gs})$ group, its rerouting logic-induced delay overhead is

$$D(f_i) = D_{\text{MUX}_{N_{gf}-\text{to}-1}} + D_{\text{MUX}_{(N_{gs}+1)-\text{to}-1}} \quad (3)$$

[2]Here, we assume that M is an odd number.

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where $D_{\text{MUX}_{N\text{-to-}1}}$ is the propagation delay of an N-to-1 MUX, which can be calculated as

$$D_{\text{MUX}_{N\text{-to-}1}} = \log_2(N) D_{\text{MUX}_{\text{2-to-1}}} \quad (4)$$

However, using different logic implementation, the actual value of $D_{\text{MUX}_{N\text{-to-}1}}$ can be reduced. According to (3) and (4), it is desirable to partition f-TSVs into smaller groups (i.e., smaller N_{gf} with respect to the same N_{gs}) in order to reduce the overhead. Note that, for those EM-vulnerable f-TSVs on the critical paths, their timing slacks can be impacted slightly by the added rerouting logic circuitry and its introduced delay overhead. However, this penalty is unavoidable since the EM-induced timing failures can be more severe without the proposed repair solution.

2) Area Overhead: The area overhead can be introduced by: a) reconfiguration routing network and b) recovery selector. Here, we analyze the corresponding overheads for both static and dynamic scheduling approaches as follows.

a) Static scheduling: For static scheduling approach, recovery schedule is generated by a small FSM internally since it can be fixed at design-time, incurring negligible area overhead. Therefore, the area overhead is dominated by the assigned s-TSVs and added MUXes [3] in the reconfiguration routing network. After implementing TSV grouping with GR $= N_{gf}{:}N_{gs}$, the total area overhead of all groups can be represented as[3]

$$A = N_{gs}|\mathbf{F}|[A_s/N_{gf} + (2 - 1/N_{gf})A_{\text{MUX}_{\text{2-to-1}}}] \quad (5)$$

where A_s is the area of an s-TSV and $A_{\text{MUX}_{\text{2-to-1}}}$ is the area of a 2-to-1 MUX. Therefore, for a fixed N_{gs}, it is more preferred to partition f-TSVs into larger groups (i.e., larger N_{gf}) to reduce the area overhead.

b) Dynamic scheduling: For dynamic scheduling approach, the same reconfigurable routing network is used as the static one, and the only difference here is the area overhead introduced by recovery selector (i.e., the aging sensor equipped with TSV). However, since only a few sensors are used for the entire chip (at most one per IP block), the overall overhead is very negligible.

VI. Numerical Results and Discussion

A. Experimental Setup and Implementation Flow

For our simulations, six 3-D benchmark designs selected from OpenCore benchmark suite [22] were used, including *des_perf–i*, *cf_rca_16–i*, and *cf_fft_256_8–i* (i = 2, 4). Here, *i* is the number of stacked dies in each design. Given the netlist of each design, Cadence SoC Encounter was used to generate layout file using the Nangate 45-nm library [23]. Here, f-TSVs were placed regularly across each die with a 10-μm pitch to form a grid [24], and s-TSVs were placed at the edges of the f-TSV grid with the same pitch [12]. For both f-TSVs and s-TSVs, the total TSV cell size including the keep-out zone is 8.4 μm, which corresponds to six standard cell rows [25].

Given a grouping ratio GR $= N_{gf}{:}N_{gs}$, the proposed TSV grouping technique was conducted on the generated layout files of each design to obtain TSV groups. Afterward, based on a periodic recovery schedule with a user-defined T_{unit}, the EM model proposed in [11] can be used to estimate the MTTF of each group considering transient recovery effect. To this end, the power/thermal characteristics of each TSV in the group need to be generated. After creating a top-level Verilog netlist for the design, post synthesis simulation was performed in Modelsim with a testbench containing 10^5 random input vectors. In this way, the switching activity of each f-TSV can be extracted. Moreover, the generated switching activity interchange format file was forwarded to power compiler in order to obtain the power consumption of each cell. Based on this information and layout files, the experienced temperature of each TSV can be estimated using the 3-D hotspot [26]. In order to obtain the timing slack of each repair-critical TSV, the standard parasitic exchange format (SPEF) file of each die was extracted by performing parasitic extraction after routing. In addition, a top-level Verilog file with the interconnections among dies and a top-level SPEF file with the TSV parasitics were created. Afterward, all netlist and parasitic information are fed into timing analysis tool (e.g., Synopsys Primetime) to obtain timing slack value for each f-TSV.

B. Impact of T_{unit}^{stat} and GR on Repair Solution

There are two user-defined parameters in the proposed approach, namely, T_{unit} and GR. In this section, we investigate their impact on the generated repair solution, and undertake the tradeoff analysis between reliability improvement and the corresponding overhead.

1) Impact of T_{unit}^{stat}: $T_{\text{unit}}^{\text{stat}}$ is the duration of each subcycle in the repair cycle during in-field repair for a static approach. A larger $T_{\text{unit}}^{\text{stat}}$ implies longer recovery time of deactivated TSVs in each repair cycle, but also indicates more EM degradation of the TSVs operating in active mode. As discussed in Section V-A1, $T_{\text{unit}}^{\text{stat}}$ is assumed to be constant over time for a static recovery scheduling. Here, we present the impact of $T_{\text{unit}}^{\text{stat}}$ on the generated static repair solution in terms of achieved MTTF.

Here the proposed repair solution with static scheduling were conducted on both *des_perf–2* and *cf_fft_256_8–2*, and the grouping ratio GR = 3:1. Fig. 6 illustrates the relationship between the achieved MTTF and $T_{\text{unit}}^{\text{stat}}$. As shown, for both of the two benchmarks, a repair solution with short $T_{\text{unit}}^{\text{stat}}$ (e.g., 10^{-3} s) is incapable of fully exploiting EM recovery effect, which results in an extremely short lifetime. With the increased $T_{\text{unit}}^{\text{stat}}$, the generated repair solution attempts to strike a balance between recovery and degradation in each repair cycle, and achieve it at different $T_{\text{unit}}^{\text{stat}}$ for different benchmarks. However, with the further increase of $T_{\text{unit}}^{\text{stat}}$, the achieved balance becomes disturbed as the EM degradation in each repair cycle can no longer be compensated by recovery effect. As a result, the achieved MTTF becomes lower and saturates finally.

2) Impact of GR*:* Grouping ratio GR $= N_{gf}{:}N_{gs}$ denotes the ratio between the number of f-TSVs and s-TSVs in each group. On the one hand, for a fixed N_{gs}, the partitioning with less N_{gf} leads to better EM recovery in each repair

[3]Here we assume that $|\mathbf{F}|$ is divisible by N_{gf}.

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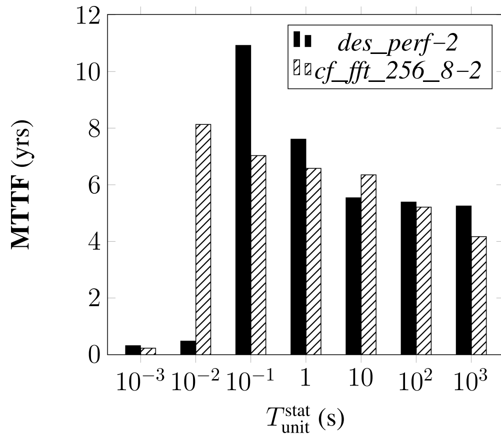

Fig. 6. Relationship between the achieved MTTF and T_{unit}^{stat}.

cycle and smaller delay overhead introduced by rerouting logic circuitry (as discussed in Section V), but also results in higher area overhead according to (5). On the other hand, for the same GR, the different N_{gs} can also impact the generated repair solution in terms of MTTF and overhead.

In order to evaluate the impact of GR, the proposed repair solution with static recovery scheduling was performed on *des_perf-2*. The duration of each repair subcycle $T_{unit} = 0.1$ s. First, for a fixed $N_{gs} = 1$, N_{gf} was varied from 2 to 4, and the achieved MTTF and the corresponding overhead can be obtained using the proposed approach with different GR. Afterward, three different cases with GR =2:1, 4:2, 6:3 were considered, in which N_{gs} was varied from 1 to 3 but GR always equals 2. For all the cases, we report the achieved MTTF and the overhead in both area and delay. Here the area overhead is presented in terms of the number of assigned s-TSVs and added MUXes. Since the rerouting wire-induced delay overhead is highly dependent on the given placement of s-TSVs, we only focus on the logic-induced delay overhead here, and report the average value of all the groups.

The results are listed in Table II. Here ΔD is the average delay overhead of all groups in design introduced by repair solution, and ΔA is the percentage of area introduced by repair solution with respect to total cell area including f-TSV and logic cells. As shown, for a fixed N_{gs}, we can achieve a higher MTTF with smaller rerouting logic-induced delay overhead by partitioning less N_{gf} into each group, but also results in larger area overhead. Note that here reducing the number of s-TSVs can save far more area compared with the area overhead introduced by MUXes. Moreover, for the same GR, assigning more s-TSVs to each group can provide longer recovery time for each repair cycle, which improves lifetime reliability more significantly. However, the penalty is the increased area and delay overheads. Therefore, the desirable GR can be determined by the constraints of timing slacks of repair-critical TSVs (i.e., the target clock period).

C. Benefit of Nonuniform TSV Grouping

As discussed in Section IV-D, for a target MTTF, a repair solution using nonuniform TSV grouping can achieve a better tradeoff between reliability improvement and area overhead. Therefore, a greedy group-merge algorithm is proposed to divide all EM-vulnerable f-TSVs into several groups with varying N_{gf}. In this section, we show the superiority of the proposed nonuniform grouping approach when targeting the specified MTTF of f-TSV network.

TABLE II
TRADEOFF ANALYSIS BETWEEN THE ACHIEVED MTTF AND OVERHEAD FOR DIFFERENT GRs

Grouping ratio	MTTF (yrs)	Overhead	
		ΔD (ps)	ΔA (%)
2:1	11.81	87.717	4.23
3:1	10.92	106.159	2.95
4:1	9.69	116.462	2.24
4:2	12.74	132.260	4.47
6:3	13.67	175.045	5.01

The experiment was conducted on all six benchmark designs as follows. First, the proposed TSV repair solution with static recovery schedule and uniform TSV grouping was performed. Here GR = 2:1 and T_{unit} = 0.1 s. Second, the proposed greedy group-merge algorithm was performed under the timing constraints of EM-vulnerable f-TSVs until the target MTTF ($MTTF_{target}$) is achieved. Here, $MTTF_{target}$ is a user-defined parameter, which can be set according to different application requirements.

The simulation results are presented in Table III. Here ΔD is the delay overhead introduced by repair solution with respect to critical path delay (CPD), and ΔA is the percentage of area introduced by repair solution with respect to total cell area including f-TSV and logic cells. Compared to the repair solution with uniform TSV grouping, the nonuniform solution can achieve the same $MTTF_{target}$ (which is less than the optimized one of the uniform solution), but introduce less area overhead. According to our simulation results, the improvement can be achieved by 15.19% in average. The penalty here is the increased delay overhead, which comes from: 1) increased rerouting signal path and 2) the more complicated fan-out structure of the MUX circuitry. However, compared with the CPD of each design, this delay overhead introduced by repair solution is very limited. In addition, since the specified timing slack of each f-TSV is considered during nonuniform TSV grouping, the timing correctness can still be guaranteed with the increased delay overhead. Therefore, a better tradeoff between timing performance and area overhead can be achieved by the proposed approach for the area-critical systems.

D. Comparison With Conventional Reactive Repair Approach

We compare our proposed proactive repair approach with the conventional reactive one [3], and the results in terms of achieved MTTF are listed in Table IV. Here, $|\mathbf{F}|$ is the number of EM-vulnerable f-TSVs in each design, and ΔA is the percentage of area introduced by repair solution with respect to total cell area including f-TSV and logic cells. In order to perform a fair comparison, the same power/thermal

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TABLE III

COMPARISON BETWEEN THE UNIFORM AND NONUNIFORM APPROACHES WHEN TARGETING THE SAME MTTF VALUE OF F-TSV NETWORK $MTTF_{TARGET}$

Benchmark	CPD (ns)	$MTTF_{target}$ (yrs)	$MTTF_{achieved}$ (yrs)		ΔD (%)			ΔA (%)		
			Uniform	Non-uniform	Uniform	Non-uniform	Change (%)	Uniform	Non-uniform	Change (%)
des_perf–2	1.75	10	11.81	10.33	7.89	8.81	+11.66	4.23	3.82	-9.69
cf_rca_16–2	2.31	8	9.71	8.14	6.69	7.63	+14.05	1.84	1.60	-13.04
cf_fft_256_8–2	2.92	6	8.51	6.19	5.71	6.35	+11.21	2.23	1.94	-13.00
des_perf–4	1.93	8	9.55	8.21	6.68	7.84	+17.37	6.24	5.09	-18.43
cf_rca_16–4	2.51	7	8.93	7.13	5.89	6.80	+15.45	3.38	2.50	-26.04
cf_fft_256_8–4	3.54	6	8.01	6.23	4.43	5.27	+18.96	2.44	2.06	-15.57
Average							+14.78			-15.19

TABLE IV

COMPARISON BETWEEN THE PROPOSED PROACTIVE APPROACH AND THE CONVENTIONAL REACTIVE APPROACH [3]

Benchmark	$\|\mathbf{F}\|$	Grouping ratio	ΔA (%)	$MTTF_{achieved}$ (yrs)		Improvement (X)
				Proactive	Reactive [3]	
des_perf–2	55	2:1	4.23	11.81	1.62	7.29
		3:1	2.95	10.92	0.98	11.14
		4:1	2.24	9.69	0.87	11.14
cf_rca_16–2	87	2:1	1.84	9.71	3.51	2.78
		3:1	1.25	9.14	3.32	2.75
		4:1	0.97	8.93	2.94	3.04
cf_fft_256_8–2	235	2:1	2.23	8.51	2.21	3.85
		3:1	1.53	8.13	2.04	3.99
		4:1	1.18	7.78	1.78	4.37
des_perf–4	183	2:1	6.24	9.55	1.23	7.76
		3:1	4.26	9.01	0.81	11.12
		4:1	3.30	8.65	0.71	12.18
cf_rca_16–4	218	2:1	3.38	8.93	3.03	2.95
		3:1	2.33	8.21	2.89	2.84
		4:1	1.80	7.99	2.72	2.94
cf_fft_256_8–4	314	2:1	2.44	8.01	2.11	3.80
		3:1	1.68	7.75	1.57	4.94
		4:1	1.30	7.03	1.42	4.95
Average						5.77

profiles and recovery-aware EM model are used during TSV lifetime estimation. The only difference between the two schemes is that $T_{\text{unit}}^{\text{stat}} = 0$ for the reactive approach. As shown, the proposed approach with static recovery scheduling can increase MTTF of the TSV grid by up to 12× relative to the reactive method. Moreover, the number of EM-vulnerable f-TSVs $|\mathbf{F}|$ and the area overhead rate ΔA (in terms of percentage of area introduced by s-TSVs and MUXes with respect to total chip area) are also listed in the table. According to our results, the area overhead introduced by the proposed repair solution is pretty small, which can be negligible for a large design. Note that, since here we assume that the same reconfiguration network is used in both proactive and reactive approaches, the proposed technique does not increase the delay and area overheads compared to the baseline, but can achieve a higher MTTF.

E. Comparison Between Static and Dynamic Proactive Repair Approaches

Until now, we assumed that the executed workloads can be estimated *a priori* or the changes in the workloads are limited over time, and thus, a static proactive repair approach with a fixed recovery interval is appropriate in this context. However, in many systems, the workload characteristics vary dynamically in the field, and the set of executed workloads might differ from chip to chip. Therefore, the EM stress build-up of each TSV should be taken into account during recovery scheduling in order to achieve a longer EM-related lifetime, and a dynamic repair approach with varied recovery time is proposed in Section V-A2.

In order to evaluate the superiority of the proposed dynamic approach compared to the static one, the experiments were conducted on each benchmark with different GR $= N_{gf}{:}N_{gs}$ as follows. For each design, two sets of running workloads are considered (i.e., "normal" and "heavy" workloads), respectively. Here, the "normal" workload is the same with the one used in Section VI-D, in which the current density of each f-TSV is extracted from a testbench containing 10^5 random input vectors (as discussed in Section VI-A). On the other hand, a "heavy" workload is used to simulate a more aggressive application scenario, in which the current density of each TSV equals to twice the corresponding value

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TABLE V
COMPARISON BETWEEN THE PROPOSED STATIC AND DYNAMIC PROACTIVE REPAIR APPROACHES

Benchmark	Grouping ratio	$MTTF_{achieved}$ (yrs)			Improvement (X)
		normal+static	heavy+static	heavy+dynamic	
des_perf−2	2:1	11.81	4.15	17.85	4.30
	3:1	10.92	3.97	14.49	3.65
	4:1	9.69	3.42	11.21	3.28
cf_rca_16−2	2:1	9.71	4.03	9.56	2.37
	3:1	9.14	3.82	8.77	2.30
	4:1	8.93	3.07	8.14	2.65
cf_fft_256_8−2	2:1	8.51	3.81	8.82	2.31
	3:1	8.13	3.06	8.21	2.68
	4:1	7.78	2.87	8.04	2.80
des_perf−4	2:1	9.55	3.25	14.45	4.45
	3:1	9.01	3.03	12.86	4.24
	4:1	8.65	2.85	10.31	3.62
cf_rca_16−4	2:1	8.93	2.94	8.89	3.02
	3:1	8.21	2.77	8.16	2.95
	4:1	7.99	2.41	8.02	3.33
cf_fft_256_8−4	2:1	8.01	2.45	8.11	3.31
	3:1	7.75	2.21	7.94	3.59
	4:1	7.03	2.04	7.41	3.63
Average					3.25

in the “normal” case. Afterward, three sets of results in terms of the achieved MTTF were extracted and reported in Table V.

First, the static repair approach was applied for different benchmarks with the “normal” running workloads (i.e., “normal + static” case in Table V). Next, considering the “heavy” workload for each benchmark, the static and dynamic repair approaches were used, respectively, and the achieved MTTF values are listed in the fourth and fifth columns of Table V (i.e., “heavy + static” and “heavy + dynamic” cases). According to the results listed in Table V, the achieved MTTF of the “heavy + static” case is significantly reduced compared to the one of the “normal + static” case for each benchmark due to the increased current density and temperature in the “heavy” workloads. This means that under heavy utilization, the static approach may not be able to fully compensate the EM degradation. However, compared to the static repair approach, the dynamic one with varied $T_{\text{unit}}^{\text{dyn}}$ (i.e., the “heavy + dynamic” case) can achieve a higher MTTF, and the improvement can be up to 4.45× according to our simulation results. In this paper, $T_{\text{unit}}^{\text{dyn}}$ of each repair cycle can be obtained by (2), in which $M = 11$ and $\alpha = 0.1$.

F. Discussion

In this paper, we limit our scope only to the signal TSVs. However, as an integral part of power distribution networks in 3-D ICs, power/ground (P/G) TSVs are more susceptible to EM degradation compared to signal TSVs as they experience large amount of unidirectional currents. In [27], a repair solution has been proposed to enhance the EM-related lifetime reliability of P/G TSV networks by leveraging EM recovery effect.

In this paper, we assume that each EM-vulnerable f-TSV and its assigned s-TSV belongs to different interconnect trees. Here, the “interconnect tree” is the elemental EM reliability unit, which is a multibranch interconnect segment consisting of a continuously connected, highly conductive metal lines terminated by diffusion barriers and located within the single level of metallization [28]. However, in the opposite scenario, in which multiple TSVs within the same metal layer are connected, there is a complex correlation between voiding times in the multivoid case due to the interplay between growth kinetics of voids and current redistribution among the TSVs [29]. This more general scenario will be considered as part of the future work.

VII. CONCLUSION

In this paper, we have proposed a proactive repair approach to combat EM in TSVs by taking the use of the EM recovery effect. Applied to 3-D benchmark designs, our proactive approach improves the lifetime reliability of TSVs susceptible to EM failure by approximately 12× over the conventional reactive one with less area overhead, even using simple recovery scheduling. Moreover, a dynamic recovery approach with negligible overhead has been proposed to further improve the TSV lifetime reliability for a more realistic operation condition.

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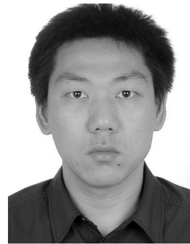

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