Compact Thermal Modeling For Package Design With Practical Power Maps *

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ABSTRACT
This paper proposes a new thermal modeling method for package design of high-performance microprocessors. The new approach builds the thermal behavioral models from the given accurate temperature and power information by means of the subspace method. The subspace method, however, may suffer predictability problem when the practical power is given as a number of power maps where power inputs are spatially correlated. We show that the input power signal needs to meet some dependency requirements to ensure model predictability. We develop a new algorithm, which generates independent power maps to meet the spatial rank requirement and can also automatically select the order of the resulting thermal models for the given error bounds. Experimental results validates the proposed method on a practical microprocessor package constructed via COMSOL software under practical power signal inputs.

1. INTRODUCTION
Temperature has become a major concern for high performance microprocessor and package design as more devices are integrated on a chip. Thermal management and related design problems continue to be identified by the Semiconductor Industries Association Roadmap [1] as one of the five key challenges during the next decade for achieving the projected performance goals of the industry. Thus, accurate and efficient thermal modeling and analysis is vital for the thermal-aware chip and package designs to improve performance, reliability, power reduction, and online temperature regulation techniques [15, 3, 17].

The traditional bottom-up approaches including FEM (finite element), FDM (finite difference), and computational flow dynamics (CFD) based methods were widely used for thermal modeling and analysis in the past. For compact modeling, many existing approaches try to use thermal resistors and capacitors with fixed topology networks subject to different thermal boundary conditions [10, 4, 2]. However, the accurate RC values of elements, especially for complex geometries and boundary conditions are difficult to determine, and the optimization against the field numerical or analytic results [6, 14] and measured data are usually required [16].

For thermal modeling at the package level, existing work on HotSpot [8, 17] attempts to solve this problem by generating the compact thermal model in a bottom-up manner based on processor and package structures. However, such compact models may suffer from accuracy loss, and have to be calibrated with hardware if more accurate models are required. Recently, top-down behavioral thermal modeling methods have been proposed using the matrix pencil method [11] and the subspace method [5]. The subspace method, though, may suffer from the lack of predictability problems in general [12, 9], especially when the input power is given as series of power maps where the input signal is highly correlated. The reason is that it is difficult to distinguish the contribution from specific inputs when all the inputs have the same or similar transient waveforms.

In this paper, we present a new subspace-based thermal modeling techniques trained by more practical power maps for package level design space exploration of high-performance microprocessors. First, we show that there exists a required rank of the input power maps (their power signal matrix) to avoid the predictability problems in subspace method. Second, we develop a new modeling algorithm to automatically select the order of the thermal models for given error bounds. Experimental results validates the proposed method on a practical microprocessor package constructed via commercial COMSOL software under practical power signal inputs.

2. THERMAL MODELING PROBLEM CONSIDERING POWER MAPS
We first present how the power inputs are modeled in our problem. A microprocessor chip is partitioned into $p = n \times m$ power grids as shown in Fig. 1, where each square power grid has a power source as an input and its measured temperature at its adjacent 4 corners as outputs. We can abstract this power grid model into a discrete linear system with $p = n \times m$ power inputs and q temperature outputs as shown in Fig. 2. The $n \times m$ power input distribution at one time instance is defined as a *power map*, which can be measured or computed practically.

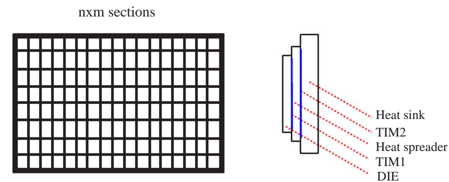

Figure 1: Partitioned chip and package

We can abstract this $p = n \times m$ model into a discrete linear

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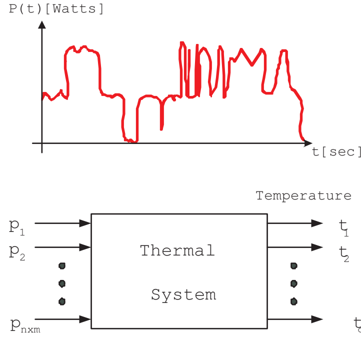

Figure 2: The abstracted model system and correlated power inputs

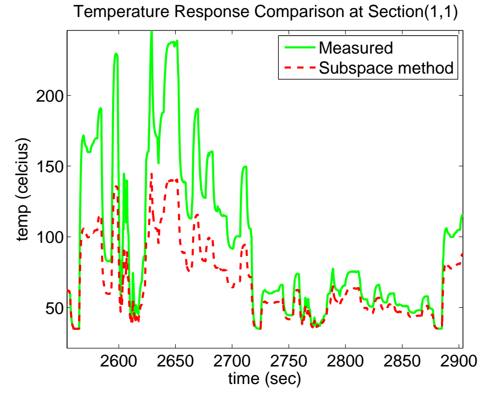

Figure 3: Transient temperature response of the system trained with one highly correlated power inputs

system with p inputs and q outputs as shown in Fig. 2. The inputs are the power traces of all the cores, while the outputs are the measured temperatures.

$$\begin{aligned} x(t+1) &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Du(t), \end{aligned} \tag{1}$$

where $A \in \mathbb{R}^{l \times l}$ is a stable matrix, l is the number of states. $B \in \mathbb{R}^{l \times p}$, $C \in \mathbb{R}^{q \times l}$, and $D \in \mathbb{R}^{q \times p}$. The input vectors $u(t) \in \mathbb{R}^{p \times 1}$ are the measured power input traces and output vectors $y(t) \in \mathbb{R}^{q \times 1}$ are the temperature responses. With s input samples $u(t_i)$ and s output samples $y(t_i)$ where $i = 1, 2, \ldots, s$, the problem at hand is how to generate state matrices A, B, C, and D, where D is typically considered a matrix of zeros.

For all the $n \times m$ power map, they may be highly correlated as mentioned before. In an extreme case, all the power input waveforms are exactly the same and they are only different by their magnitudes. Fig. 2 (top) shows a typical power input waveforms. Their spatial difference in magnitudes essentially is described by the *power map* of the chips. The magnitude (power map) distributions can be defined by a function and applied in a practice setting to a testing package (called testing vehicle). Such magnitude distribution is called *power map configuration* in this paper.

Such highly correlated power inputs, however, will lead to poor predictability by using the subspace identification method [13, 9]. Fig. 3 show that the waveforms produced by the model trained by highly correlated power inputs (one power map configuration), where the results from model and from original temperature does not match well.

3. REVIEW OF SUBSPACE METHODS FOR SYSTEM IDENTIFICATION

Given input $u(t)$ and output $y(t)$, subspace identification method identifies the state matrices A, B, C, and D of (1). The subspace identification basically tries to first identify the system states (Kalman states), then the state matrices will be obtained by the least square based optimization method [9]. There are several implementations such as the Ho-Kalman' method, the MOSEP method and the N4SID (Numerical algorithms for Subspace System IDentification) method [12]. In this paper, we apply the widely used N4SID method for this system identification problem.

Defining the input Hankel matrix of an l-order system as

$$U_{a|b} := \begin{bmatrix} u(a) & u(a+1) & \cdots & u(a+N-1) \\ u(a+1) & u(a+2) & \cdots & u(a+N) \\ \vdots & \vdots & \vdots & \vdots \\ u(b) & u(b+1) & \cdots & u(b+N-1) \end{bmatrix} \in \mathbb{R}^{(b-a+1)p \times N} \tag{2}$$

where a, b and N are the time points, u is the input power matrix. The input signal of the subspace methods must satisfy the so called *persistently exciting condition*. That is $\text{rank}(U_{0|2k-1}) = 2pk$ for a p-port system assuming the number of columns of the Hankel matrix N is sufficiently large in the N4SID method [9, 13].

Generally speaking, the input signal is *qualified* if a unique system can be identified from the given input and output data. Consider the FIR (finite impulse response) model

$$y(t) = \sum_{i=0}^{2k-1} q_i u(t-i) \tag{3}$$

where $q_0, q_1, \cdots, q_{2k-1} \in \mathbb{R}^{p \times p}$ are the system impulse responses. Denote

$$Q_{2k-1} := [\ q_{2k-1}, q_{2k-2}, \ldots, q_0\ ] \tag{4}$$

and the system identification comes down to determining Q_{2k-1} using the input and output data.

From (3), we readily get

$$Y_{2k-1|2k-1} = Q_{2k-1} U_{0|2k-1} \tag{5}$$

where $U_{0|2k-1} \in \mathbb{R}^{2Nk \times N}$. This is a least square problem and Q_{2k-1} can be uniquely solved when $U_{0|2k-1}$ has full row rank [7].

$$\text{rank}(U_{0|2k-1}) = 2pk \tag{6}$$

4. NEW THERMAL MODELING METHOD FOR CORRELATED POWER INPUTS

4.1 Spatial rank requirement

In general, the *persistently exciting*, or PE condition can be easily satisfied for a MIMO dynamic system when all the input signals are uncorrelated. However, if those signals are highly correlated, the PE condition may not be easily

satisfied, which leads to poor predictability of the resulting models as shown in Fig. 3. Specifically, consider a 2-input system. We assume that all the inputs have exactly the same time domain waveform and denote it as $f(t)$. The difference in magnitudes are represented by another spatial function $g(x)$ in 1-D space (x-axis) for simplicity, which represents the 1-D power map configuration. The i-th input sample for such 2-input system is

$$u(i) = \begin{bmatrix} g(x_0)f(t_i) \\ g(x_1)f(t_i) \end{bmatrix} \tag{7}$$

We further define the i-th block row in the input Hankel matrix as

$$U_i = \begin{bmatrix} g(x_0)f(t_i) & g(x_0)f(t_{i+1}) & \cdots & g(x_0)f(t_{i+N-1}) \\ g(x_1)f(t_i) & g(x_1)f(t_{i+1}) & \cdots & g(x_1)f(t_{i+N-1}) \end{bmatrix} \tag{8}$$

The input Hankel matrix can be expressed as

$$U_{0|2k-1} = [U_0^T, \quad U_1^T, \quad ... \quad U_{2k-1}^T]^T \tag{9}$$

The *persistently exciting* condition is satisfied when $U_{0|2k-1}$ has full row rank, that is $\text{rank}(U_{0|2k-1}) = 4k$ for this 2-input case. However, it is clear that the two rows in U_i are linearly dependent, which makes $\text{rank}(U_{0|2k-1}) = 2k$ and fail to satisfy the *persistently exciting* condition.

In order to make the input Hankel matrix $U_{0|2k-1}$ full row rank, we need to make the i-th block row U_i full row rank, assuming $N \gg k$. For this 2-input example case, we can achieve this by simply introducing another power map configuration. Now we have two configurations, g_1 and g_2. The i-th block row U_i is shown in (10) on top of the next page, where $i < m < i + N - 1$. The two dimensional case can be generalized into higher dimensions with g_i as a function of two spatial variables x and y. By calling the row rank of i-th block row U_i the *spatial rank* of input signals, we have the following proposition.

PROPOSITION 1. *For p-input MIMO dynamic systems with correlated input signals, the spatial rank of input signals must be equal to p to satisfy the persistently exciting condition in the subspace method.*

To meet such spatial rank requirement for input signals, we have to generate multiple *independent* power map configurations. In this next section, we show how this can be achieved in a systematic way.

4.2 Orthogonal set of power map configurations

In this section, we show how to automatically generate independent power map configurations to meet the PE requirement as mentioned in previous subsection. It is necessary since the number of inputs can be large.

Take the 1-D example again, if $x \in [0, L]$, a set of orthogonal functions over the interval $[0, L]$ can serve as the systematic solution for the independent and robust configurations. The orthogonal function set $\{g_1, g_2, \ldots, g_N\}$ satisfies

$$\int_0^L g_i(x)g_j(x)\,dx = \begin{cases} 0 & i \neq j \\ \|g_i(x)\|^2 & i = j \end{cases} \tag{11}$$

Note that one is free to choose any set of orthogonal functions. In this paper, $sin(i\pi x/L)$, $i = 1, 2, 3, \ldots$, is used as the arbitrary orthogonal function on $x \in [0, L]$. In our application, we choose i up to p, the number of ports, and L as the maximum of x dimensions.

4.3 New thermal modeling algorithm with automatic order selection - ThermSubCP

Now we are ready to introduce our new thermal modeling algorithm considering the highly correlated power inputs – *ThermSubCP*. Once we generate all the independent power map configurations, we need to generate two transient power sequences – one for training and one for validation. For each power map configuration, we basically divide the given transient power input waveform into two parts. The first part will be used for the training and the second part will be used for the validation. To test the predictability of the models, we will also add some additional power maps, which are not used for training. For instance, suppose we have a 4-input MIMO system, then we need 4 independent power maps with transient power inputs denoted as P_1, P_2, P_3, P_4. Then we split $P_1 = [P_{11}, P_{12}]$ into two parts in time scale. We do the same for other 3 power inputs. Then the training sequence will be $[P_{11}, P_{21}, P_{31}, P_{41}]$, while the validation sequence will be $[P_{12}, P_{22}, P_{32}, P_{42}, P_{a1}, P_{a2}]$, where P_{a1}, P_{a2} are the additional power inputs in power maps not used for training.

ThermSubCP also tries to automatically select the proper order of the models to satisfy the given error bounds by gradually increasing the order of the models until the accuracy in the validation phase is met. In our implementation, we use the maximum of the mean errors and their variances (standard deviation) over all the transient responses for all the outputs as the error criteria. The proposed ThermSubCP flow is shown in Fig. 4

ALGORITHM: THERMSUBCP
Input: p power map configurations (power inputs and output responses)
Output: thermal model with proper order to meet the error bound

1. Start with order one and use the p training configurations to generate thermal models.
2. Use the verification configurations to generate the output of the subspace model
3. Compute the average error and the standard deviation of the error for each output
4. If the error criteria is not satisfied, increase the model order and goto step 1. Otherwise, return the models obtained so far and stop.

Figure 4: The new ThermSubCP algorithm

5. IMPLEMENTATION AND NUMERICAL RESULTS

The microprocessor chip package used in this study is shown in Fig. 5, where the single silicon die is $10mm \times 10mm \times 0.7mm$. We partition it into 4×4 power grids as shown in Fig. 6. The input power sources are placed in each power grids and we measure the temperature at the adjacent 4 corners of each square power grids. As a result, we end up with 16-input and 25-output thermal system. We used the convection coefficient of 450 $(W/(m^2 \cdot K))$ to model the

$$U_i = \begin{bmatrix} g_1(x_0)f(t_i), ..., g_1(x_0)f(t_{i+m}), g_2(x_0)f(t_{i+m+1}), .., g_2(x_0)f(t_{i+N-1}) \\ g_1(x_1)f(t_i), ..., g_1(x_1)f(t_{i+m}), g_2(x_1)f(t_{i+m+1}), .., g_2(x_1)f(t_{i+N-1}) \end{bmatrix} \quad (10)$$

convective cooling effect from the cooling fan on top of the chip package.

To build a more realistic package with right dimension and materials, we applied COMSOL 4.1 [18] to build the package structures with input from our industry partner. The thermal response was performed in COMSOL by the finite element method under the input power maps we generated. Fig. 7 shows the steady state temperature distribution under a given power input on the constructed package and the chip.

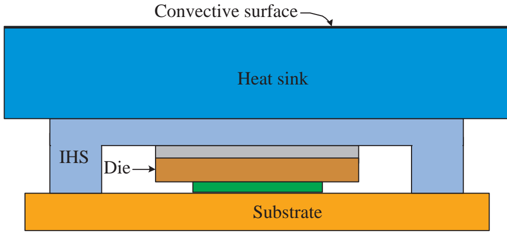

Figure 5: Microprocessor chip package

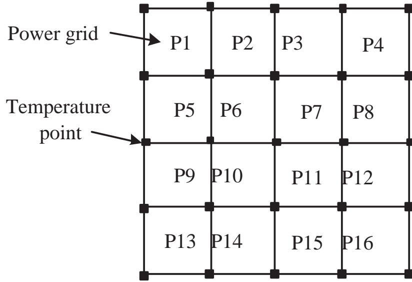

Figure 6: Partitioned die area with power grids and temperature points

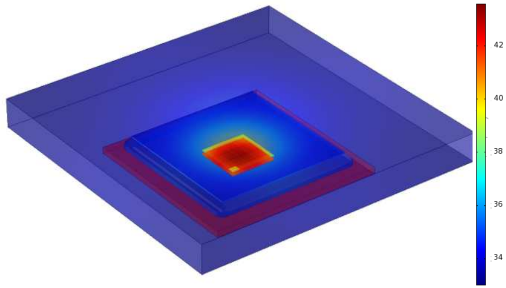

Figure 7: Steady state temperature distribution simulated by COMSOL 4.1

The transient power input for each power grids (its magnitudes will be determined by the specific power map) is shown in Fig. 8, which comes from our industry partner.

5.1 Multi-configuration training and validation

In this case, 16 orthogonal power map configurations are generated by $g_{mn}(x, y) = sin(m\pi x/L_x)sin(n\pi y/L_y)$, in which m and n are the indices starting from 1 up to 4; x and y are the position variables; L_x and L_y are the size of the chip in the x and y direction respectively . Each power input waveform of these independent power map configurations are divided into the two parts for training and validation respectively as mentioned before. The system is trained with the 16 input power map configurations. In the validation phase, in addition to the 16 automatically generated power map configurations, new configurations from #17 to #20 are introduced and their spatial distributions are defined in Table 1, where P_0 is the input power intensity at the origin where (x, y) represents the position on the chip. These new power map configurations(from #17 to #20) are totally different from the configurations used for training the system. The matched response in both time domain and frequency domain demonstrated that the thermal system has been correctly identified by the subspace method which uses multiple independent power map configurations as its training inputs.

Table 1: Additional input power map configurations for validation

$0 < x < 4 \quad 0 < y < 4$

Configuration Num.	Spatial Distribution of the Input
17	$P = P_0(cos(\frac{x+y-2}{4}) + \frac{xy^3}{ln(x+2)} + e^{y+2} + \frac{1}{3}\frac{\sqrt{xy}ln(4y+x-4)}{5x^2\sqrt{y+1}\sqrt{\sqrt{x}y}})$
18	$P = P_0(e^{-2x-y} + \frac{x}{4})$
19	$P = P_0(e^{-xy} + \frac{ln(\sqrt{x}y^2+1)}{x})$
20	$P = P_0\frac{(x+y+e^{-x+2}+xy^3e^{-x}+1)}{5y\sqrt{x}}$

The output error information of the identified system is summarized in Table 2, where we list the maximum of the mean errors ($Max\ Mean\ error$) and the maximum of its standard deviation ($Max\ standard\ deviation$) among all the ports over the entire transient simulation period. $Train(sec)$ is the

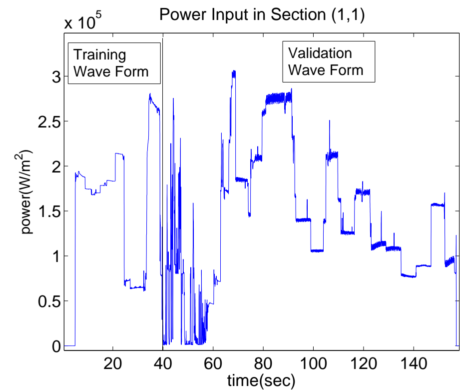

Figure 8: Input power trace for training and validation

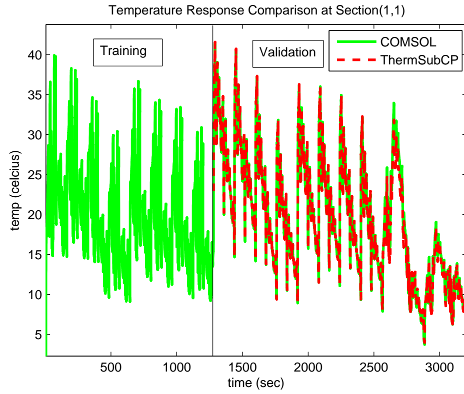

Figure 9: On-chip temperature response in section (1,1)

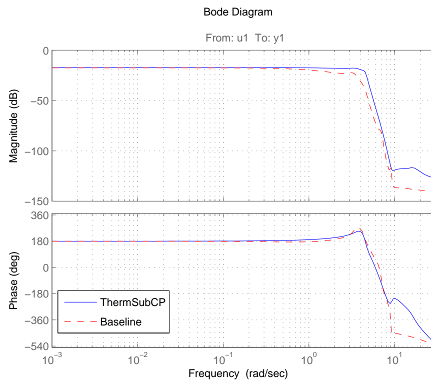

Figure 10: Bode diagram of transfer function from input u_1 to output y_1

simulation time time used for the training process. We can clearly observe that both the error and its deviation are reduced as the model order increases; the cost of using the higher order model is the increased simulation time for system training.

Table 2: Training and error information

ThermSubCP order	30	25	20
Train (min)	19.4	15.5	10.4
Max mean error	1.61%	4.00%	10.1%
Max standard deviation	0.038	0.035	0.075

6. CONCLUSION

In this paper, we have proposed a new thermal modeling technique considering practical power maps with highly correlated input powers. We showed that the power maps should be independents and has sufficient numbers to ensure model predictability. We developed a new modeling method, which generates independent power maps to meet the spatial rank requirement and can also automatically select the order of the thermal models for the give error bounds. Experimental results validates the proposed method on a practical microprocessor package constructed by COMSOL software under practical power signal inputs.

7. REFERENCES

[1] "International technology roadmap for semiconductors(ITRS)," 2009 update, http://public.itrs.net.

[2] A. Augustin, B. Maj, and A. Kostka, "A structure oriented compact thermal model for multiple heat source ASICs," *Mircroelectronics Journal*, vol. 36, no. 8, pp. 700–704, August 2005.

[3] D. Brooks and M. Martonosi, "Dynamic thermal management for high-performance microprocessors," in *Proc. of Intl. Symp. on High-Performance Comp. Architecture*, 2001, pp. 171–182.

[4] F. Christiaens, B. Vandevelde, E. Beyne, R. Mertens, and J. Berghmans, "A generic methodology for deriving compact dynamic thermal models, applied to the PSGA package," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, vol. 21, no. 4, pp. 565–576, December 1998.

[5] T. Eguia, S. X.-D. Tan, R. Shen, E. H. Pacheco, and M. Tirumala, "General behavioral thermal modeling and characterization for multi-core microprocessor design," in *Proc. Design, Automation and Test In Europe. (DATE)*, March 2010, pp. 1136–1141.

[6] Y. C. Gerstenmaier and G. Wachutka, "Rigorous model and network for transient thermal problems," *Mircroelectronics Journal*, vol. 33, pp. 719–725, September 2002.

[7] G. H. Golub and C. V. Loan, *Matrix Computations*, 3rd ed. The Johns Hopkins University Press, 1996.

[8] W. Huang, M. Stan, K. Skadron, K. Sankaranarayanan, S. Ghosh, and S. Velusamy, "Compact thermal modeling for temperature-aware design," in *Proc. Design Automation Conf. (DAC)*, 2004, pp. 878–883.

[9] T. Katayama, *Subspace Methods for System Identification.* Springer, 2005.

[10] C. Lasance, H. Vinke, H. Rosten, and K.-L. Weiner, "A novel approach for the thermal characterization of electronic parts," in *Proceedings of the IEEE 11th Annual Semiconductor Thermal Measurement and Management Symposium*, 1995, pp. 1–9.

[11] D. Li, S. X.-D. Tan, and M. Tirumala, "Architecture-level thermal behavioral characterization for multi-core microprocessors," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)*, 2008, pp. 456–461.

[12] P. V. Overschee and B. D. Moor, "N4SID: Subspace algorithms for the identification of combined deterministic-stochastic systems," *Automatica*, vol. 30, no. 1, pp. 75–93, 1994.

[13] ——, *Subspace Identification for Linear Systems, Theory - Implementation - Applications.* Kluwer Academic Publishers, 2006.

[14] H. Pape, D. Schweitzer, J. H. Janssen, A. Morelli, and C. M. Villa, "Thermal transient modeling and experimental validation in the european project PROFIT," *IEEE Tran. on Components and Pacakaging Technologies*, vol. 27, no. 3, pp. 530–538, September 2004.

[15] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in VLSI circuits: Principles and methods," *Proc. of the IEEE*, vol. 94, no. 8, pp. 1487–1501, Aug. 2006.

[16] M. Rencz, G. Farkas, V. Székely, A. Poppe, and B. Courtois, "Boundary condition independent dynamic compact models of packages and heat sinks from thermal transient measurements," in *Proceedings of the 5th Electronics Packaging Technology Conference*, 2003, pp. 479–484.

[17] K. Skadron, M. R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan, "Temperature-aware microarchitecture," in *Proc. Int. Symp. on Computer Architecture (ISCA)*, 2003, pp. 2–13.

[18] www.comsol.com, "Comsol mutiphysics: User guide," *Version 4.1.*