Compact Thermal Modeling For Microprocessor Design With Spatially Correlated Power Inputs *

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ABSTRACT

This paper proposes a new thermal modeling method for the thermal design of package for high-performance microprocessors. The new approach builds the thermal behavioral models from the given accurate temperature and power information by means of the subspace method. The subspace method, however, may suffer predictability problem when the practical power inputs are spatially correlated (power maps). We try to address this important issue in this paper. We first we show that there exists a theoretical spatial rank (or the ranks of signals among different correlated power inputs) requirement to ensure model predictability. Second, we develop a new algorithm, which generates independent power maps to meet the spatial rank requirement and can also automatically select the order of the resulting thermal models for the given error bounds. Experimental results validate the proposed method on a simplified microprocessor under practical power signal inputs.

1. INTRODUCTION

Recently, temperature has become a major concern for high-performance microprocessor design as more devices are integrated on a chip. Thermal management and related design problems continue to be identified by the Semiconductor Industries Association Roadmap [7] as one of the five key challenges during the next decade for achieving the projected performance goals of the industry. Thus, accurate and efficient thermal modeling and analysis is vital for the thermal-aware chip and package designs to improve performance, reliability, power reduction, and online temperature regulation techniques [14, 2, 16].

The traditional bottom-up approaches including FEM (finite element), FDM (finite difference), and computational flow dynamics (CFD) based methods were widely used for thermal modeling and analysis in the past. Many of these approaches try to use thermal resistors and capacitors with fixed topology networks subject to different thermal boundary conditions [9, 3, 1]. However, the accurate RC values of elements, especially for complex geometries and boundary conditions are difficult to determine, and the optimization against the field numerical or analytic results [5, 13] and measured data are usually required [15].

For thermal modeling at the architecture level, existing work on HotSpot [6, 16] attempts to solve this problem by generating the architectural thermal model in a bottom-up manner based on the internal structure/architecture of the microprocessor. However, bottom-up compact models may suffer from accuracy loss, and have to be calibrated with hardware if more accurate models are required. Recently, top-down behavioral thermal modeling methods have been proposed using the matrix pencil method [10] and the subspace method [4]. The subspace method, though, may suffer from the lack of predictability problems in general [11, 8], especially when the input signal is highly correlated as it is difficult to distinguish the contribution from specific inputs when all the inputs have the same or similar transient waveforms.

In this paper, a new subspace-based thermal modeling techniques is developed for package-level thermal design of high-performance microprocessors. First, we theoretically demonstrated there exists a required rank of the input power signal matrix to avoid the predictability problems in subspace method. Second, we developed a new modeling algorithm to automatically select the order of the thermal models for given error bounds. Experimental results validates the proposed method on a simplified microprocessor under piratical power inputs.

2. THERMAL MODELING PROBLEM UNDER POWER MAP WITH SPATIALLY CORRELATED POWER SIGNALS

A microprocessor chip is meshed into $p = n \times m$ grids as shown in Fig. 1, where each grid has a power source and its measured temperature as output. We can abstract this $p = n \times m$ model into a discrete linear system with p power inputs and p temperature outputs as shown in Fig. 2.

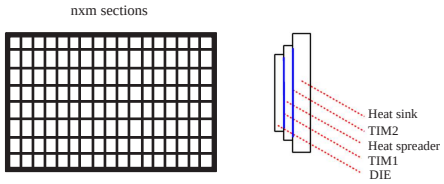

Figure 1: Partitioned chip and package

$$\begin{aligned} x(t+1) &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Du(t), \end{aligned} \quad (1)$$

where $A \in \mathbb{R}^{l \times l}$ is a stable matrix, l is the number of states. $B \in \mathbb{R}^{l \times p}$, $C \in \mathbb{R}^{p \times l}$, and $D \in \mathbb{R}^{p \times p}$. The input vectors $u(t) \in \mathbb{R}^{p \times 1}$ are the measured power input traces and output vectors $y(t) \in \mathbb{R}^{p \times 1}$ are the temperature responses. With s input samples $u(t_i)$ and s output samples $y(t_i)$ where $i = 1, 2, \ldots, s$, the problem at hand is how to generate state matrices A, B, C, and D, where D is typically considered a matrix of zeros.

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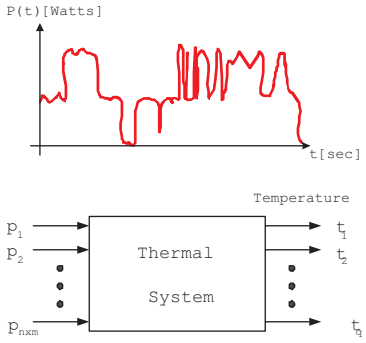

Figure 2: The abstracted model system and correlated power inputs

For all the $n \times m$ power inputs, they may be highly correlated as mentioned before. In an extreme case, all the power input waveforms are the same and they are only different by their magnitudes. Fig. 2 (top) shows a typical power input waveforms. Their spatial difference in magnitudes can be described by the *power map* of the chips, which can be measured in practice. The magnitude (power map) distributions can be even, linear, exponential or any 2-D shapes defined by a function. Such magnitude distribution is called *power map configuration* in this paper.

Such highly correlated power inputs will lead to poor predictability by using the subspace identification method [12, 8]. Fig. 3 show that the waveforms produced by the model trained by highly correlated power inputs (one power map configuration), where the results from model and from original temperature does not match well.

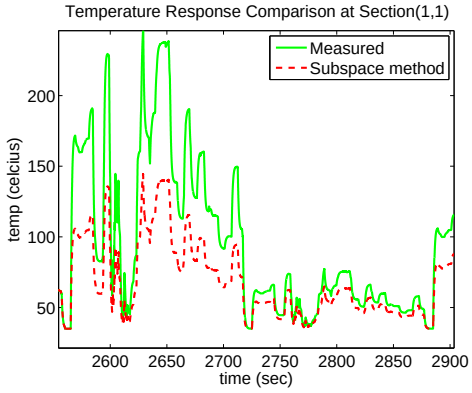

Figure 3: Transient temperature response of the system trained with one highly correlated power inputs

3. NEW THERMAL MODELING METHOD FOR POWER MAP WITH CORRELATED POWER INPUTS

3.1 Spatial rank requirement

Given input $u(t)$ and output $y(t)$, subspace identification method identifies the state matrices A, B, C, and D of (1). The subspace identification basically tries to first identify the system states (Kalman states), then the state matrices will be obtained by the least square based optimization method [8]. In this paper, we apply the widely used N4SID method for this system identification problem.

In general, the *persistently exciting*, or PE condition is required for system identification [12], which can be easily satisfied for a MIMO dynamic system when all the input signals are uncorrelated. However, if those signals are highly correlated, the PE condition may not be easily satisfied, which leads to poor predictability of the resulting models as shown in Fig. 3. Specifically, consider a 2-input system. We assume that all the inputs have exactly the same time domain waveform and denote it as $f(t)$. The difference in magnitudes are represented by another spatial function $g(x)$ in 1-D space (x-axis) for simplicity, which represents the 1-D power map configuration. The i-th input sample for such 2-input system is

$$u(i) = \begin{bmatrix} g(x_0)f(t_i) \\ g(x_1)f(t_i) \end{bmatrix} \tag{2}$$

We further define the i-th block row in the input Hankel matrix as

$$U_i = \begin{bmatrix} g(x_0)f(t_i) & g(x_0)f(t_{i+1}) & \cdots & g(x_0)f(t_{i+N-1}) \\ g(x_1)f(t_i) & g(x_1)f(t_{i+1}) & \cdots & g(x_1)f(t_{i+N-1}) \end{bmatrix} \tag{3}$$

The input Hankel matrix can be expressed as

$$U_{0|2k-1} = [U_0^T, \quad U_1^T, \quad \ldots \quad U_{2k-1}^T]^T \tag{4}$$

The *persistently exciting* condition is satisfied when $U_{0|2k-1}$ has full row rank, that is $\text{rank}(U_{0|2k-1}) = 4k$ for this 2-input case. However, it is clear that the two rows in U_i are linearly dependent, which makes $\text{rank}(U_{0|2k-1}) = 2k$ and fail to satisfy the *persistently exciting* condition.

In order to make the input Hankel matrix $U_{0|2k-1}$ full row rank, we need to make the i-th block row U_i full row rank, assuming $N \gg k$. For this 2-input example case, we can achieve this by simply introducing another power map configuration. Now we have two configurations, g_1 and g_2. The i-th block row U_i is shown in (5) on top of the next page, where $i < m < i + N - 1$. The two dimensional case can be generalized into higher dimensions with g_i as a function of two spatial variables x and y. By calling the row rank of i-th block row U_i the *spatial rank* of input signals, we have the following proposition.

PROPOSITION 1. *For p-input MIMO dynamic systems with correlated input signals, the spatial rank of input signals must be equal to p to satisfy the persistently exciting condition in the subspace method.*

3.2 Orthogonal set of power map configurations

In this section, we show how to automatically generate independent power map configurations to meet the PE requirement as mentioned in previous subsection. It is necessary since the number of inputs can be large.

Take the 1-D example again, if $x \in [0, L]$, a set of orthogonal functions over the interval $[0, L]$ can serve as the systematic solution for the independent and robust configurations. The orthogonal function set $\{g_1, g_2, \ldots, g_N\}$ satisfies

$$\int_0^L g_i(x)g_j(x)\,dx = \begin{cases} 0 & i \neq j \\ \|g_i(x)\|^2 & i = j \end{cases} \tag{6}$$

Note that one is free to choose any set of orthogonal functions. In this paper, $sin(i\pi x/L)$, $i = 1, 2, 3, \ldots$, is used as the arbitrary orthogonal function on $x \in [0, L]$. In our application, we choose i up to p, the number of ports, and L as the maximum of x dimensions.

$$U_i = \begin{bmatrix} g_1(x_0)f(t_i), ..., g_1(x_0)f(t_{i+m}), g_2(x_0)f(t_{i+m+1}), .., g_2(x_0)f(t_{i+N-1}) \\ g_1(x_1)f(t_i), ..., g_1(x_1)f(t_{i+m}), g_2(x_1)f(t_{i+m+1}), .., g_2(x_1)f(t_{i+N-1}) \end{bmatrix} \quad (5)$$

3.3 New thermal modeling algorithm with automatic order selection - ThermSubCP

Now we are ready to introduce our new thermal modeling algorithm considering the highly correlated power inputs – *ThermSubCP*. Once we generate all the independent power map configurations, we need to generate two transient power sequences – one for training and one for validation. For each power map configuration, we basically divide the given transient power input waveform into two parts. The first part will be used for the training and the second part will be used for the validation. To test the predictability of the models, we will also add some additional power maps, which are not used for training. For instance, suppose we have a 4-input MIMO system, then we need 4 independent power maps with transient power inputs denoted as P_1, P_2, P_3, P_4. Then we split $P_1 = [P_{11}, P_{12}]$ into two parts in time scale. We do the same for other 3 power inputs. Then the training sequence will be $[P_{11}, P_{21}, P_{31}, P_{41}]$, while the validation sequence will be $[P_{12}, P_{22}, P_{32}, P_{42}, P_{a1}, P_{a2}]$, where P_{a1}, P_{a2} are the additional power inputs in power maps not used for training.

ThermSubCP also tries to automatically select the proper order of the models to satisfy the given error bounds by gradually increasing the order of the models until the accuracy in the validation phase is met. In our implementation, we use the maximum of the mean errors and their variances (standard deviation) over all the transient responses for all the outputs as the error criteria. The proposed ThermSubCP flow is shown in Fig. 4

ALGORITHM: THERMSUBCP
Input: p power map configurations (power inputs and output responses)
Output: thermal model with proper order to meet the error bound

1. Start with order one and use the p training configurations to generate thermal models.
2. Use the verification configurations to generate the output of the subspace model
3. Compute the average error and the standard deviation of the error for each output
4. If the error criteria is not satisfied, increase the model order and goto step 1. Otherwise, return the models obtained so far and stop.

Figure 4: The new ThermSubCP algorithm

4. IMPLEMENTATION AND NUMERICAL RESULTS

The proposed method has been implemented in Matlab. The simplified model used in this study is shown in Fig. 5, where the single silicon die is $4mm \times 4mm \times 2mm$. We partition it into $8 \times 8 \times 4$ grids (total 256 grids). The 64 grids at the lower level have input power sources and we measure the temperature at the top level grids. As a result, we end up with 64-input and 64-output system. Here the thermal conductivity used is $149W/(m \cdot K)$, density is $2300kg/m^3$, specific heat is $700J/(kg \cdot K)$. To model the convection effect at the top (all the other sides are adiabatic). We partition the top surface into four parts with different heat coefficients, where the unit is $(W/(m^2 \cdot K))$.

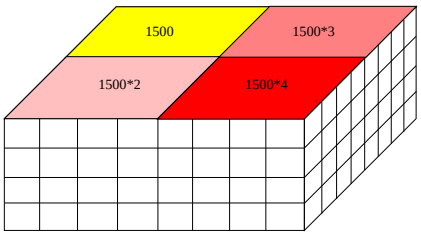

Figure 5: Simplified mesh-structured silicon microprocessor

The transient power input for each grids (its magnitudes will be determined by the specific power map) is shown in Fig. 6, which comes from our industry partner.

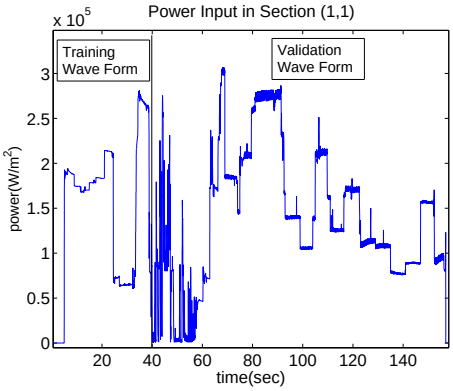

Figure 6: Input power trace for training and validation

4.1 Multi-configuration training and validation

In this case, 64 orthogonal power map configurations are generated by $g_{mn}(x, y) = sin(m\pi x/L_x)sin(n\pi y/L_y)$, in which m and n are the indices starting from 1 up to 8; x and y are the position variables; L_x and L_y are the size of the chip in the x and y direction respectively . Each power input waveform of these independent power map configurations are divided into the two parts for training and validation respectively as mentioned before. The system is trained with the 64 input power map configurations. In the validation phase, in addition to the 64 automatically generated power map configurations, new configurations from #65 to #68 are introduced and their spatial distributions are defined in Table 1, where P_0 is the input power intensity at the origin where (x, y) represents the position on the chip. These new power map configurations(from #65 to #68) are totally different from the configurations used for training the system. The matched response in both time domain and frequency domain demonstrated that the thermal system has been correctly identified by the subspace method which uses multiple independent power map configurations as its training inputs.

The output error information of the identified system is sum-

Table 1: Additional input power map configurations for validation

$0 < x < 4 \quad 0 < y < 4$

Configuration Num.	Spatial Distribution of the Input
65	$P = P_0(cos(\frac{x+y-2}{4}) + \frac{xy^3}{ln(x+2)} + e^{y+2} + \frac{1}{3}\frac{\sqrt{xy}ln(4y+x-4)}{5x^2\sqrt{y+1}\sqrt{\sqrt{xy}}})$
67	$P = P_0(e^{-2x-y} + \frac{x}{4})$
68	$P = P_0(e^{-xy} + \frac{ln(\sqrt{x}y^2+1)}{x})$
69	$P = P_0\frac{(x+y+e^{-x+2}+xy^3e^{-x}+1)}{5y\sqrt{x}}$

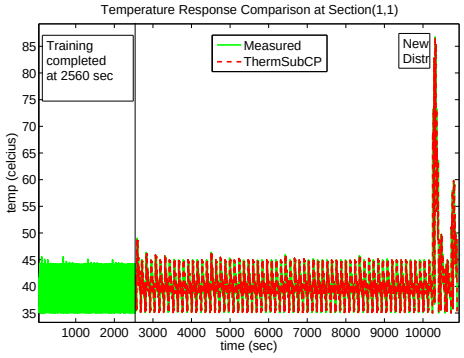

Figure 7: On-chip temperature response in section (1,1)

marized in Table 2, where we list the maximum of the mean errors (*Max Mean error*) and the maximum of its standard deviation (*Max standard deviation*) among all the ports over the entire transient simulation period. $Train(sec)$ is the simulation time time used for the training process. We can clearly observe that both the error and its deviation are reduced as the model order increases; the cost of using the higher order model is the increased simulation time for system training.

5. CONCLUSION

In this paper, we have proposed a new thermal modeling technique considering practical power maps with highly correlated input power signals. We showed that sufficient number of independent power maps are required to ensure model predictability. we developed a new modeling algorithm,

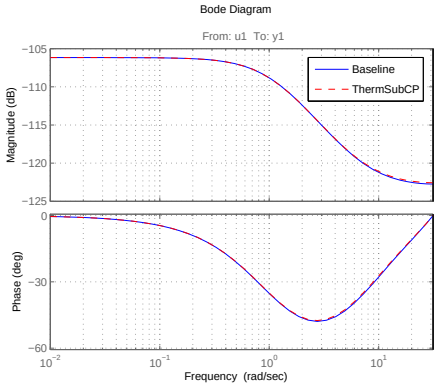

Figure 8: Bode diagram of transfer function from input u_1 to output y_1

Table 2: Training and error information

ThermSubCP order	5	3	1
Train (sec)	48.06	30.39	13.9
Max mean error	0.0061%	0.011%	0.072%
Max standard deviation	0.038	0.0494	0.327

which generates independent power maps to meet the spatial rank requirement and can also automatically select the order of the thermal models for the given error bounds. Experimental results validates the proposed method on a simplified microprocessor under practical power signal inputs.

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