Random Walk Guided Decap Embedding for Power/Ground Network Optimization

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***Abstract*—The reliability of Power/Ground networks is becoming significantly important in modern integrated circuits, while decap insertion is a main approach to enhance the power grid safety. In this brief, we propose a fast and efficient decap allocation algorithm, and adequately consider the leakage effect of decap. This approach borrows the idea of random walks to perform circuit partitioning and does subsequent decap insertion based on locality property of partitioned area, which avoids solving a large nonlinear programming problem in traditional decap optimization process. The optimization flow also integrates a refined leakage current model for decaps which makes it more practical. Experimental results show that our proposed method can achieve approximate 15X speed up over the optimal budget method within the acceptable error tolerance. Also this algorithm only causes a few penalty area to compensate the leakage effect.**

***Index Terms*—Leakage, optimization, power/ground (P/G) network, random walks.**

I. Introduction

As TECHNOLOGY scales down to 90 nm and below, robust power/ground (P/G) delivery network is considered as one of the grand design challenges. Power problems are caused by the rising frequency and continuously squeezing for more device integrations. The improper design of power distribution system can degrade the circuit reliability and cause functional failures due to excessive IR drops, Ldi/dt noise as well as leakage current.

Driven by the importance of the robust design of P/G delivery network, many novel circuit simulation methods [1]–[4] have been proposed to capture the excessive IR drops and the increasing dynamic voltage fluctuations of the power grid. In general, due to the trend of higher current consumption of the power grid, wire sizing technique [5], [6] is typically used to reduce the static IR drop, which enlarges the trunk widths in power ground networks and consumes more routing resource. However dynamic voltage fluctuations may still exceed the limitation even if the wire sizing strategy is performed. In this case, adding decoupling capacitors [7]–[10] on the spare die area is a suitable way to reduce dynamic noise. According to the modeling of P/G network shown in Fig. 1, decap provides reservoir capacitor between power net and ground net, which can form fast current return paths to reduce the dynamic noise. For Ldi/dt noise, some research results, i.e., [14], show that the on die wire inductance effect is not so significant compared with that in the package, thus in this work, we mainly concentrate on fast decap insertion, also, because a inductance can be treated as parallel connected conductance and current source after discretization [17], the algorithm described in this brief can also be extended to handle inductance dominant cases.

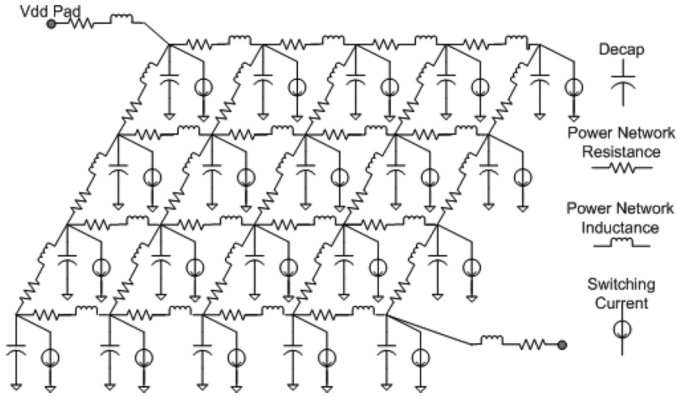

Fig. 1. Model of P/G network.

In order to acquire the optimal decap area, the authors in [7], [8] use nonlinear optimization to get the optimal results under given constraints. But the optimization process is very time-consuming due to the sensitivity computation and line search for new descent direction. Also, partitioning-based conjugate gradient method [9] uses the divide-and-conquer strategy to deal with decap budgeting problem, but it still has to carry out nonlinear programming to optimize the subcircuits.

In this work, we adopt an efficient and practical algorithm to optimize the dynamic performance of power network without solving any linear/nonlinear programming problem. We use preconditioned conjugate gradient (PCG) method to get the transient response of power grid, and then perform the random walks starting from the violation nodes to get a local area around the violation nodes and finally get a partitioning of the network. Because global dynamic performance highly relies on the performance of each individual subarea due to the locality of power grid [16], and the random walk method shall intuitively generate the circuit partition whose boundaries might have low IR drop, thus the accuracy loss due to partitioning can be reduced. Still, our experiment results demonstrate that trying to improve the local solution quality while get the requirement at the boundary node to be relaxed will improve overall design quality and computation efficiency than just trying to improve

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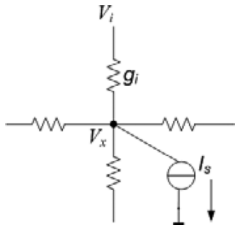

Fig. 2. Representative part of P/G networks.

the global solution quality. Besides, because the additional leakage current caused by decaps will cause extra voltage drop, we integrate a more accurate decap leakage model which can improve the practical design quality.

II. Using Random Walk for Network Partition

A. Traditional Random Walks for Circuit Simulation

Random walk [3], a classical stochastic simulation technique, is also widely used to solve many engineering problems. For example, random walk is adopted for circuit simulation such as the power grid verification [4], the analysis of the circuit with the resistor and power supply can be transformed into a random walk on the circuit graph via using walking probability determined by the electrical parameters on one path. No matrix solving technique is needed in the random walk algorithm.

For the circuit illustrated in Fig. 2, (1) in nodal equation form can be got according to Kirchoff 's current law

$$V_x \sum g_i - \sum g_i V_i = -I_s. \tag{1}$$

Equation (1) can be reformulated as follows:

$$V_x = \sum \frac{g_i}{\sum g_i V_i} - \frac{I_s}{\sum g_i}. \tag{2}$$

If we define the coefficient $g_i / \sum g_i$ to be $p_{x,i}$, then we can get $\sum p_{x,i} = 1$. Thus, $p_{x,i}$ can be treated as the walking probability from node x to node i. This means that the constant $-I_s / \sum g_i$ can be treated as the cost we should pay at node x [4]. When achieving the home nodes (pad nodes), the walker stops the walking process and get a certain award. Through the whole walking process, we can calculate the total cost by accumulating that at each step. It has been proved that the average cost from one node to the home node in random walk process is equal to the node voltage calculated by traditional P/G network analysis process [3]. Thus, we can play the walks for a certain number of rounds, and calculate the expected cost as the voltage of the starting node in a statistical way.

It has been demonstrated that the complexity of random walks for dc analysis is linear in circuit size, and it is really an accuracy-runtime tradeoff [4]. Compared with other methods, the performance of the random walks is very excellent when solving a specific node or a portion of the large power grid. But there are still some problems existing as follows.

- First, if the grid has few vdd pads or the grid is too large, the algorithm has large runtime overhead, because in such circuits, the chance of hitting the home nodes is too small.
- Second, the speedup over other methods only suits for a single node or a small number of nodes. It is difficult to use random walk method to calculate a complete large circuit.

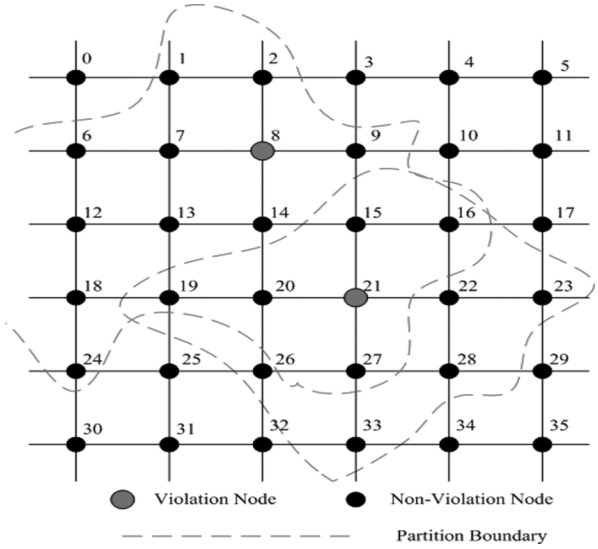

Fig. 3. Boundary gained by the modified random walk process.

- Third, it is also difficult to use the approach to solve the transient analysis problem, because the linear model of dynamic elements deduced by Norton Equivalent model should be updated in each simulation step. In other words, if we use random walk approach to solve all the nodes in transient analysis, it may not be very effective on analyzing the voltage variation for decoupling capacitor budgeting.

In the next part, we will introduce the partition approach using the random walk process, which utilizes the advantage of the random walks.

B. Partition Based on Random Walks

Our main idea is to use the random walk process to partition the power grid.

Firstly, we adopt the conjugate gradient solver with incomplete Cholesky decomposition preconditioner (ICCG) as the transient analysis simulation tool. After the simulation process is finished, the violation nodes, whose voltage is below the threshold, are gained.

Then, we treat these violation nodes as the starting nodes in the random walk process so that the violation node is included in the partition. In our new method, the process still walks according to the probability mentioned in Section II which mainly decided by the resistors in power grid. But differently, in the power grids of the standard-cell layout, only a few pads locate at the boundary of chip, thus we do not force the walk terminates at pad nodes, instead, the termination condition in our method is controlled by a parameter which affects the size of the subarea getting from the modified walking process. After the walking process is finished, we can get an area around the violation nodes. As we do not need to reach the pad nodes, the costs in random walk for each violation node mentioned is quite small. By performing the walk process several times, all the nodes, accessed from the starting node, have been recorded thus the boundary for each violation node can be gained.

Fig. 3 gives out an example of the boundary generated by our proposed method. In this figure, node 8 and 21 are violation nodes and the boundaries are shown in dashed lines.

Compared with the method adopting a fixed boundary near violation node, the area generated by walking process is more isolated because the walking process tends to stop at nodes

which have less conductance connection with other nodes. Also, the shape of most isolated areas is always irregular, thus to fix the area size will not approach the isolated area exactly. So, by walking method we can get good isolation area to embed decaps.

III. Optimization Technique

A. Isolation Decap Planting

Our decap embeding technique is based on the following observation: due to high via density in M1, the noise current inside local area usually not propagates along with the rail but trends to go up to M2 first from the vias. Thus, if no decaps are planted to provide fast current return path, it will go to up layers until the pad is reached. This usually causes long current paths and makes significant dynamic voltage drop. On the other hand, the higher metal layer the noise current goes, the smaller voltage drop it can causes due to small metal resistance. So, if we can reduce the path length in M1 and M2, it is enough to reduce the noise level obviously.

After the isolation area is given using walking method introduced in the last section, we can embed decaps at the subarea first to enhance the isolation property for dynamic noise reduction. Because decaps cannot reduce the static voltage drop efficently, how many decaps should be embeded depends on the dynamic wavefrom analysis for switching current. When the first time simulation is finished, we can get all the waveform of violation nodes. Then we can perform fast Fourier transform (FFT) analysis on these waveforms to eliminate low frequency noise and using the amplitude of high frequency harmonics to caculate the quantity of decaps.

For any continues waveform of switching current in time domain, named $I(t)$: the Fourier transformation can represent the time-domain waveform using different frequency harmonics ω_i as shown in

$$I(t) = a_0 + \sum_{i=1}^{N-1} (a_i \cos \omega_i t + b_i \sin \omega_i t). \tag{3}$$

Usually, the time-domain analysis will describe the current waveform in discrete way, which means we only know the current value at discrete time point. Given a current waveform series $x(i)$, which represents the current at time point i, ranging from time point zero to time point $N-1$ with total time period equal to T, different harmonic amplitude can be calculated using FFT transformation described in (4)

$$X(\omega_k) = \sum_{n=0}^{N-1} x(n) e^{-j\left(\frac{2\pi}{N}\right)nk} \tag{4}$$

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(\omega_k) e^{j\left(\frac{2\pi}{N}\right)nk}. \tag{5}$$

After the FFT process, we can divide original current into the dc part I_{dc} and the ac part I_{ac} according to the harmonic frequency (dc part has harmonic frequency trend to zero)

$$I(t) = I_{\mathrm{dc}}(t) + I_{\mathrm{ac}}(t). \tag{6}$$

Then, we can remove the dc part from the original current and use the inversing FFT process to recover the $I_{\mathrm{ac}}(t)$ in time domain. Finally, we can use (7) to get the charge needed by internal violation nodes. Because the supply voltage U is already known, thus dividing the needed charge by U, we can get the estimation for the boundary capacitance as shown

$$Q = \sum_i \int_0^T I_{\mathrm{ac}}^{(i)}(t) dt \tag{7}$$

$$C = Q/U. \tag{8}$$

TABLE I
Voltage Drop Comparison Before/After Using the Isolation Decap Planting

Sub area	Node Number	Total Node Number	Improved Node Num	Max Voltage Drop (mv)	
				Former	Improved
1	11	806	11	202.92	188.34
2	36	4032	35	385.17	263.86

Here, we choose a subarea from each power grid, and use the transient simulation tool to compare the IR drops of each node inside the subarea before and after planting process. Table I gives out the isolation planting experiments on test cases. In Table I, columns 1, 2, 3, 4 represent the subarea ID, the internal node number of each subarea, the node number of the whole circuit, and the number of nodes in the subcircuit whose IR drops have been improved, respectively. The last two columns represent the maximum voltage drop of the former subarea and that after planting decaps. From these results, we can observe that, after planting decaps, the dynamic IR drop in the subcircuit has been reduced obviously and nearly all the nodes' voltage drops have been improved. In other words, if the boundary condition is good enough, the planted decaps will isolate every subarea perfectly and each of them can be taken into consideration independently.

B. Boundary Improvement

As shown in Fig. 3, the partitions, acquired by node 8 and 21, are not separated due to the violation nodes lay closely to each other. Especially, the violation node may locate on other node's boundary, so that the boundary node will consume large dynamic current and the isolation decap planting may not be very effective in reducing the voltage drops at the internal nodes of the partition. So it is essential to merge the partitions that intersect each other.

The combination of the intersection partitions can be carried out during the partitioning process based on random walks in Section II. For a certain violation node, we also adopt the modified random walks process to record the accessed nodes. Meanwhile if the accessed node also belongs to another partition, then we can set the intersection mark for the two partitions. So the combination is not very time-consuming due to the complexity of combination is linear with the violation nodes and it can be implemented during the walking process.

As we mentioned above, the improvement of random walk based partition approach ensures that the violation nodes would not appear at the boundary of the subcircuits. In this case, embedding decaps at the boundary node can improve the dynamic performance of internal nodes. In the improved algorithm, the partition results (the number and size of the partitions) are decided by the walking step which is the terminal parameter of

TABLE II
PARTITION RESULTS IN DIFFERENT WAKING STEPS

Walking Step	2	3	4	6	8	10
#Partitions	196	116	78	39	24	7

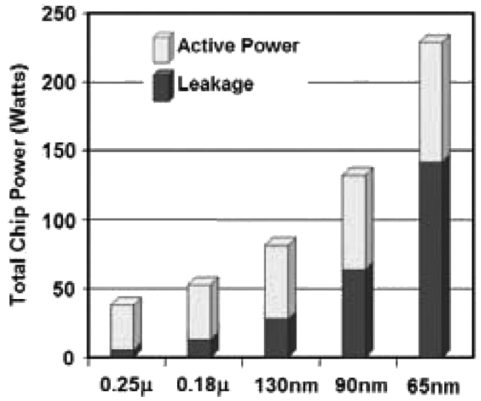

Fig. 4. Trend of power in chips.

the partition process. We partition the same power grid in different walk step, and the results in Table II show that the larger the parameter is, the smaller the partition number is, while the partition size becomes larger. So if the walking step becomes too large, the partition process will generate very large area which almost equal to the original area. Also, the results in Table II demonstrate that in order to get optimal partition size, the walking step will be about 3–6. We also apply this walking step to do the decap embedding process for other industrial circuits, and the result proves that this walking step is approaching the optimal one.

C. Refined Leakage Current Model for Decaps

As Fig. 4 shows, when the technology advances into nano-era, the leakage current will dominant the total current, even larger than the active dynamic current. In [11], the authors first point the necessity of considering leakage current for P/G optimization, but the leakage model is a little simplified. On-chip decaps are usually made of MOS transistors to reduce dynamic voltage noise of different frequencies [12]. The gate leakage of MOS-based decaps may hurt power consumption significantly, and it can be formulated as (9) [11], [13]

$$I_{\text{gate}} = \alpha \times e^{-\beta T_{\text{ox}}} \times w_n \tag{9}$$

where α and β are parameters related to specific technology, w_n is the gate width of nMOS (or pMOS) while T_{ox} is oxide thickness and V is the supply voltage.

The leakage effect in turn will make the added decaps less effective to reduce the voltage drops. But we can further compensate the leakage current through wire sizing strategy. First, it optimizes the dynamic noise assuming all decaps are leakage free, and then, to compensate the IR drops caused by leakage currents, it performs a wire sizing strategy using a branch and bound method to minimize the compensated wire area.

As the isolation decap planting technique, decaps may be planted over ahead. So it is necessary to compensate the leakage current of decaps to make the optimization more practical. The model in [11] as shown in Fig. 5(a), is a little bit oversimplified

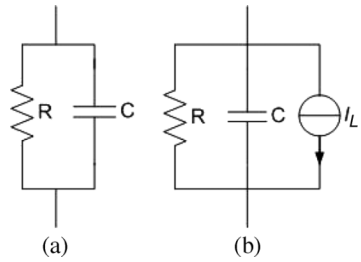

Fig. 5. Two equivalent models for decaps leakage.

TABLE III
VIOLATION NODE STATISTICS COMPARISON TO THE SIMPLIFIED MODEL WHEN OUR NEW MODEL IS CONSIDERED

Circuit Name	Node Number	Dynamic VN Number	Eliminated Leakage VN Number	Newly VN Number using Our Model
1	806	91	6	1
2	4032	665	26	7
3	32952	4750	132	9

VN = Violation Node

```
1. Simulate the circuit, and identify the violation nodes;
2. While (violations) {
3.  For each violation node {
4.    Apply modified random walk process;
5.    Form the partition in the walking process}
6.  Merge the partitions if necessary;
7.  Use boundary allocation strategy for each partition;
8.  Update all decaps and simulate the new circuits}
9. Use wire sizing to compensate the leakage current;
10. Optimization Successful.
```

Fig. 6. Optimization flow guided by random walks.

which only contains a constant resistor besides decap, but the exponential effect is not considered. Here we use an approximate leakage decap model to analyze gate leakage current for MOS-based decaps. As shown in Fig. 5(b), we propose a more accurate leakage decap model containing a resistor, a capacitor and a time-variant current source, which mainly captures exponential changes of the leakage current. We have made a comparison between the two models.

After the circuits are optimized with the simplified leakage model, we introduce our leakage model to P/G grid and apply transient simulation to verify whether the violation nodes still exist. According to Table III, although the optimization process with the simplified leakage model has finished, new violation nodes still appear when the exponential relation between the leakage current and the supply voltage is considered. In order to maintain a robust optimization for P/G network, the decap leakage current model must be sufficiently accurate.

IV. OPTIMIZATION FLOW

The whole optimization flow based on modified random walks is shown in Fig. 6.

Firstly, we read the circuit of power gird, and apply ICCG based circuit simulation tool to get the transient response. Step 2–8 is the iterative optimization flow based on the random walks. Finally, wire sizing strategy is performed to compensate the leakage current of decaps.

In the decap budgeting flow, we only apply transient simulation at two places. One is at the very beginning to solve the circuit, and get all the violation nodes. The other is at the end

TABLE IV
EXPERIMENTAL RESULTS COMPARED TO EXISTING OPTIMAL BUDGET METHOD

Circuit	#Cell	#Leaf Node	Net Area (um^2)	Optimal Budget		Our Proposed Budget			Speed up On Optimal	Deviation from Optimal	Increasing of Net Area
				Decap Area (um^2)	Time (s)	Decap Area (um^2)	Net Area (um^2)	Time (s)			
1	744	806	4804.80	5677.96	109.62	5850.70	4871.65	6.98	15.70	3.04%	1.39%
2	3741	4032	13642.80	35007.88	339.41	37284.03	13917.03	32.37	10.49	6.50%	2.01%
3	32112	32952	52505.60	174591.12	1285.15	183642.33	53140.12	89.74	14.32	5.18%	1.21%
4	112392	108392	44202.24	653771.75	12184.86	683996.98	45842.56	410.89	29.65	4.62%	3.71%
5	1618026	1233432	194976.00	NA	NA	2981355.54	211224.00	1235.42	NA	NA	8.33%

TABLE V
NET AREA INCREASE COMPARISON OF TWO LEAKAGE MODELS

Circuit	#Node	Added Decap without Leakage (um^2)	Ratio of Net Area Increases	
			Simplified Model	Our Accurate Model
1	806	5850.70	1.35%	1.39%
2	4032	37284.03	1.97%	2.01%
3	32952	183642.33	1.19%	1.21%

of every iteration step to check the updated circuits and verify the decap budgeting result. Comparing to the nonlinear methods which need to cost long time to construct the adjoint network, to compute the sensitivity of object function, and to determine the new descent direction, the method proposed in this brief make good use of random walks to avoid complex computation for adjoint network and etc. Also the iterative times is very small demonstrated by experimental results.

By using the optimization, we did experiment on the industry test cases, and compare our proposed method with the optimal decap areas acquired by using the nonlinear programming [8], where the constraints is incorporated into decap area, and the objective functionis solved by traditional conjugate gradient (CG) method based on sensitivity computing using the adjoint network. The comparison result is given in Session V.

V. EXPERIMENT

We implement our presented algorithm in C++. All the experimental results are obtained on a SUN UltraSparc workstation V880 with 1-GHz CPU and 4-GB memory. All test cases are generated as the real industry standard-cell circuits with preplacement information in LEF/DEF format, which have complexities ranging from 806 nodes to 1.2 million nodes.

To demonstrate the efficiency of our proposed optimization algorithm, we compare it with the existing optimal decap budget method using nonlinear programming [7], [8]. To make the comparison possible, we test on the same circuits with the same constraints. Table IV summarizes the comparison, where columns 1–4 represent circuit name, total cell number, total node number, and original power net area, respectively. And the last three columns, we compare the CPU times, decap area deviation and the increase of net area. It shows the following.

1) The random walk based optimization approach is especially fast, and in particular, it almost has a 30× speedup on the optimal method for large circuits.
2) The proposed method only has approximate 5% decap area overhead compared with the optimal budget.
3) The increasing of power nets, used to compensate leakage effect of decaps, just occupies a little more resource.

Specially, at the last step of the optimization flow, we compare our proposed model with the simplified model [11] in net area resource. The comparisonshown in Table V demonstrates that our proposed leakage model, which considers the exponential effect, almost occupies the same net area as the simplified leakage model while it makes the optimization process more practical for use.

VI. CONCLUSION

In this brief, we have proposed a fast and efficient decap allocation algorithm to optimize the P/G networks We use random walk process to find out the best partitioning which shall have good locality, the decap planting on the boundary compensate the dynamic noise inside. A refined leakage current model for decap is also introduced to the proposed optimization flow which only takes a little more resource. The experimental results on the industry test cases show that the proposed method based on random walks achieves approximate a 15× speed up over the optimal method with the acceptable error tolerance.

REFERENCES

[1] M. Zhao, R. V. Panda, S. S. Sapatnekar, and D. Blaauw, "Hierarchical analysis of power distribution networks," *IEEE Trans. Comput.-Aided Design*, vol. 21, no. 2, pp. 159–168, Feb. 2002.
[2] Y. Cao, Y. Lee, T. Chen, and C. Chen, "HiPRIME: Hierarchical and passivity reserved interconnect macro-modeling engine for RLKC power delivery," in *Proc.39th DAC*, Jun. 2002, pp. 379–384.
[3] P. G. Doyle and J. L. Snell, Random Walks and Electric Networks arXiv: math.PR/0001057.
[4] H. F. Qian, S. R. Nassif, and S. S. Sapatnekar, "Random walks in a supply network," in *Proc.40th DAC*, 2003, pp. 93–98.
[5] T. Mitsuhashi and E. S. Kuh, "Power and ground network topology optimization for cell based VLSIs," in *Proc.29th DAC*, 1992, pp. 524–529.
[6] X. Wu, X. Hong, and Y. Cai *et al.*, "Area minimization of power distribution network using efficient nonlinear programming techniques," in *Proc. ICCAD*, 2001, pp. 153–157.
[7] H. Su, S. S. Sapatnekar, and S. R. Nassif, "An algorithm for optimal decoupling capacitor sizing and placement for standard cell layouts," in *International Symposium on Physical Design*, 2002, pp. 68–73.
[8] J. Fu, Z. Luo, X. Hong, Y. Cai, S. X.-D. Tan, and Z. Pan, "A fast decoupling capacitor budgeting algorithm for robust on-chip power delivery," in *Proc. ASPDAC*, Jan. 2004, pp. 505–510.
[9] H. Li, Z. Qi, S. X.-D. Tan, and L. Wu, "Partitioning-based approach to fast on-chip decap budgeting and minimization," in *Proc.42nd DAC*, 2005, pp. 170–175.
[10] L. Kang, Y. Cai, X. Hong, and S. X.-D. Tan, "Fast decoupling capacitor budgeting for power/ground networks using random walk approach," in *Proc. ASPDAC 2007*, pp. 751–756.
[11] Y. Cai, J. Fu, X. Hong, S. X.-D. Tan, and Y. Luo, "Power/ground network optimization considering decap leakage currents," *IEEE Trans. Circuit and System II*, vol. 53, no. 10, pp. 1012–1016, Oct. 2006.
[12] D. J. Herrell and B. Beker, "Modeling of power distribution systems for high-performance microprocessors," *IEEE Trans. Advanced Packaging*, vol. 22, no. 3, pp. 240–248, Aug. 1999.
[13] N. S. Kim, T. Austin, and D. Blaauw *et al.*, "Leakage current: Moore's aw meets static power," *IEEE Trans. Computer*, vol. 36, no. 12, pp. 68–75, 2003.
[14] S. Pant and E. Chiprout, "Power grid physics and implications for CAD," in *Proc.43rd DAC*, 2006, pp. 199–204.
[15] H. F. Qian and S. S. Sapatnekar, "Hierarchical random-walk algorithms for power grid analysis," in *Proc. ASPDAC*, 2004, pp. 499–504.
[16] E. Chiprout, "Fast flip-chip power grid analysis via locality and grid shells," in *Proc. ICCAD*, 2004, pp. 485–488.
[17] W. Guo, S. Tan, Z. Luo, and X. Hong, "Partial random walk for large linear network analysis," in *Proc. ISCAS 2004*, pp. 173–176.