# Physics-Based Electromigration Models and Full-Chip Assessment for Power Grid Networks

Xin Huang, Armen Kteyan, Sheldon X.-D. Tan, *Senior Member, IEEE*, and Valeriy Sukharev

***Abstract*—This paper presents a novel approach and techniques for physics-based electromigration (EM) assessment in power delivery networks of very large scale integration systems. An increase in the voltage drop above the threshold level, caused by EM-induced increase in resistances of the individual interconnect branches, is considered as a failure criterion. It replaces a currently employed conservative weakest branch criterion, which does not account an essential redundancy for current propagation existing in the power-ground (P/G) networks. EM-induced increase in the resistance of the individual grid branches is described in the approximation of the recently developed physics-based formalism for void nucleation and growth. An approach to calculation of the void nucleation times in the group of branches comprising the interconnect tree is implemented. As a result, P/G networks become time-varying linear networks. A developed technique for calculating the hydrostatic stress evolution inside a multibranch interconnect tree allows to avoid over optimistic prediction of the time-to-failure made with the Blech–Black analysis of individual branches of interconnect tree. Experimental results obtained on a number of International Business Machines Corporation benchmark circuits show that the proposed method will lead to less conservative estimation of the lifetime than the existing Black–Blech-based methods. It also reveals that the EM-induced failure is more likely to happen at the place where the hydrostatic stress predicted by the initial current density is large and is more likely to happen at longer times when the saturated void volume effect is taken into account.**

***Index Terms*—Electromigration (EM), hydrostatic stress, interconnect tree, power grid, void, voltage drop.**

## I. Introduction

With the complexity of modern very large scale integration (VLSI) designs, reliability is becoming a more serious concern. Electromigration (EM)-induced reliability threats become more significant with technology scaling and this problem is more severe for power delivery networks as they experience large unidirectional currents and thus are more susceptible to EM effects than signal circuits characterized by bidirectional currents. A physical meaning of the void-induced failure is an increase of the resistance of an individual line. Increase in the resistance above some critical value, say 10% of the initial line resistance, is considered as an EM-induced failure. Continuous increase in the die size accompanied by reduction of the metal line cross sections and, hence, by increase of the current densities, which is governed by a technology scaling, results in an increasingly difficult EM signoff when the traditional EM checking approaches are employed. In these approaches the EM-induced failure rates of the individual branch are considered as a measure of EM-induced reliability and, in the extreme end, a mean time-to-failure (MTTF) of the weakest branch is accepted as a measure for the chip lifetime. It results in a very conservative design rule for the current densities that can be used in the chip design for a particular technology node in order to avoid EM failure. A very different way to EM assessment can be proposed from the positions of interconnect functionality, when the failure means its inability to function properly. There are two most important functions of the chip interconnect, which are: 1) providing a connectivity between different parts of design for a proper signal propagating and 2) delivering a needed amount of voltage where it is required. While cutting-off the individual branches of the interconnect circuits can degrade both functions, the role of EM is quite different in these two cases of degrading the power supply chain and the signal circuits. The difference is in the types of electric currents employed in these two cases. Indeed, the signal lines carrying bidirectional pulse currents are characterized by very long times to the EM-induced failure. It is caused by a repetitive increase and decrease of the mechanical stress at the branch ends, caused by the excessive atom accumulation and depletion due to interaction with the electron flow. In contrast, power lines carrying unidirectional currents can fail in much shorter time due to continuous stress buildup under the EM action. Thus, we can conclude that EM-induced chip failure is happening mostly when interconnect cannot deliver needed voltage to any gate of the circuitry. It means that loss of performance, which is a parametric failure, should be considered as the practical criterion of EM-induced failure. It is clear that a structure of the power grid, which is characterized by high level of redundancy, can affect the kinetics of failure development. Indeed, due to redundancy the failure of some of interconnect branches does not necessary result in a critical voltage drop on the grid causing an electrical malfunction [1], [2]. Thus,

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X. Huang and S. X.-D. Tan are with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA 92521 USA (e-mail: stan@ece.ucr.edu).

A. Kteyan is with Mentor Graphics Corporation, Yerevan 0036, Armenia.

V. Sukharev is with Mentor Graphics Corporation, Fremont, CA 94528 USA.

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more accurate and less pessimistic full-chip EM assessment and MTTF prediction will require development of new methods that deal with the grid structure and take redundancy into account.

An ideal EM assessment assumes a calculability of transient current densities and temperatures in each tree across interconnect. A complexity of extraction of these distributions is acerbated by an uncertainty in workload taking place in modern chips. Its complex multimodal behavior results in different modes of operation. It means that current densities and temperatures in different interconnect trees should be estimated for different workloads and should be used for prediction of MTTF happening in different scenarios including worst-case conditions for voltage drop [1].

Additional problem that should be addressed in order to develop a robust methodology for the full-chip EM assessment is an employment of accurate physics-based models for void/hillock initiation and evolution responsible for a time-dependent degradation of the branch resistance. Currently, employed method of predicting the time to failure based on the approximate statistical Black's equation [3]

$$\mathrm{MTTF} = Aj^{-n}\exp\{E_a/k_BT\} \tag{1}$$

calculating the MTTF of individual branches characterized by known current densities and temperatures, is the subject of growing criticism. Here, $j$ is the current density, $k_B$ is the Boltzmann's constant; $T$ is the absolute temperature; $E_a$ is the EM activation energy. The symbol $A$ is a constant, which depends on a number of factors, including grain size, line structure and geometry, test conditions, current density, thermal history, etc. Black has determined the value of $n$ as equals to 2. However, it is a today's common understanding that $n$ depends on residual stress and temperature [4], [5], and its value is highly controversial. In addition, as it was shown in a number of experiments (see [6]) $E_a$ is a function of the current density. All these observations make rather controversial the widely accepted methodology of calculating the MTTF at use condition, represented by chip operation current density and temperature, while using $n$ and $E_a$ determined at the stressed (accelerated) condition, characterized by high current densities and elevated temperatures as

$$\mathrm{MTTF}_{\mathrm{use}} = \mathrm{MTTF}_{\mathrm{stress}}\left(\frac{j_{\mathrm{stress}}}{j_{\mathrm{use}}}\right)^n exp\left\{\frac{E_a}{k_B}\left(\frac{1}{T_{\mathrm{use}}} - \frac{1}{T_{\mathrm{stress}}}\right)\right\}. \tag{2}$$

Employments of the Blech limit [7]

$$(j \times L) \le (j \times L)_{\mathrm{crit}} = \frac{\Omega\sigma_{\mathrm{crit}}}{eZ\rho} \tag{3}$$

for the out-filtration of immortal branches, is also required a serious justification. Here, $L$ is the branch length, $\Omega$ is the atomic volume, $e$ is the electron charge, $eZ$ is the effective charge of the migrating atoms, $\rho$ is the wire electrical resistivity, $\sigma_{\mathrm{crit}}$ is the critical stress needed for the failure precursor nucleation for void or hillock. Condition of immortality (3) means that the atomic flux, generated by stress gradient in the metal lines characterized by $(j \times L) \le (j \times L)_{\mathrm{crit}}$, compensates the atomic flux caused by electrical current density. It should be mentioned that the Blech limit is valid only for branches with the diffusion blocking boundaries. Accumulation of the hydrostatic stress, caused by redistribution of the metal atoms under the current density action, exceeding the critical stress responsible for void nucleation or the liner rupture, followed by metal extrusion into intra metal dielectric (hillock formation), takes place in branches with the confined metal atoms only. Modern power-ground (P/G) networks consist of interconnect trees representing continuously connected, highly conductive metal lines within one layer of metallization, terminated by diffusion barriers (Fig. 1).

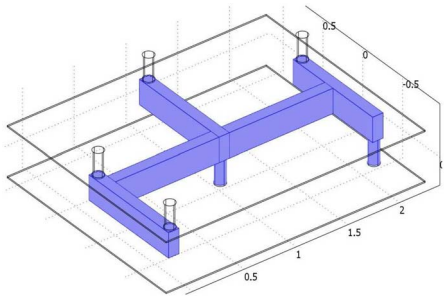



Fig. 1. Interconnect tree confined by diffusion barriers/liners.

Absence of blocking boundaries at one or both ends of the individual branches of interconnect trees prevents atoms from accumulation/depletion at the branch ends, and, hence, makes the traditional immortality assessment and MTTF calculation as groundless [8]. A widely practiced decomposing the multibranch interconnect tree on individual branches and applying the immortality condition to these individual branches makes the EM assessment over optimistic. While all individual branches can satisfy the condition of immortality, the interconnect tree can be mortal [9]. In addition, the presence of residual stresses in the interconnect wires and possible variation of these stresses across on-chip interconnect undermines the procedure of outfiltration of immortal branches based on Blech effect (3). Indeed, we need to compare the $(j \times L)$ product calculated for the each interconnect tree with the variable critical product, different for different branches

$$(j \times L)^i_{\mathrm{crit}} = \frac{\Omega\Delta\sigma^i}{eZ\rho}; \quad \sigma^i_{\mathrm{init}} + \Delta\sigma^i = \sigma_{\mathrm{crit}}. \tag{4}$$

Here, $\sigma^i_{\mathrm{init}}$ is the residual stress existing in the interconnect branch before EM stressing was applied. $\Delta\sigma^i$ is the stress developed in the branch after EM stressing was applied. Hence, the critical product is not a constant anymore but a variable, which depends on branch location and relates to all possible stress sources. Thus, in the case of the chip-scale EM assessment, in addition to the required assessments of temperature and current density the proper assessment of residual stresses is a plus. Hence, new, physics-based MTTF compact model, which is free of all discussed flaws related to the Black–Blech formulation, should be developed.

In this paper, we try to mitigate the mentioned problems for full-chip EM assessment and signoff techniques. We propose a novel approach and techniques for physics-based EM assessment in power delivery networks of chips. The new approach consists of the following contributions.

1) Instead of considering the failure of a single interconnect branch, we consider the failure criterion as the increase in the voltage drop above the threshold level, caused by the EM-induced resistance increase of the individual branches. The new approach takes full

account of essential redundancy for current delivery existing in the P/G networks.

2) We propose the new method to calculate the EM-induced resistance increase of the individual branches in terms of the recently developed physics-based formalism for void nucleation and growth.
3) We develop a novel approach to calculate the void nucleation times in the group of branches comprising the interconnect tree. We then develop a new technique for calculating the hydrostatic stress evolution inside a multibranch interconnect tree, which allows to avoid over optimistic prediction of the time-to-failure (TTF) made with the Blech–Black analysis of individual branches of an interconnect tree.
4) Finally, we model the resulting P/G networks as time-varying linear networks, which was solved in the EM-time scale to estimate the time-varying voltage drops of P/G networks due to the EM effects over time and the resulting full-chip EM failure time.

Experimental results obtained on a number of International Business Machines Corporation (IBM) power grid benchmark circuits show that the proposed method will lead to less conservative estimation of the lifetime than the existing Black–Blech-based methods. It also reveals that the EM-induced failure is more likely to happen at the place where the hydrostatic stress predicted by the initial current density is large and is more likely to happen at longer times when the saturated void volume effect is taken into account.

This paper is organized as follows. Section II reviews the physics of EM. Section III introduces the physics-based models for void nucleation and growth. It also discusses the interconnect tree-based stress analysis. Section IV presents the proposed new power grid reliability analysis method using the physics-based EM models. The experimental results are discussed in Section V. Section VI concludes this paper. The Appendix discusses the prevoiding stress evolution and the postvoiding stress evolution accompanying the void shape evolution and void motion.

## II. Electromigration Fundamentals

EM is a physical phenomenon of the migration of metal atoms along a direction of the applied electrical field. Atoms (either lattice atoms or impurities) migrate toward the anode end of the metal wire along the trajectory of conducting electrons. This oriented atomic flow, which is caused mostly by the momentum exchange between atoms and the conducting electrons, results in metal density depletion at the cathode, and a corresponding metal accumulation at the anode end of the metal wire. This depletion and accumulation happen because atoms cannot easily escape the metal volume. The rate of EM, as defined by the Nernst–Einstein equation, depends on the atomic diffusivity, meaning different materials are characterized by different rates of EM. Typical interconnect metals, such as copper (Cu) and aluminum (Al), are prone to EM, due to their high self-diffusivity. Refractive metals, such as tungsten, tantalum, and titanium, demonstrate strong resistance to EM. Because of this big difference in diffusivities of the conducting and barrier metals the interconnect tree is the EM reliability unit of the P/G interconnect. Thin layers of refractive metals form the diffusion barriers for Cu atoms, preventing them from diffusing into interlayer dielectric (ILD) and intermetal dielectric (IMD). When metal wire is embedded into a rigid confinement, which is the case with interconnect metallization, the intention of the wire volume changes (induced by the atom depletion and accumulation due to migration) create tension at the cathode end and compression at the anode end of the line. Over time, the lasting unidirectional electrical load increases these stresses, as well as the stress gradient along the metal line. In some cases, usually when a line is long, this stress can reach critical levels, resulting in a void nucleation at the cathode and/or hillock formation at the anode end of line (Fig. 2). Different physical mechanisms can be responsible for generating these damages. In the case of voiding, existing cohesive or interfacial micro-cracks near or at the barrier/Cu interfaces can develop into a void by action of the appropriate stresses. Hillock formation, which is a compression-induced extrusion of metal into the surrounding dielectric, that can cause a shortage between neighboring metal lines, can be initiated by micro-cracks in the adhesion/barrier layers.

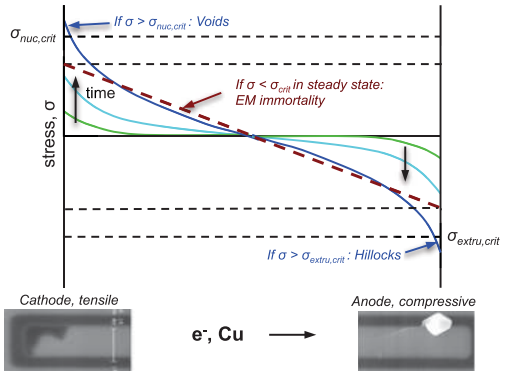


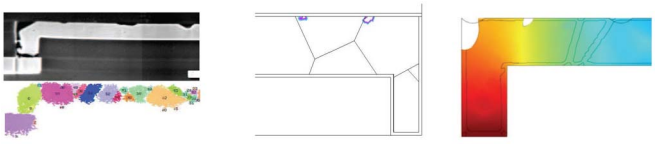

Fig. 2. Stress development and distribution in EM [10].

In the case, when an initially void-less confined metal line is stressed with the electric current density a void-related failure process consists of two steps: 1) void nucleation and 2) void growth to the critical volume resulting the critical (say, for example, 10%) increase of line resistance. Void nucleates near the cathode edge of line when the ever increasing tensile stress creates a condition for a stable growth of flaws located at the metal/barrier interface [11], [12]. An estimation of the critical stress $\sigma_{\text{crit}}$ needed for forming the growing void on the basis of the classical model of the homogeneous nucleation [13] can be found in [11] and [12]. It is shown that introduction of a spherical flaw of a radius $r$ into a solid stressed with a tension $\sigma$ changes its free energy as

$$\Delta F(r) = 4\pi r^2\gamma - \frac{4}{3}\pi r^3\sigma. \tag{5}$$

Here, $\gamma$ is the surface energy per unit area, $4\pi r^2\gamma$ is the increase of the free energy by flaw insertion; $4\pi r^3\sigma/3$ is the work done by the stress $\sigma$ to relocate atom, originally occupying the flaw volume, to the solid. Analysis of the (5) shows that the growth of the flaw with an initial size exceeding $r_{\text{crit}} = 2\gamma/\sigma$ reduces the free energy. Assuming that a void can be originated from a pre-existing flaw only, we can conclude that the flaw with the initial size $r_f$ will grow if the stress exceeds the value

$$\sigma_{\text{crit}} = \frac{2\gamma}{r_f}. \tag{6}$$



(a) (b) (c)

Fig. 3. (a) Transmission electron microscopy picture of voids nucleated at the top interface [14]. (b) and (c) Simulated kinetics of the void nucleation at the triple points and growth (electron flow from right to left) [15]. (c) Simulated growth of the line corner void by scavenging the vacancy flux and agglomerating with the small voids drifting along the top interface [16].

The assumption about the pre-existing flaws needed for the void nucleation is supported by calculations done by Gleixner and Nix [11]. They have demonstrated that an enormous energy is required for the homogeneous nucleation of the critical void by agglomeration of vacancies. But their estimation, performed with the representative values of $\gamma = 1$ J/m$^2$, shows that a pre-existed flaw with the size of 4 nm will start growing when the hydrostatic stress will reach the level of 500 MPa. Hence, the void nucleation time $t_{\text{nuc}}$ can be determined from the known kinetics of stress evolution caused by electric current density stressing as the instant in time when stress reached the critical level of $\sigma_{\text{crit}}$ (Fig. 2).

In addition to voids nucleated at the cathode end of line, where a divergence in atomic flux happens (atom flux is terminated at the barrier interface), additional voids can be nucleated down to the polycrystalline metal line toward the anode end at any location characterized by the atom flux divergence. These are the triple points formed by intersections between grain boundaries (GBs) and the top dielectric barrier (typically composed of SiCN), or contacts between three neighbor grains [Fig. 3(a) and (b)]. Those triple points where the number of outward diffusion channels exceeds the number of inward channels, which can be responsible for the flux divergence, can develop depletion in metal density, leading to the development of tension and possible void nucleation. As shown in Fig. 3(c), two major mechanisms of void growth are as follows.

1) Scavenging the vacancies that migrate to the void due to the stress gradient between the void surfaces (zero stress) and the surrounding metal (tensile stress).
2) Agglomeration of voids traveling along the metal line toward the cathode end (against the electron flow) due to the capillarity effect.

It should be mentioned that this paper does not consider the hillock-induced failure since its less frequent appearance in comparison with the void-induced failure. Experiments demonstrate that the level of stress needed for the generation of hillocks is much higher than in the case of voiding. In addition, more severe process-induced flaws, such as ruptures of the barrier liners, should be presented, that are also less frequent than small cavities playing a precursor role for voiding.

Thus, in order to predict the degradation kinetics of the resistance of P/G nets and corresponding voltage drop degradation we should calculate the cooperative stress evolution and voiding dynamics everywhere inside every tree. Traditional simulation techniques addressing this problem as well as the novel approach proposed recently are described in the following sections.

## III. Physics-Based EM Analysis Method

Solution of the system of coupled partial differential equations (PDEs) describing the evolution of concentrations of vacancies and atoms, plated at GB and interfaces of the interconnect line embedded in ILD/IMD confinement, together with the force balance equation, describing the evolution of stress components inside this line, and Laplace equation describing the current density distribution, can provide the kinetics of stress distribution everywhere inside analyzed line [15], [17]. A proper introduction of the variation of the grain sizes and anisotropies of grain mechanical properties and atomic diffusivities along the GBs and interfaces allow simulating evolution of stress distribution and vacancy concentration up to the instant in time when the void is nucleated. Postvoiding evolution of stress distribution along with the void movement and evolution of its shape can be obtained by a modified phase-field approach [18]. Original system of equations is combined with an additional PDE describing the evolution of introduced order parameter equal to 1 and $-1$ in the metal and void correspondingly, with smooth transition between them in the void interface. It allows describing a void and a metal as two different phases, and coupling the phase-field equation with EM model by reducing the values of material properties for the space occupied by the growing void to zero by means of the order parameter. This modeling approach is described in the Appendix.

This formalism has allowed simulating of many interesting cases such as effect of interfaces [19] and GB [17] on the stress and vacancy concentration evolution in the confined metal branches, role of grain crystallography on voiding [14], void migration along metal line with GB [16], etc. While being successful in simulating the EM related physics in the frame of the finite-element analysis (FEA), this type of modeling cannot be employed for our purpose, which is the simultaneous analysis of stress evolution caused by the electrical load in hundreds of millions interconnect branches. A reason is the enormous size of the computational problem. To address this problem it is desirable to have analytical descriptions of the void nucleation time and kinetics of void size evolution which, while being simple enough to provide fast simulations, should contain the dependencies on all major parameters such as material properties, segment geometries, grain size and morphology, temperature, diffusivities, etc.

### A. Nucleation Phase and Nucleation Time

Such analytical formulation has been proposed and developed by Korhonen *et al.* [20] and further developed by other researchers (see [12], [21], [22]). In a simple 1-D approximation, which was used by Korhonen *et al.* [20] for deriving a model of the stress evolution in a confined and electrically loaded metal line, a standard assumption was employed: the divergence of the atomic flux $\Gamma_A$ generates a volumetric stress $\Theta$

$$\frac{\partial \Theta}{\partial t} = \Omega \frac{\partial \Gamma_A}{\partial x}. \tag{7}$$

Here, $\Gamma_A$ is a total atomic flux comprised by the fluxes caused by the EM force and stress gradient

$$\Gamma_A = \frac{D_a}{\Omega k_B T}\left(eZ\rho j + \frac{\partial \sigma}{\partial x}\right). \tag{8}$$

Here, $D_a$ is the effective atomic diffusivity, $eZ$ is the effective charge of migrating atoms, $B$ is the effective bulk elasticity

modulus, $\Omega$ is the atomic lattice volume, $\rho$ is the metal resistivity, $j$ is the current density, $k_B$ is the Boltzmann constant, $T$ is the temperature, $x$ is the coordinate along the line, and $t$ is time. We assume here that the lattice cite concentration is taken as $N_a = 1/\Omega$. Substituting the total flux $\Gamma_A$ and the volumetric strain as $\Theta = \sigma/B$ in (7) provides

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\frac{D_a B \Omega}{k_B T}\left(\frac{eZ\rho j}{\Omega} + \frac{\partial \sigma}{\partial x}\right). \tag{9}$$

Equation (9) is the well-known Korhonen's equation describing evolution of the stress distribution along the confined metal line caused by the applied electric current [4]. A number of the simplifying assumptions are adopted: it is assumed that the confinement (metal and dielectric barriers) is absolutely rigid, the atom diffusivity does not depend on stress; vacancy concentration is in the equilibrium with stress at any instant in time everywhere including grain interior; stress evolution is caused just by the atomic flux divergence, the additional stress evolution due to vacancy equilibration with the stress is not accounted. It should be mentioned, while the derivation of (9) was done for 1-D line, the employed effective valence $Z$ and atomic diffusivity $D_a$ allow accounting some elements of wire texture and 3-D geometry [5].

A solution to this initial-boundary value problem in the case of a finite line with the diffusion blocking ends located at $x = 0$ and $L$, where $L$ is the line length, loaded with the dc current density $j$ was obtained by the method of separation of variables in [4]

$$\sigma = \sigma_T + \frac{eZ\rho jL}{\Omega}\left\{\frac{1}{2} - \frac{x}{L} - 4\sum_{n=0}^{\infty}\frac{\cos\left(\frac{(2n+1)\pi x}{L}\right)}{(2n+1)^2\pi^2}e^{-\kappa\frac{(2n+1)^2\pi^2}{L^2}t}\right\}. \tag{10}$$

Here, $\sigma_T$ is the residual stress pre-existing in the line, $\kappa = D_a B\Omega/k_B T$, and $D_a = D_0\exp\{-((E_D - \Omega^*\sigma_T)/k_B T)\}$, where $E_D$ is the activation energy of the atom diffusion, and an activation volume $\Omega^* \approx 0.95\ \Omega$ is the combination of the vacancy formation and the migration volumes [23].

Approximate value of void nucleation time extracted from (10), which is determined as an instant in time when the stress at the cathode end of line ($x = 0$) is reached $\sigma_{\text{crit}}$ is

$$t_{\text{nuc}} \approx \frac{L^2 k_B T}{2D_a B\Omega}\ln\left\{\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_T + \frac{eZ\rho jL}{2\Omega} - \sigma_{\text{crit}}}\right\} \tag{11}$$

where $D_a \approx N_V D_V = D_0\exp(-((E_V + E_{\text{VD}} - \Omega^*\sigma_{\text{crit}})/k_B T))$. Here $N_V$ and $D_V$ are the vacancy concentration and vacancy diffusivity, $E_V$ and $E_{\text{VD}}$ are the activation energy of vacancy formation and diffusion, $\sigma_T$ is the thermal stress developed in the metal line confined in the ILD/IMD dielectric during cooling from the zero stress temperature $T_{\text{ZS}}$ down to the temperature of use condition.

### *B. Growth Phase and the Rate of Wire Resistance Change*

The second phase is the void size growth mode. Void is formed at $t_{\text{nuc}}$ and grows at $t > t_{\text{nuc}}$. It is clear that only the void growth mode can be responsible for the line resistance degradation. Indeed, continuous reduction of the metal line cross section area at the location of the growing void, which in the extreme case forces the current to flow through the highly resistive metal diffusion barriers when void cuts the entire metal cross section, is accompanied by line resistance increase. A void nucleation, which represents a transformation of the process-induced flaws located at the metal/passivation interface into the stable growing void that happens when a level of the EM-induced hydrostatic tensile stress reaches the critical, cannot introduce any noticeable changes in the line resistance. Hence, the kinetics of EM-induced degradation of the line resistance should be characterized by the presence of an initial incubation time, needed for void nucleation, followed by the resistance increase caused by the void growth. Exactly this type of kinetics is observed in experiments [24]. As a result, the P/G network becomes a time-varying network and its voltage drops will keep changing over time. An accurate description of the void growth kinetics is quite complicated. It involves atom migration along the void surface and the atom transfer into the metal under the action of electric current density and stress field. When the postvoiding evolution of stress is considered, two different cases characterized by different initial conditions at the moment when the electric current density is applied should be analyzed. The first one is the case when the thermal stress-induced void pre-exists inside analyzed segment.

At the equilibrium the stress everywhere in the metal line is zero [12], [25]. Later, upon loading the line with electric current, the stress is developing along the growth of the pre-existing void. In this case, initially, the void volume grows linearly with current density [12], [25]. This type of kinetics, strictly speaking, is valid in the cases of the unconfined line edge drift [26], and the initial growth of a saturated void, pre-existed in the confined metal line [25], when the stress in the line has a negligible effect on the movement of the free surface. Quite different void volume evolution takes place when an initially void-less metal line embedded into the rigid confinement is stressed with electric current density. In this case we have a void evolution consisting of two steps: 1) already discussed void nucleation and 2) void growth. A portion of metal neighboring the surface of growing void is under essential tension, which can be estimated from (12). A large stress gradient, which is developed between the zero normal stress void surface and the surrounding metal with the hydrostatic stress of the order of magnitude of $\sigma_{\text{crit}}$, pushes the atoms to escape the void surface toward the metal bulk

$$\sigma_{\text{crit}} = \sigma_T + \frac{eZ\rho jL}{\Omega}\left\{\frac{1}{2} - 4\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2\pi^2}e^{-\kappa\frac{(2n+1)^2\pi^2}{L^2}t_{\text{nuc}}}\right\}. \tag{12}$$

Fig. 4 shows the evolution of stress in the initially void-less metal line taking place after the void nucleation. This result was obtained from the numerical solution of the system of PDEs presented in the Appendix describing the void evolution with COMSOL FEA tool [27]. It can be seen from Fig. 4 that in initial times, the atomic flux at the void surface is mainly determined by the large stress gradient. As it was demonstrated in [28], the initial evolution of the void volume does not depend on the electric current density contrary to the

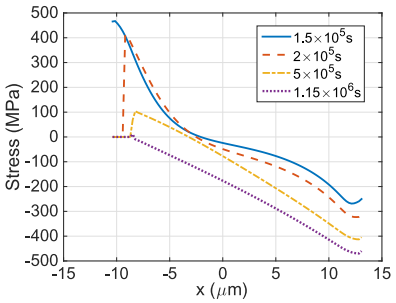



Fig. 4. Postvoiding stress evolution when the void was nucleated by electrical stressing calculated with COMSOL FEA tool.

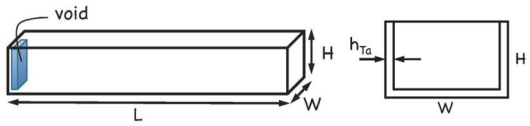



Fig. 5. Schematics of the line geometry.

case of the line edge drift approximation characterized by the linear dependence of the initial void growth rate on the current density. At long-time limit the derived solution provides the same steady state with the stress linearly distributed along the line as in the case of preexisted void. In this paper, we use the conventional method (pre-existing void case) to estimate void volume evolution and preserve the latter case for future analysis.

Void growth is accompanied by redistribution of the extra atoms, previously occupied the void volume, through the metal line. It reduces tensile stress at the cathode side of the line and increases compressive stress at the opposite anode side. Accepting that the drift velocity of the void edge relates to atomic flux ($J = (D_a eZ\rho j/\Omega k_B T)$) as $\vartheta = \Omega J$ [12] we can express it as

$$\vartheta = \frac{D_a}{k_B T} eZ\rho_{\mathrm{Cu}} j. \tag{13}$$

Kinetics of the change of the branch resistance can be described as

$$\Delta r(t) = \vartheta \cdot (t - t_{\mathrm{nuc}}) \cdot \left[ \frac{\rho_{\mathrm{Ta}}}{h_{\mathrm{Ta}}} \cdot \frac{1}{2H + W} - \frac{\rho_{\mathrm{Cu}}}{HW} \right] \tag{14}$$

where $\rho_{\mathrm{Ta}}$ and $\rho_{\mathrm{Cu}}$ are the resistivities of the barrier material (Ta/TaN) and Cu, $W$ is the line width, $H$ is the Cu thickness, and $h_{\mathrm{Ta}}$ is the barrier layer thickness schematically shown in Fig. 5. It is assumed that a void occupies the whole cross section of the line and the current is forced to flow through the barrier layer at that portion of the line. Void growth continues until its volume reaches the so-called saturation value. This so-called saturated void is formed when the flux of atoms previously located in the part of metal, which is consuming by the growing void, is balanced by the back flux of atoms generated by the gradient of the building up stress. If the wire is stressed under constant current density, we can derive the void saturated volume by using the following equation [12]:

$$\frac{V_{\mathrm{SS}}^{\mathrm{volm}}}{V_{\mathrm{line}}^{\mathrm{volm}}} = \frac{\sigma_T}{B} + \frac{eZ\rho jL}{2B\Omega}. \tag{15}$$

Here, $V_{\mathrm{SS}}^{\mathrm{volm}}$ is the void saturated volume and $V_{\mathrm{line}}^{\mathrm{volm}}$ is the total volume of the metal line. Expression (15) was obtained under

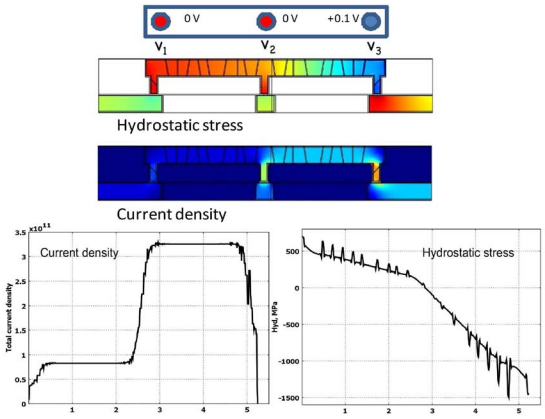



Fig. 6. Current density and stress distributions in a metal tree.

the assumption of a constant current density load. On the other hand, when a constant voltage $V$ is applied to the line ends, then the change in the current density, caused by the growing void (14), should be taken into account. In other words, the current density is no longer constant in this case. Based on the obvious relations $j(t) = j_0/(1 + \Delta r(t)/r_0)$ and $\Delta r(t)/r_0 \approx V^{\mathrm{volm}}(t)/V_{\mathrm{line}}^{\mathrm{volm}}$, where $j_0$ and $r_0$ are the current density and line resistance before void was nucleated, the condition of the formation of saturated void volume takes the form

$$\frac{V_{\mathrm{SS}}^{\mathrm{volm}}}{V_{\mathrm{line}}^{\mathrm{volm}}} = \left( \frac{\sigma_T}{B} + \frac{eZ\rho j_0 L}{2B\Omega} \right) \Big/ \left( 1 + \frac{eZ\rho j_0 L}{2B\Omega} \right). \tag{16}$$

Based on (13), (14), and (16) we can derive the void growth kinetics

$$\frac{V^{\mathrm{volm}}(t)}{V_{\mathrm{line}}^{\mathrm{volm}}} = \frac{D_a eZ\rho j_0}{k_B TL \cdot \left( 1 + \frac{V^{\mathrm{volm}}(t)}{V_{\mathrm{line}}^{\mathrm{volm}}} \right)} \cdot (t - t_{\mathrm{nuc}}) \tag{17}$$

and time needed to reach the void saturated volume

$$t_{\mathrm{VS}} = t_{\mathrm{nuc}} + \frac{k_B TL^2}{2B\Omega D_a} \cdot \left( 1 + \frac{2\sigma_T \Omega}{eZ\rho j_0 L} \right). \tag{18}$$

Upon reaching the saturation, the further void growth is stopping and the line resistance comes to saturation. This steady state lasts as long as the applied voltage is keeping constant. When the voltage is changed the void size and line resistance again start evolving toward the new steady state.

### C. Tree-Based EM Analysis Method

The proposed physics-based EM assessment model and the simulation flow discussed above were attributed to a single confined interconnect line. But, as it was mentioned already, the modern P/G networks consist of large interconnect trees (Fig. 1). These trees might have multiple voltage inputs/outputs and current source ports represented by interlayer vias and contacts. The major difference between iso-lines and individual branches of interconnect trees is an absence of blocking boundaries at one or both ends of the branches. It prevents atoms from accumulation/depletion and eliminates related stress buildup at the branch ends, and, hence, makes traditional immortality assessment as a groundless. Fig. 6 shows distributions of the current density and hydrostatic stress developed in the three terminal metal segments

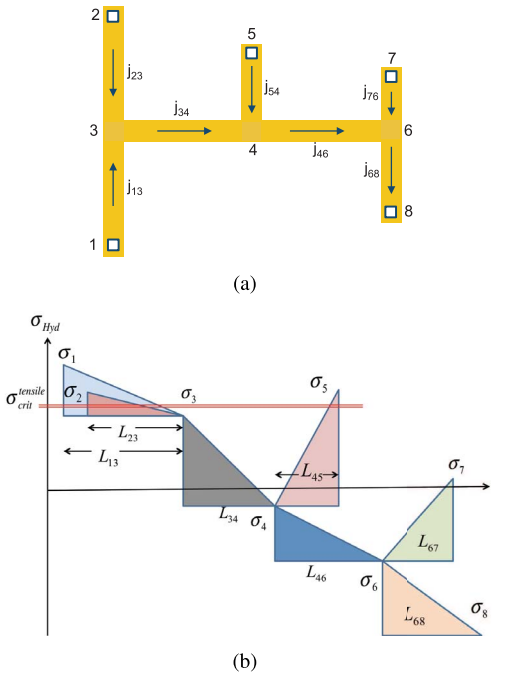



Fig. 7. (a) Example of an interconnect tree. (b) Hydrostatic stress distribution in the interconnect tree.

located at the upper metal layer. Two vias are used as electron flow inlets ($v_1, v_2$) and one positively biased as outlet ($v_3$). The hydrostatic stress obtained from the solution of the described in the Appendix system of PDEs with the FEA tool COMSOL [27] demonstrates the two-slope distribution resulted by the intra branch interaction. It makes clear that in order to explain such distribution we should consider the whole metal tree for stress analysis but not separated single wires [9]. Below we will demonstrate how it affects the developed EM assessment flow.

Let us assume that for a given interconnect tree a distribution of the dc current densities and the current flow directions are known, and the void-less steady state was achieved. We will remove the void-less assumption in the course of development. In this case the steady state means that all atomic fluxes are vanished. It can be reached if the atomic flux in each branch caused by electron flow is balanced by the atomic backflow caused by stress gradient. It provides a simple estimation of the stresses would be developed at the cathode and anode ends of each branch

$$\sigma_i^c - \sigma_j^a = \triangle\sigma_{ij} = \frac{eZ\rho j_{ij}L_{ij}}{\Omega}. \tag{19}$$

Here, $\sigma_i^c$ and $\sigma_j^a$ are the hydrostatic stresses at the cathode (electron flow inlet) and anode (electron flow exit) ends of the $ij$-branch. Fig. 7 shows an example of the multibranch interconnect tree. Equation (19) allows one to obtain the stresses at all branch ends as functions of the "reference" stress developed at any arbitrary chosen end. This uncertainty can be easily eliminated by adding to consideration the atom conservation condition. Indeed, due to unblocked ends of branches the atom redistribution between branches causes the final stress distribution, but keeps the total amount of atoms unchanged. It provides the equation for determination of the missing reference stress

$$\sum_{i=1}^{k}\left[\sigma_i - \left(\sigma_T + \frac{eZ\rho j_{ij}L_{ij}}{2\Omega}\right)\right]L_{ij} = 0. \tag{20}$$

Equation (19), together with the atom conservation condition (20) allow obtaining the steady state stress distribution in the interconnect tree as shown in Fig. 7(b). Calculated stresses should be compared with the critical stress ($\sigma_{\text{crit}}$) responsible for the void nucleation. If any calculated stress exceeds $\sigma_{\text{crit}}$ then the time for void nucleation at the cathode, characterized by the biggest stress $\sigma_m$, should be calculated as

$$t_{\text{nuc}}^m \approx \frac{L_{\text{max/min}}^2}{2D_0} e^{\frac{E_V+E_{\text{VD}}}{k_BT}} \frac{k_BT}{\Omega B} \exp\left\{-\frac{\Omega^*\sigma_{\text{crit}}}{k_BT}\right\} \times \ln\left\{\frac{\sigma_{m(j_1,j_2,\ldots,j_n)} - \sigma_T}{\sigma_{m(j_1,j_2,\ldots,j_n)} - \sigma_{\text{crit}}}\right\}. \tag{21}$$

Equation (21) is the extension of (11) for the case of multibranch interconnect tree. Here, $\sigma_{m(j_1,j_2,\ldots,j_n)}$ is the steady state stress at the cathode end of a branch characterized by the biggest tensile stress in the considered interconnect tree, and $n$ is the number of branches, $L_{\text{max/min}}$ is the distance inside the tree, which connects the cathode (maximal tensile stress) with anode (maximal compressive or minimal tensile stress). In a case when several cathodes reveal stresses exceeding, the nucleation time still should be calculated for the cathode with the biggest stress. Indeed, the described method for finding the cathode with the steady state hydrostatic stress exceeding $\sigma_{\text{crit}}$ is just a simple way to find a location inside a tree where the $\sigma_{\text{crit}}$ is first developed. A correct stress distribution inside considered tree at the moment of time when the first void is nucleated, and, which is most important, during the time when the void evolves, can be derived from the solution of the system of equations, similar to (9), describing the simultaneous stress evolution in all branches of the tree. Boundary conditions (BCs) representing the continuity of stress and the atomic flux conservation at the branch joints should be employed. A zero normal stress BC should be used at the edges of the growing voids. Fig. 8 demonstrates evolution of the prevoid stress distributions along the branches of T-shape tree, which was obtained from the solution of stress evolution equations [29], [30]. Analysis of the time-dependent stress distributions in all three branches provides that the largest steady state stress would be developed at the cathode of the branch "3." If we accept, just for illustration purposes, that $\sigma_{\text{crit}}$=200 MPa, then Fig. 8(c) shows that indeed a void is nucleated at the branch 3 cathode area at $t_{\text{nuc}} = 1 \times 10^7$ s. The biggest stress in the branch "1" at this time will be 150 MPa, which is smaller than $\sigma_{\text{crit}}$. Starting from this instant in time the stress evolution kinetics will not be described any more by the same dependencies that were valid for $t < t_{\text{nuc}}$. For times $t > t_{\text{nuc}}$ stress evolution inside all branches is described by the same system of equations but with the different BC at the cathode end of the branch 3, which now represents the edge of the growing void, i.e., $\sigma = 0$. Initial condition for the new solution will be the stress distribution at obtained for the void-less case [28].

As it was shown in [28], a nucleated void reduces the stress everywhere inside the interconnect tree. Depending on the current densities in different branches and the pace of atom redistribution through the tree branches, the first

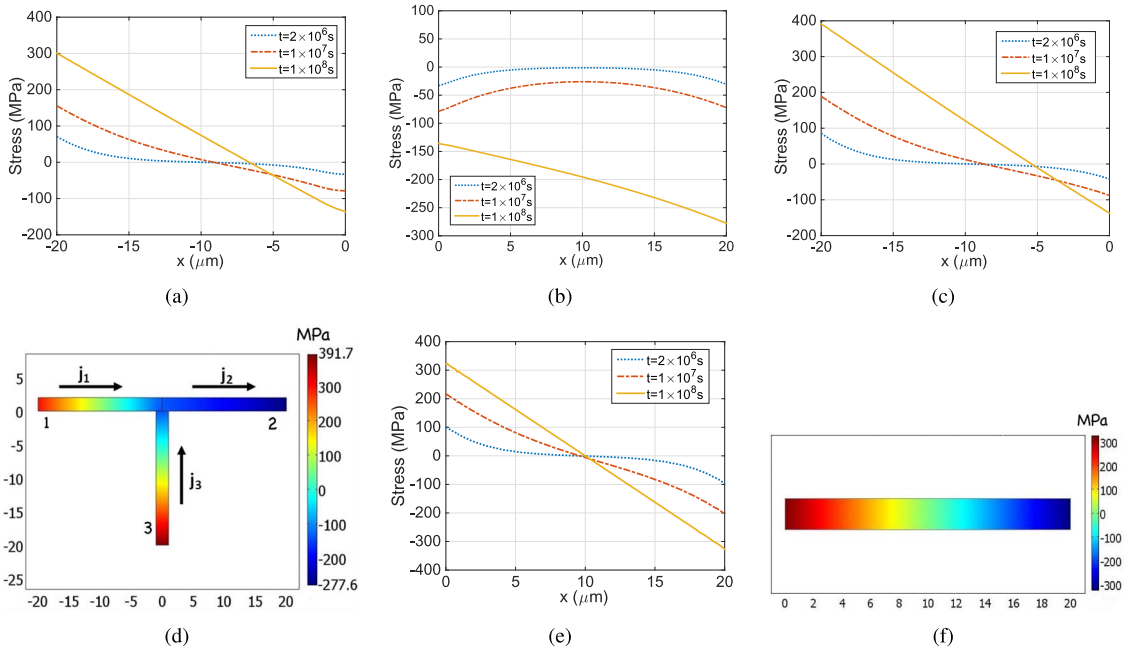



Fig. 8. Evolution of the stress distribution along the branches. (a) Line 1, (b) line 2, (c) line 3 of the (d) T-shaped tree shown. These distributions differ from (e) stress evolution functions in a (f) single line.

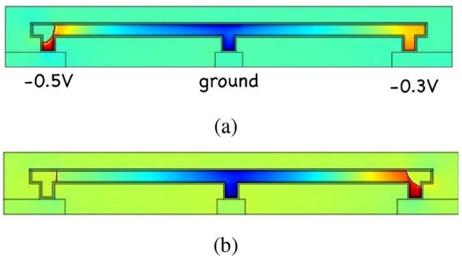



Fig. 9. Failure of a two-branch tree. (a) Voiding of the left branch, while the right branch is immortal due to smaller applied voltages. (b) Voiding of the right branch due to current density redistribution after the left segment failed.

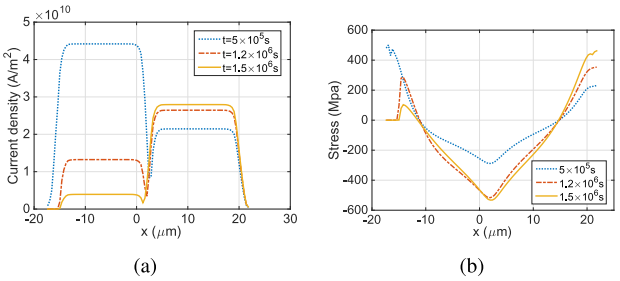



Fig. 10. (a) Current density redistribution due to left segment voiding in the structure shown in Fig. 9. (b) Hydrostatic stress evolution caused by the left segment voiding in the structure shown in Fig. 9.

nucleated void can either prevent void nucleation in other branches or not. In order to demonstrate these two possible outcomes we have simulated the EM-induced degradation in the multibranch interconnects trees (M1-V1-M2-V1-M1) with the commercial FEA tool COMSOL. Full multiphysics system of PDEs described in the Appendix was solved. Fig. 9 shows an EM-induced failure development in two-branch tree. Fig. 10(a) demonstrates the kinetics of void-induced redistribution of the current densities inside interconnect tree shown in Fig. 9. Originally, a two-branch test-tree was loaded in a way that the right branch should be immortal, while the electric current density in the left branch should be able to build up the stress required for voiding. Due to void-induced increase of the resistance of left branch, the current in the right branch increases [Fig. 10(a)], causing an increase in tensile stress at the right cathode end. As a result, the void is nucleated in the right branch as well. This process is accompanied by tensile stress reduction in the left branch due to atoms moved from the surface of expanding void to the metal bulk [Fig. 10(b)]. Thus, an accurate EM model should properly consider the void volume evolution responsible for the evolution of both the current density and stress.

This and similar simulations dealing with different electrical load conditions clearly demonstrate that both cases are possible: 1) first nucleated void prevents nucleation of other voids in the tree and 2) multiple voids are nucleated in the tree. For the sake of simplicity, we consider the former case: a nucleated void does not allow stress anywhere to reach the critical level until the current/voltage load is changed. It means that the tensile stress reduction in the void-less branches caused by the migration of atoms from the portion of the branch occupied by growing void happens faster than the increase due to the action of the electric current passing through these branches. But, the increase in the resistance of the voided branch can cause an increase of the current densities in the void-less branches and can generate the stress exceeding somewhere in the interconnect tree. Thus, a new void can be generated. All voids can grow until the saturated volumes (15) or (16) are developed. Another possible scenario is that all stresses corresponding to the adjusted current densities are smaller than $\sigma_{\text{crit}}$. In this case, the evolution of the branch resistance will stop upon development of the $V_{\text{SS}}^{\text{volm}}$. However, this state will last not long. Due to electrical interconnectivity of all trees the resistivity change in any of these trees caused by voiding will cause the change of the current densities in all neighboring trees, which will

change the volume of the saturated voids, and the resistances of the corresponding branches. That will trigger new calculation iteration. This iterative procedure will last until the voltage at any node of the P/G network reaches the threshold value or the total physical time exceeds the required lifetime.

## IV. New Power Grid Reliability Analysis Method

In this section, we present the proposed new power grid reliability analysis method using the nucleation and growth concepts and physics-based EM models we discussed in the previous sections.

### A. Power Grid Models

Because of the concern with the long-term average effects of the current, in EM related work a dc model of the power grid is generally assumed [1]. As a result, we need to consider only the EM-induced kinetics of the power grid network resistances. For the transient current sources, we will show how to compute the effective EM current and EM current sources later. In our problem formulation, each mortal wire, which is the subject to the EM impact, will start to change its resistance value upon achieving the nucleation time. As a result, we end up with the power grid systems, which is a linear, time-varying, and driven by the dc effective currents. For a power grid network with $n$ nodes

$$G(t) \times v(t) = I(t) \tag{22}$$

where $G(t)$ is a $n \times n$ time-varying conductance matrix; $I(t)$ is transient current source vector; $v(t)$ is the corresponding vector of nodal voltages. In our problem, the time scale is the EM time scale, which can be months or years.

### B. Effective-EM Current Density

EM is a long-term cumulative failure phenomenon. In reality the P/G nets are characterized by the time-dependent current densities. Small background dc currents distributed across the grid are perturbed with the unipolar pulses generated by switching cells. An intensity of these perturbations depends on the activity factors of standard cells, which are different for different workloads. In general, total current passing between the neighbor power vias is a unidirectional pulsed current. Unidirectional current and the long length of the power net segments can provide the conditions for $\sigma_{\text{crit}}$ accumulation. In this case, the criterion for determination of the effective dc current should be established [31]. The effective-EM currents will give the same lifetime as the transient waveforms. It can be understood from the following. Equation (9) provides the kinetics of the hydrostatic stress in the interconnect line caused by applied current. A simple integration provides

$$\sigma(t, x) - \sigma_0 = \frac{\partial}{\partial x}\left[\int_0^t \kappa \frac{\partial \sigma}{\partial x} dt + \kappa \frac{eZ\rho}{\Omega} \int_0^t j dt\right]. \tag{23}$$

It means that under assumptions made for derivation of [20, eq. 9], the stress distribution at any particular instant in time is governed by the time integral of the applied current density. This can be used as a justification of the replacing the current density waveforms with the time averaged dc current density. For most general cases of both uni-directional and bi-directional current densities, we have the following effective-EM current density [31], [32]:

$$j_{\text{trans,EM,eff}} = \frac{1}{P}\left[\int_0^P j^+(t)dt - R\int_0^P \left|j^-(t)\right|dt\right] \tag{24}$$

where $j^+(t)$ and $j^-(t)$ are the current densities of the positive and negative phases of the bipolar current, $R$ is the EM recovery factor determined by experiments, $P$ is the period of the current density waveform. When the current density is unidirectional, the effective-EM current density $j_{\text{trans,EM,eff}}$ is the time averaged current density. Furthermore, if the current sources are time dependent, we can compute the effective EM current sources in a similar way, which will generate the same effective current densities in each interconnect tree so that only one dc analysis is required for EM analysis at each EM time point.

### C. New Analysis Method Flow

Now, we present the new EM-induced reliability analysis algorithm and flow for P/G networks. In our formulation of the dynamic P/G networks, the wire resistance begins to change (increase) starting with the nucleation time ($t_{\text{nuc}}$). After this, their resistance changes will be computed by (14). First, we compute initial current densities $j_{0,\text{mn}}$ for each branch of every tree. Then, by using the proposed tree-based EM analysis method, we obtain the stresses for all branches in all trees. Next, we identify the trees, which are the subjects for void nucleation: hydrostatic stress at any of the tree nodes is larger than $\sigma_{\text{crit}}$. Then, we compute the set of $t^i_{\text{nuc}}$ for all suspicious branches. Branch characterized by the largest stress and smallest $t_{\text{nuc}}$ among others sets up the initial (starting) time $t_0$, which is indicated by $t_0 = \min\{t^i_{\text{nuc}}\}$ in the step 4 in the algorithm, and the branch will be included in the growth phase pool. After this, we move to next step $t_1 = t_0 + \Delta t$. The chosen time-step $\Delta t$ should be small enough to detect approximately an instant in time when the critical stress is developed in any branch of any interconnect tree. We update power grid conductance matrix $G$ due to resistance change in the wire in the growth phase, recompute current densities $j$ for each wire of each tree again, and then repeat the previous steps: stress calculation, identification of the branches satisfying $\sigma > \sigma_{\text{crit}}$, putting the most vulnerable branch into growth phase pool if reaches its $t_{\text{nuc}}$, and moving to the next step: $t_2 = t_1 + \Delta t$. We continue this process until the voltage drops at one or more nodes reach the given threshold such as 10% of the supply voltage. We identify this instant in time as the TTF of the whole P/G network. It is worth noting that, in the step 7 in the algorithm, we consider the generation of the void saturated volume when updating the branch resistance. For each branch in the growth phase, we first obtain its void volume saturation time $t_{\text{VS}}$. Then we compare $t_{\text{VS}}$ with last instant in time $t_{i-1}$. Only the branches in the growth phase pool with $t_{\text{VS}} > t_{i-1}$ have resistance increase during $[t_{i-1}, t_{\text{VS}}]$.

## V. Numerical Results and Discussion

The proposed EM assessment method is implemented in C++ on a 2.3 GHz Linux server with 132 GB memory and validated by the IBM power grid benchmark circuits [33], which has both power networks and ground networks. The power networks are used to test our method and their source current values are modified to ensure that the initial voltage

**Algorithm 1** New Power Grid EM-Induced Reliability Analysis Algorithm

**Input:** power grid networks with current inputs, time step, and technology parameters

**Output:** The time reaching the threshold voltage drop and failed branches.

1: Compute the initial effective EM current density.
2: Divide the power grids into interconnect trees with a number of connected branches.
3: Compute the steady state distributions of hydrostatic stress inside each interconnect tree.
4: Conclude all suspicious branches whose tensile stress is larger than critical stress. Calculate the nucleation time $t_0 = min\{t^i_{nuc}\}$ for the most vulnerable branch(with the largest stress).
5: Start the analysis from time $t = t_0$. Branch with nucleation time $t_0$ enters into the growth phase.
6: **while** the largest voltage drop $\leq$ threshold **do**
7: Move to next instant in time $t := t + \Delta t$, update the wire resistances for wires with void volume increase.
8: Perform the DC analysis of the power grids. Recompute the current densities of each branch.
9: Compute the steady state distributions of hydrostatic stress inside each branch based on the updated EM current densities.
10: For each tree, identify new branches with the stresses exceeding the critical value. Calculate the $min\{t^i_{\text{nuc}}\}$ for suspicious branches in the nucleation phase. If $min\{t^i_{\text{nuc}}\} \leq t$, the corresponding branch steps into the growth phase.
11: **end while**
12: Output $t$ and the failed branch

TABLE I
PARAMETERS USED IN OUR MODEL

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $E_V$ | 0.75eV [34] | $T$ | 373K |
| $E_{\text{VD}}$ | 0.65eV [34] | $\sigma_T$ | 400MPa |
| $T_{\text{ZS}}$ | 623K [35] | $Z$ | 10 [36] |
| $B$ | $1 \times 10^{11}$Pa [37, 38] | $\sigma_{crit}$ | 500MPa [11] |

drop of any node is smaller than the threshold value. In this paper, we assume the interconnect material is Cu and the power grid circuit fails when the largest voltage drop exceeds $10\%V_{\text{DD}}$. Parameters used in our model are listed in Table I.

Table II shows the power grid lifetime obtained from both Black's equation and our proposed approach. In Black's equation-based analysis, (2) is used to estimate the MTTF of single metal line, where $T_{\text{stress}} = 600$ K, $j_{\text{stress}} = 3$ MA/cm$^2$, $Ea = 0.86$ eV, and $\text{MTTF}_{\text{stress}}$ is obtained from (11) under stressed condition (use condition characteristics are the same as characteristics used in our predictive work). The current density exponent $n$ is taken as 2 when failure is nucleation dominated and is taken as 1 when failure is nucleation dominated. Two different Black's equation-based models are used to compare with the proposed method. One is series model, under which the circuit is considered to have failed as soon as any branch fails. The other is mesh model that takes redundancy into account, defining the circuit fails when it cannot deliver required amount of voltage. From the experimental results, we can observe that the Black's equation-based series model would lead to a too pessimistic prediction. The TTF estimated by Black's equation-based mesh model is more conservative than our model because it assumes infinite resistance after the predicted TTF of each branch while actually the metal line continues to conduct voltage after TTF with increasing resistance. Fig. 11(a) and (b) shows the steady state hydrostatic stress distribution predicted by the initial current density, and the initial voltage drop distribution in the metal layer that directly connects to the underlying logic blocks, respectively.

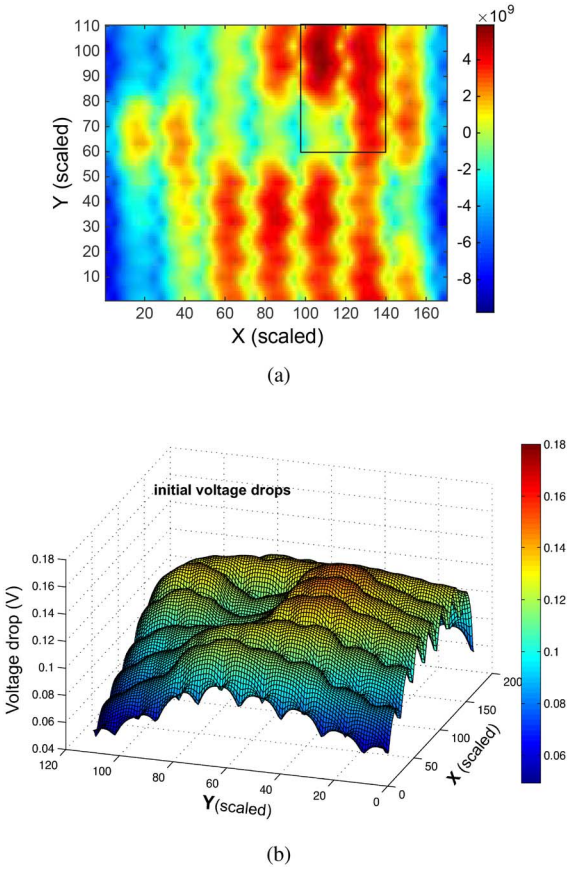


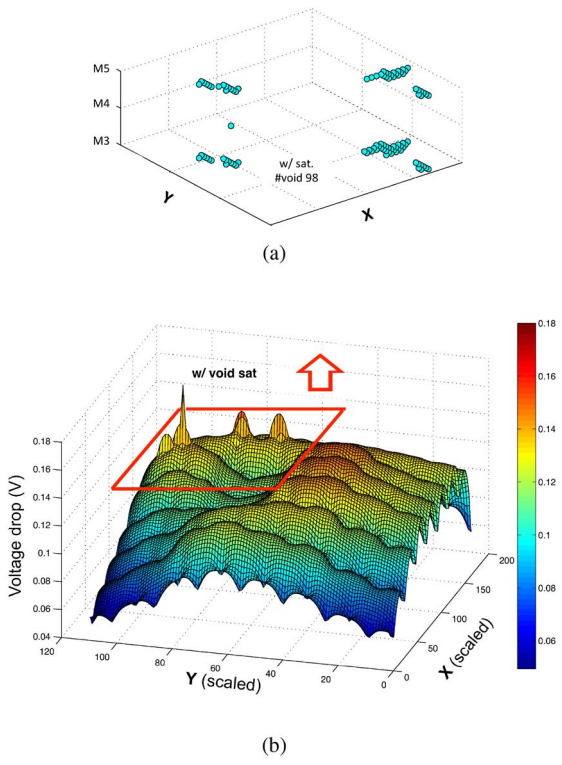

Fig. 11. Steady state hydrostatic stress (Pa) distribution predicted by the (a) initial current densities and (b) initial voltage drop (V) distribution in the layer that directly connects to circuits (M3) of IBMPG2.

The locations of voids nucleated during the lifetime of the circuit are demonstrated in Fig. 12(a). We can observe from Figs. 11(a) and 12(b) that with uniformly distributed temperature, the failure is most likely to happen at the place where the hydrostatic stress predicted by the initial current density is large. It is due to the fact that the branches with larger stress are more likely to nucleate void and, since the void growth rate is almost independent on stress, and a larger stress would result in a larger void saturated volume, which means larger resistance change, the voltage drops at these places will more likely to exceed the threshold value.

We also implemented the assessment method, which assumes that the void keeps growing once it is nucleated. Fig. 13(a) and (b) is the experimental results obtained from the model in which the void volume saturation is not considered. The distribution of the voids in the P/G net and the distribution of voltage drops in the first metal layer at the instant in time the circuit fails are depicted, respectively. It is observed

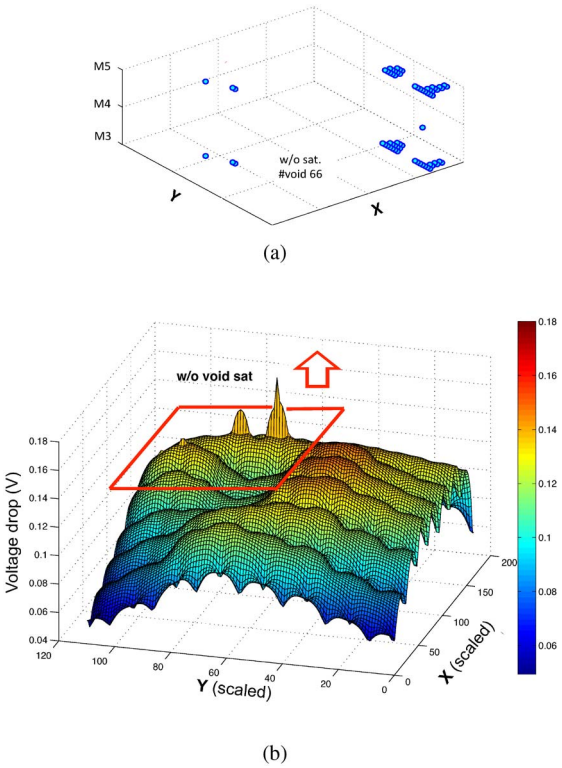
TABLE II
COMPARISON OF POWER GRID MTTF USING BLACK'S EQUATION AND PROPOSED MODEL

| Power Grid | | Time to Failure (yrs) | | | | |
|---|---|---|---|---|---|---|
| | | Black's Equation | | Proposed Model | | |
| Name | Nodes | Series | Mesh | no void sat | with void sat | Run Time |
| IBMPG2 | 61797 | 6.17 | 12.83 | 16.85 | 18.78 | 6.36 min. |
| IBMPG3 | 407279 | 12.79 | 17.90 | 23.56 | 31.97 | 5.83 hr. |
| IBMPG4 | 474836 | 13.23 | 22.27 | 26.97 | 33.41 | 14.71 hr. |
| IBMPG5 | 497658 | 4.41 | 12.34 | 19.13 | 25.16 | 40.64 min. |
| IBMPG6 | 807825 | 8.44 | 10.89 | 14.62 | 19.85 | 1.75 hr. |
| IBMPGNEW1 | 715022 | 12.85 | 13.96 | 18.84 | 25.97 | 16.78 hr. |
| IBMPGNEW2 | 715022 | 12.73 | 13.84 | 15.60 | 21.79 | 15.32 hr. |




(a) (b)

Fig. 12. (a) Void distribution and (b) voltage drop (V) distribution in the layer that directly connects to circuits (M3) of IBMPG2 at $t$ = TTF. Void volume saturation is taken into account.




(a) (b)

Fig. 13. (a) Void distribution and (b) voltage drop (V) distribution in the layer that is directly connected to circuit (M3) of IBMPG2 at $t$ = TTF. Void volume saturation is not considered.

that when the void saturated volume is taken into account, the more voids are distributed in the circuit when compared to the distribution where the voids keep growing upon nucleation. Table II summarizes the comparison between TTF obtained when considering and neglecting void volume saturation. We can conclude that for the same circuit, introducing void volume saturation would result in a larger number of nucleated voids, thus a larger number of branches in the circuit whose resistance have changed due to EM effect, but a longer TTF. It is due to the fact that when the void volume saturation has been considered, a void would stop growing when its volume reaches the saturation state. It starts growing again only when the current passing this branch increases due to voids generated in neighbor branches/trees. Thus the overall change of branch resistance is slower than in the case of neglected void volume saturation, more time and more voids will be needed for the circuit to meet the same failure criteria. So accounting for the void volume saturation in the EM analysis is necessary in order to get precise circuit lifetime.

Node voltage keeps changing with time after creation of the first void in the network and its value can be tracked as shown in Fig. 14. Effect of different average chip temperatures on P/G network's TTF is investigated. From Fig. 15, the experimental result reveals that TTF obtained from our proposed method obeys the same functional dependencies as the Black's equation, which is the Arrhenius dependence on temperature. So reducing the temperature can efficiently suppress the EM effect.

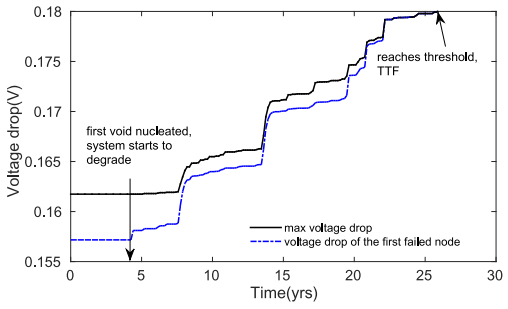



Fig. 14. Voltage drop of the first failed node and maximum voltage drop in IBMPGNEW1 change over time.

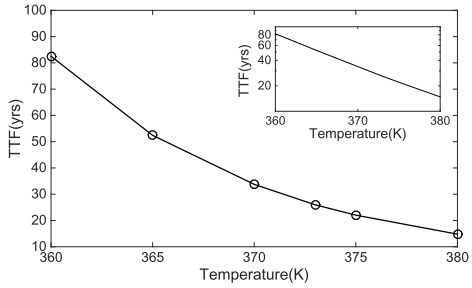



Fig. 15. Effect of temperature on TTF.

## VI. Conclusion

In this paper, a new physics-based EM modeling and assessment method has been proposed and implemented for the power grid networks of VLSI systems. The proposed method considers EM-induced degradation as a parametric failure caused by IR-drop increase above the acceptable level. Void nucleation and growth are considered for assessing the resistance growth. The new EM modeling method accounts the statistical nature of the EM phenomenon due to a random grain size distribution. It can also account the thermal and other process-induced residual stresses, which is ignored by the Black's equation-based EM assessment. Developed technique allows to assess the evolution of hydrostatic stress inside a multibranch interconnect tree for more accurate prediction of the TTF in comparison with the traditional Blech–Black analysis of individual branches of the interconnect tree. The experimental results show that the Black's equation based analysis in either weak branch or mesh approximations would lead to more pessimistic results when are compared with the proposed method. It also reveals that for the IBM P/G circuits, the EM-induced failure is more likely to happen at the places where the hydrostatic stress predicted by the initial current density is large and is more likely to happen at longer times when the saturated void volume effect is accounted.

## Appendix

This section provides the formalism, which was developed for the analysis of prevoiding stress evolution in the confined metal line loaded with the unidirectional electric current, and the further postvoiding stress evolution accompanying the void shape evolution and void motion.

### A. Prevoiding Stress Evolution

The fact is: when the deformation of metal is generated by volumetric causes such as atom density redistribution, the stress is generated by the interaction with confinement. Therefore, the theories of EM-induced stress build-up consider two main inter-related processes: 1) atomic diffusion due to electron wind force and 2) the corresponding strain–stress generation.

A vacancy mechanism of atomic diffusion accepted in these theories is valid for the interconnect metals: atoms migration through the vacant lattice sites is described as a flow of vacancies. The kinetic equation for the vacancy concentration $N(r,t)$, describing the rate of the vacancy concentration as a divergence of the vacancy flux, should take into account an equilibration of the vacancy concentration with the hydrostatic stress. This equilibrium achieves by the generation-annihilation of the vacancy-extra (plated) atom pairs. In the confined polycrystalline Cu lines, the copper interfaces with barriers and GBs are the sites for these pair generation-annihilation. The equilibrium concentration of vacancies is determined by the energy of GB or interface deformation by the plated atoms and the energy of volume relaxation around the formed vacancy. This concentration is defined by the local hydrostatic stress $\sigma_{\mathrm{Hyd}}$ and the thermal energy $k_BT$

$$N_{\mathrm{eq}} = N_0 \exp\left(f\Omega\sigma_{\mathrm{Hyd}}/k_BT\right) \tag{25}$$

where $N_0$ is the thermodynamic vacancy concentration in the stress-free state, $f$ is the ratio of the vacancy and atomic volumes. The rate of the generation-annihilation of the vacancy-plated atom pairs can be presented in the relaxation time $\tau$ approximation

$$G = -\frac{N - N_{\mathrm{eq}}}{\tau}. \tag{26}$$

A detailed description of the vacancy generation/annihilation modeling approach could be found in [16] and [17] and in the literature cited there. Thus, evolution of the vacancy concentration is described by the following continuity equation:

$$\frac{\partial N}{\partial t} + \nabla J_{\mathrm{vac}} + G = 0$$
$$J_{\mathrm{vac}} = -D\nabla N - \frac{DN}{k_BT}\left\{(1-f)\Omega\nabla\sigma_{\mathrm{Hyd}} - eZ\rho j\right\} \tag{27}$$

where $J_{\mathrm{vac}}$ is the flux of vacancies, $N$ is the vancancy concentration, and $D$ is the diffusivity of vacancies. It should be mentioned that the term $G$ is described by (26) on the interfaces and GBs and is equal to zero in the grain interiors. The diffusivity $D$ is also stress-dependent

$$D = D_0 \exp\left\{-\frac{E_D - \Omega\sigma_{\mathrm{Hyd}}}{k_BT}\right\} \tag{28}$$

and has much larger values on the interfaces and GBs, than in the grain interior.

Since the plated on GBs and interfaces extra atoms are practically immobile, the kinetics of their concentration $M$ is governed by the rate of its generation-annihilation

$$\frac{\partial M}{\partial t} + G = 0. \tag{29}$$

In order to obtain the solutions of (27)–(29), we need, as it was mentioned earlier, to couple them to the equations describing the evolution of the strain/stress and the current density taking place under the redistribution of vacancies and plated atom densities. The current density $j = \nabla V/\rho$ is determined by means of Laplace's equation. Stress is caused by a deformation of the metal line volume, which is characterized by two strain components: 1) elastic deformation, which is a result of inhomogeneities in the vacancy/plating atom distributions and interaction with the confinement and 2) inelastic deformation, due to vacancy/plating atom generation/annihilation and vacancy migration. By representing the concentration of vacancies and plated atoms in $1/\Omega$ units, we get the inelastic volume deformation as a strain tensor: $\varepsilon^{\mathrm{inel}} = -(1-f)(N - N_0) + (M - M_0)$. The generated strain includes also the elastic component $\varepsilon^{\mathrm{el}}$, which determines the stress components according to the Hook's law. The total strain is defined by the displacement vector $u$

as $\varepsilon_{ij} = (\partial u_i/\partial x_j + \partial u_j/\partial x_i)/2$ [here values of the index $i = (1, 2, 3)$ correspond to the coordinates $x_i = (x, y, z)$ and components of displacement vector $u_i = (u_x, u_y, u_z)$]. Final equations for the displacement vector components are

$$(\lambda + \mu)\frac{\partial \varepsilon}{\partial x_i} + \mu \Delta u_i + \frac{E}{3(1-\nu)}\frac{\partial (M - (1-f)N)}{\partial x_i} = 0. \quad (30)$$

Here, $\lambda$, $\mu$, $E$, and $\nu$ represent the Lame constant, shear modulus, Young's modulus, and Poisson's ratio of the metal. Coupled solution of (25)–(30) allows us to describe the kinetics of the stress, vacancy, and plating atom concentration for realistic 3-D problems.

In the case when the achieved steady state stress does not exceed the critical value $\sigma_{\text{Hyd}}^{\text{crit}}$ required for void nucleation, the wire remains immortal.

### B. Void Motion and Postvoiding Stress Evolution

If the applied current is large enough to generate stress exceeding the critical value, voids can be nucleated in the region with large tensile stress. EM theory presented above can be employed for the description of the postvoiding stress evolution, by combining it with phase-field methodology [18]. This method allows to get zero normal stress on the void surface. Voids are described as sinks for vacancies: outflow of atoms from the void surface are considered as inflow of vacancies, resulting in motion of the void-metal interface.

Phase-field method describes the void and metal regions as two different phases of the medium: an order parameter $\phi$ is introduced, which is defined as

$$\phi = \begin{cases} 1, & \text{in metal} \\ -1, & \text{in void.} \end{cases} \quad (31)$$

A smooth transition between these two phases and corresponding values of $\phi$ in a narrow region $d$ represents the void-metal interface. Evolution of the order parameter describes the interface motion that changes the distribution of two phases in space and time; hence, the term phase-fieldİ is used. The details of this approach are presented below.

The basic nonlinear equation of the model is

$$\eta\frac{\partial \phi}{\partial t} - \xi \nabla^2 \phi + \left(\phi^2 - 1\right)\phi + (\eta v)\nabla\phi = 0. \quad (32)$$

Here the viscosity $\eta$ is responsible for duration of void formation process (as it is considered below). The meaning of the parameters $\xi$ and $v$ becomes clear from the analytical solution of (32) in 1-D case

$$\phi(x, t) = \tanh\frac{x - x_0 - vt}{\sqrt{2\xi}} \quad (33)$$

where the coordinate $x_0$ corresponds to the void surface location at nucleation time instance. This solution demonstrates, that the thickness of void surface is $d = \sqrt{2\xi}$, and $v$ represents the velocity of the surface motion.

Equation (32) shows that in equilibrium, i.e., when $\partial\phi/\partial t = 0, v = 0$, the order parameter can have values 1 or $-1$. Following (31), we choose the condition $\phi(t < t_{\text{nuc}}) = 1$. Void nucleation, i.e., origination of a region with $\phi = -1$ is described by the same equation (32) by adding a term $F$

$$\eta\frac{\partial \phi}{\partial t} - \xi \nabla^2 \phi + \left(\phi^2 - 1\right)\phi + (\eta v)\nabla\phi = F\left(\sigma_{\text{Hyd}}\right). \quad (34)$$

Here the "external" force $F$ depends on the developed stress in the metal as

$$F\left(\sigma_{\text{Hyd}}\right) = -F_0 \cdot (\phi + 1) \cdot \begin{cases} 0, & \text{if } \sigma_{\text{Hyd}} < \sigma_{\text{Hyd}}^{\text{crit}} \\ 1, & \text{if } \sigma_{\text{Hyd}} \geq \sigma_{\text{Hyd}}^{\text{crit}}. \end{cases} \quad (35)$$

Here the parameter $F_0$ (along with the viscosity $\eta$) defines the duration of the nucleation process. The force (35) originates at any site where the critical tensile stress is achieved, and provides a local shift of the phase field from the initial state $\phi = 1$. This force influences on the system during a short period of time $\tau \sim \eta/F_0$, when the order parameter evolves locally in the range $-1 < \phi < 1$. As the new state $\phi = -1$ is achieved, which denotes void nucleation, the force $F$ vanishes [due to multiplier $(\phi + 1)$ in (35)].

Further dynamics of the nucleated void is described by (32), which provides the interface motion with velocity $v$. In the employed vacancy diffusion model, this velocity is proportional to the gradient of inflow/outflow flux of vacancies and gradient of the void surface flux

$$v = \nabla J_{\text{vac}} + \frac{\partial J_{\text{vac}}^{\text{surf}}}{\partial s}. \quad (36)$$

Here $s$ is a unit tangent vector, the surface flux of vacancies is determined by the directional derivative of the curvature $K$ and by the surface tension energy $g : J_{\text{vac}}^{\text{surf}} = (DNg/k_BT)(\partial K/\partial s)$.

Thus, (32) and (36) describe the dynamics of nucleated voids as evolution of regions characterized by the phase field value $\phi = -1$. It is obvious that the conductivity $(c = 1/\rho)$ and Young's modulus of metal, diffusivity of vacancies, and their generation/annihilation rate become equal to zero in the voided regions. This is done by replacing these parameters by the expressions

$$c_\phi = c\psi, E_\phi = E\psi, D_\phi = D\psi$$
$$G_\phi = G\psi, \psi = \frac{1+\phi}{2}. \quad (37)$$

Along with the definitions (37) we introduce large surface diffusivity, using an empiric parameter $\zeta >> 1$

$$D_{\text{surf}} = \zeta \cdot D \cdot (1 - |\phi|). \quad (38)$$

Combination of phase-field equations (31)–(38) with EM equations (25)–(30) represents a self-consistent model for study of EM-induced void nucleation and growth.

## REFERENCES


[1] S. Chatterjee, M. Fawaz, and F. N. Najm, "Redundancy-aware electromigration checking for mesh power grids," in *Proc. Int. Conf. Comput.-Aided Design (ICCAD)*, San Jose, CA, USA, 2013, pp. 540–547.

[2] V. Mishra and S. S. Sapatnekar, "The impact of electromigration in copper interconnects on power grid integrity," in *Proc. Design Autom. Conf. (DAC)*, Austin, TX, USA, 2013, pp. 1–6.

[3] J. R. Black, "Electromigration—A brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. 16, no. 4, pp. 338–347, Apr. 1969.

[4] M. Ohring, *Reliability and Failure of Electronic Materials and Devices*. San Diego, CA, USA: Academic Press, 1998.

[5] J. R. Lloyd, "New models for interconnect failure in advanced IC technology," in *Proc. Int. Symp. Phys. Fail. Anal. Integr. Circuits (IPFA)*, Singapore, 2008, pp. 1–7.

[6] M. Hauschildt *et al.*, "Electromigration early failure void nucleation and growth phenomena in Cu and Cu(Mn) interconnects," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Anaheim, CA, USA, 2013, pp. 2C.1.1–2C.1.6.

[7] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *J. Appl. Phys.*, vol. 47, no. 4, pp. 1203–1208, 1976.

[8] X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks," in *Proc. Design Autom. Conf. (DAC)*, San Francisco, CA, USA, 2014, pp. 1–6.

[9] S. P. Hau-Riege and C. V. Thompson, "Experimental characterization and modeling of the reliability of interconnect trees," *J. Appl. Phys.*, vol. 89, pp. 601–609, Jan. 2001.

[10] Z.-S. Choi, "Reliability of copper interconnects in integrated circuits," Ph.D. dissertation, Dept. Mater. Sci. Eng., Massachusetts Inst. Technol., Cambridge, MA, USA, Jun. 2007.

[11] R. J. Gleixner and W. D. Nix, "A physically based model of electromigration and stress-induced void formation in microelectronic interconnects," *J. Appl. Phys.*, vol. 86, no. 4, pp. 1932–1944, 1999.

[12] Z. Suo, "Reliability of interconnect structures," in *Comprehensive Structural Integrity, Interfacial and Nanoscale Failure*, vol. 8, W. Gerberich and W. Yang, Eds. Amsterdam, The Netherlands: Elsevier, 2003, pp. 265–324.

[13] F. F. Abraham, *Homogeneous Nucleation Theory*. New York, NY, USA: Academic Press, 1974.

[14] A. Kteyan, V. Sukharev, M.-A. Meyer, E. Zschech, and W. D. Nix, "Microstructure effect on EM-induced degradations in dual-inlaid copper interconnects," in *Proc. AIP Conf.*, vol. 945. Kyoto, Japan, pp. 42–55, 2007.

[15] V. Sukharev, "Physically based simulation of electromigration-induced degradation mechanisms in dual-inlaid copper interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 9, pp. 1326–1335, Sep. 2005.

[16] V. Sukharev, A. Kteyan, E. Zschech, and W. D. Nix, "Microstructure effect on EM-induced degradations in dual inlaid copper interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 1, pp. 87–97, Mar. 2009.

[17] V. Sukharev, E. Zschech, and W. D. Nix, "A model for electromigration-induced degradation mechanisms in dual-inlaid copper interconnects: Effect of microstructure," *J. Appl. Phys.*, vol. 102, no. 5, 2007, Art. ID 053505.

[18] D. N. Bhate, A. F. Bower, and A. Kumar, "A phase field model for failure in interconnect lines due to coupled diffusion mechanisms," *J. Mech. Phys. Solids*, vol. 50, no. 10, pp. 2057–2083, 2002.

[19] V. Sukharev and E. Zschech, "A model for electromigration-induced degradation mechanisms in dual-inlaid copper interconnects: Effect of interface bonding strength," *J. Appl. Phys.*, vol. 96, no. 11, pp. 6337–6343, 2004.

[20] M. A. Korhonen, P. Borgesen, K. N. Tu, and C.-Y. Li, "Stress evolution due to electromigration in confined metal lines," *J. Appl. Phys.*, vol. 73, no. 8, pp. 3790–3799, 1993.

[21] J. J. Clement, "Reliability analysis for encapsulated interconnect lines under DC and pulsed DC current using a continuum electromigration transport model," *J. Appl. Phys.*, vol. 82, no. 12, pp. 5991–6000, 1997.

[22] M. E. Sarychev, Y. V. Zhitnikov, L. Borucki, C.-L. Liu, and T. M. Makhviladze, "General model for mechanical stress evolution during electromigration," *J. Appl. Phys.*, vol. 86, no. 6, pp. 3068–3075, 1999.

[23] M. J. Aziz, "Thermodynamics of diffusion under pressure and stress: Relation to point defect mechanisms," *J. Appl. Phys.*, vol. 70, no. 21, pp. 2810–2812, 1997.

[24] C.-K. Hu and R. Rosenberg, "Capping layer effects on electromigration in narrow Cu lines," in *Proc. AIP Conf.*, vol. 741. Austin, TX, USA, 2004, pp. 97–111.

[25] J. He and Z. Suo, "Statistics of electromigration lifetime analyzed using a deterministic transient model," in *Proc. AIP Conf.*, vol. 741. Austin, TX, USA, 2004, pp. 15–26.

[26] I. A. Blech and E. Kinsbron, "Electromigration in thin gold films on molybdenum surfaces," *Thin Solid Films*, vol. 25, no. 2, pp. 327–334, 1975.

[27] *COMSOL Multiphysics*. [Online]. Available: http://www.comsol.com, accessed Sep. 2015.

[28] V. Sukharev, A. Kteyan, and X. Huang, "Post-voiding stress evolution in confined metal lines," *IEEE Trans. Device Mater. Rel.*, Dec. 2015, doi: 10.1109/TDMR.2015.2508447.

[29] V. Sukharev, X. Huang, H.-B. Chen, and S. X.-D. Tan, "IR-drop based electromigration assessment: Parametric failure chip-scale analysis," in *Proc. Int. Conf. Comput.-Aided Design (ICCAD)*, San Jose, CA, USA, 2014, pp. 428–433.

[30] H.-B. Chen, S. X.-D. Tan, V. Sukharev, X. Huang, and T. Kim, "Interconnect reliability modeling and analysis for multi-branch interconnect trees," in *Proc. Design Autom. Conf. (DAC)*, San Francisco, CA, USA, pp. 1–6, 2015.

[31] V. Sukharev, X. Huang, and S. X.-D. Tan, "Electromigration induced stress evolution under alternate current and pulse current loads," *J. Appl. Phys.*, vol. 118, no. 3, pp. 034504-1–034504-10, 2015.

[32] K.-D. Lee, "Electromigration recovery and short lead effect under bipolar- and unipolar-pulse current," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Anaheim, CA, USA, Apr. 2012, pp. 6B.3.1–6B.3.4.

[33] S. R. Nassif, "Power grid analysis benchmarks," in *Proc. Asia South Pac. Design Autom. Conf. (ASPDAC)*, Seoul, Korea, 2008, pp. 376–381.

[34] V. Sukharev, "Beyond black's equation: Full-chip EM/SM assessment in 3D IC stack," *Microelectron. Eng.*, vol. 120, pp. 99–105, May 2014.

[35] S.-H. Rhee, Y. Du, and P. S. Ho, "Thermal stress characteristics of Cu/oxide and Cu/low-k submicron interconnect structures," *J. Appl. Phys.*, vol. 93, no. 7, pp. 3926–3933, 2003.

[36] K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *J. Appl. Phys.*, vol. 94, no. 9, pp. 5451–5473, 2003.

[37] *Engineering Toobox*. [Online]. Available: http://www.engineeringtoolbox.com, accessed Sep. 2015.

[38] S. P. Hau-Riege and C. V. Thompson, "The effects of the mechanical properties of the confinement material on electromigration in metallic interconnects," *J. Mater. Res.*, vol. 15, no. 8, pp. 1797–1802, 2000.

**Xin Huang** received the B.S. degree from Sichuan University, Chengdu, China, in 2008, and the M.S. degree from Peking University, Beijing, China, in 2011, both in microelectronics. She is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of California at Riverside, Riverside, CA, USA.

Her current research interests include electromigration modeling and assessment and reliability-aware performance optimization.

**Armen Kteyan** received the Ph.D. degree in solid state physics from the Armenian National Academy of Sciences, Yerevan, Armenia, in 1998.

He is a Lead Engineer with the Design to Silicon Division, Mentor Graphics Corporation, Yerevan, and involved in the development of physics-based models for design for manufacturability applications. His current research interests include theory of dislocations in metals and semiconductors, and theory of superconductivity.

**Sheldon X.-D. Tan** (S'96–M'99–SM'06) received the B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, IA, USA, in 1999.

He is a Professor with the Department of Electrical Engineering, University of California at Riverside, Riverside, CA, USA, where he is also a Cooperative Faculty Member with the Department of Computer Science and Engineering. He is also a Guest Professor with Shanghai Jiao Tong University, Shanghai, and the University of Electronic Science and Technology of China, Chengdu, China. His current research interests include very large scale integration reliability modeling, optimization and management at circuit and system levels, thermal modeling, optimization and dynamic thermal management for many-core processors, statistical modeling, simulation and optimization of mixed-signal/RF/analog circuits, and parallel circuit simulation techniques based on graphics processing unit and multicore systems.

**Valeriy Sukharev** received the Ph.D. degree in physical chemistry from the Russian Academy of Sciences, Moscow, Russia.

He is a Technical Lead with the Design to Silicon Division (Calibre), Mentor Graphics Corporation, Fremont, CA, USA. His current research interests include development of new full-chip modeling and simulation capabilities for the electronic design automation, semiconductor processing and reliability management.

Dr. Sukharev was a recipient of the 2014 Mahboob Khan Outstanding Industry Liaison/Associate Award. He serves on the editorial boards and technical/steering committees of a number of profiling journals and conferences.