Compact Lateral Thermal Resistance Model of TSVs for Fast Finite-Difference Based Thermal Analysis of 3-D Stacked ICs

Zao Liu, Sahana Swarup, Sheldon X.-D. Tan, *Senior Member, IEEE*, Hai-Bao Chen, and Hai Wang

***Abstract*—Thermal issue is the leading design constraint for 3-D stacked integrated circuits (ICs) and through silicon vias (TSVs) are used to effectively reduce the temperature of 3-D ICs. Normally, TSV is considered as a good thermal conductor in its vertical direction, and its vertical thermal resistance has been well modeled. However, lateral heat transfer of TSVs, which is also important, was largely ignored in the past. In this paper, we propose an accurate physics-based model for lateral thermal resistance of TSVs in terms of physical and material parameters, and study the conditions for model accuracy. For TSV arrays or farm, we show that the space or pitch between TSVs has a significant impact on TSV thermal behavior and should be properly considered in the TSV models. The proposed lateral thermal resistance model is fully compatible with the existing modeling approaches, and thus we could build a more accurate complete TSV thermal model. The new TSV thermal model can be easily integrated into a finite difference (FD) based thermal analysis framework to improve analysis efficiency. The accuracy of the model is validated against a commercial finite element tool—COMSOL. Experimental results show that the improved TSV thermal model (with proposed lateral thermal model) could greatly improve the accuracy of FD method in thermal simulation comparing with the existing method.**

***Index Terms*—3-D stacked ICs, finite difference method, lateral resistance model, thermal analysis, TSVs.**

I. Introduction

THERMAL issue becomes a major design constraint for 3-D stacked integrated circuits (ICs). The major factors driving the issue are increased thermal resistance along the primary heat transfer path and high power density. Through silicon vias (TSVs) or thermal TSVs (TTSVs) are vertical vias in 3-D ICs, which can effectively convey heat from multiple layers to the heat sink. TSVs have shown promise in alleviating the thermal problem seen in 3-D stacked ICs [1], [2]. For thermal modeling of 3-D chip structures, it is important to incorporate TSVs into thermal model because TSVs can significantly change the thermal profile of the 3-D chip and TSV models are important for many thermal-aware physical optimizations [3]–[9].

Traditional approaches treat TSVs as a vertical lumped thermal resistor in each physical plane and its resistance value is proportional to the length and inversely proportional to the diameter of the TTSV [10], [11]. The TSV as a 1-D network implies heat flows only in the vertical direction toward the heat sink of the system. This method is shown to be insufficient in capturing the thermal behavior of the TSVs since the lateral heat transfer through these structures is neglected. Recent study shows that the lateral thermal effects due to TSVs or TSV array or farms can have a significant impact on the thermal profile of the 3-D chips [12]. Alternately, accurate numerical approaches such as finite difference (FD) and finite element methods (FEM) can be applied to build the thermal model of the chip package. However, to capture the small feature size of TSVs such as the diameter of TSV and thickness of the insulation layer of TSVs, very fine mesh grids are required, which significantly increase the model complexity and thus the cost of simulation.

For FD based analysis especially in the system and architecture levels, large grid sizes may be used in order to reduce the computation cost of thermal analysis of 3-D stacked chips with TSVs. In this case, we may have more than one TSV in one grid and it becomes important to drive the equivalent lumped models (in both vertical and lateral directions) for such TSV-bearing grids. In addition to fast FD analysis, a very compact, and accurate TSV model which offers insight about the thermal properties of TSV structures and links the heat transfer process with the physical parameters will be very useful for architecture level TSV planning and interlayer level thermal design for 3-D ICs.

Recently, a compact thermal TSV model for 3-D stacked ICs was proposed in [13], in which the lateral thermal resistance is considered. It is an initial effort to address this important thermal modeling problem. This method, however, mainly studied the stacked thermal TSVs across many active layers. It only considered the lateral thermal resistance due to the liner or insulations. Furthermore, their thermal model works only for a single TSV, not for an array of TSVs. Such simple model may lead to large errors for TSV arrays, first, the heat does not necessary pass through TSV when the heat flow goes into a TSV array, because it could bypass each TSV through the

Manuscript received December 27, 2013; revised March 9, 2014 and May 8, 2014; accepted May 26, 2014. Date of current version September 16, 2014. This work was supported in part by the NSF under Grant CCF-1017090 and Grant CCF-1255899 and in part by the Semiconductor Research Corporation under Grant 2013-TJ-2417. This paper was recommended by Associate Editor S. K. Lim.

Z. Liu, S. Swarup, and S. X.-D. Tan are with the Department of Electrical Engineering, University of California, Riverside, CA 92521 USA (e-mail: stan@ee.ucr.edu).

H.-B. Chen is with the School of Microelectronics, Shanghai Jiao Tong University, Shanghai 200240, China.

H. Wang is with the School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu 610054, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCAD.2014.2334321

0278-0070 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

silicon space between them. Second, the isothermal curves in silicon region will be bended when the heat flow passes through TSV array, causing the changes in thermal resistance in the side silicon region. The existing model does not include these effects. To mitigate the model accuracy issues, a larger model (called distributed model) is used in [13]. This in turn will impact the analysis efficiency.

In this paper, we first focus on developing a physics-based analytical expression for the lateral thermal resistance of TSVs and TSV arrays in terms of physical and material parameters. The proposed model targets at estimating the lateral thermal resistance considering TSV arrays, and the model also takes into the account of lateral resistance changes caused by the bending of isothermal curves due to the interplays of TSVs. Our contributions lie in the following aspects.

1) Our lateral thermal resistance model considers both insulation and the filling core of TSV because the thermal resistivity of copper is approximately one third that of silicon and cannot be ignored.
2) We show that the space between TSVs has a significant impact on the lateral thermal resistance as TSVs change the isothermal profiles of each other, and the models for TSV array or farms must be TSV space dependent.
3) We show that the thickness of the insulation layer has limited influence on the accuracy of the proposed model in many practical cases and does not need to be calibrated.
4) The proposed model has been integrated into a FD thermal analysis method to improve the efficiency of FD-based analysis technique.

The proposed analytical lateral thermal resistance model is validated by the commercial FEM tool—COMSOL 4.1 [14], a tool that accurately captures the characteristics of the 3-D stacked chip structures with practical material properties. Experimental results conducted on a single TSV and array of TSVs demonstrate the accuracy of the proposed method by comparing with the results from COMSOL. Second, with the proposed lateral thermal resistance model, we have improved the complete thermal model for TSV and TSV arrays. We integrate the resulting model into a FD thermal analysis program, and demonstrate that its modeling accuracy by comparing the simulated results against the results from COMSOL. The proposed method also compares favorably with recently proposed TSV model [13] in terms of accuracy.

The article is organized as follows: Section II discusses the problem formulation for lateral thermal modeling. Section III describes the mathematical formulation of the closed form expression of the lateral thermal resistance of the TSVs, and Section IV outlines the method to integrate the proposed model into 3-D finite difference thermal code. The experimental results are discussed in Section V. Section VI concludes this paper.

II. Problem Formulation

A. Finite Difference Method for 3-D Thermal Modeling

The parabolic partial differential equation is used to model the time-dependent thermal effect on 3-D ICs [15], [16]

$$\rho C_p \frac{\partial T(\vec{r},t)}{\partial t} = \kappa(\vec{r},T)\cdot\nabla^2 T(\vec{r},t) + g(\vec{r},t) \quad (1)$$

which subjects to Robin's boundary condition

$$\kappa(\vec{r},T)\frac{\partial T(\vec{r},t)}{\partial n} = h(T(\vec{r},t) - T_{amb}). \quad (2)$$

In (1), T (K) is the temperature, ρ (kg/m^3) is the density of the material, C_p (Jkg^{-1}K^{-1}) is the mass heat capacity of the material, κ (Wm^{-1}K^{-1}) is the effective thermal conductivity, which depends on the material and structure of the heat conduction media, and g (W/m^3) is the heat energy generation rate inside the material. In the boundary condition (2), n is a unit vector that is normal to the boundary surface, h (Wm^{-2}K^{-1}) is the heat-transfer coefficient for the convective surface, and T_{amb} is the ambient temperature surrounding the thermal systems.

In order to compute the item $\kappa(\vec{r},T)\cdot\nabla^2 T(\vec{r},t)$ in (1), we denote κ_x, κ_y, and κ_z as the effective thermal conductivities along the x, y, and z axes, respectively. Let κ_{x+}, κ_{x-}, κ_{y+}, κ_{y-}, κ_{z+}, and κ_{z-} represent the effective thermal conductivities in the $x+$, $x-$, $y+$, $y-$, $z+$, and $z-$ directions to model the inhomogeneous of the heat conduction media, respectively, i.e., we have the following relations:

$$\kappa_x = \begin{cases} \kappa_{x+}, & x \to x+ \\ \kappa_{x-}, & x \to x- \end{cases}$$
$$\kappa_y = \begin{cases} \kappa_{y+}, & y \to y+ \\ \kappa_{y-}, & y \to y- \end{cases}$$
$$\kappa_z = \begin{cases} \kappa_{z+}, & z \to z+ \\ \kappa_{z-}, & z \to z-. \end{cases}$$

By using the FD method, one can calculate the derivatives at discretized mesh grid (i,j,k), given by

$$\begin{aligned}
\kappa_x\frac{\partial^2 T}{\partial x^2} &= \kappa_x\frac{T_{i+1,j,k} - 2T_{i,j,k} + T_{i-1,j,k}}{\Delta x^2} \\
&= \frac{\kappa_{x+}}{\Delta x^2}(T_{i+1,j,k} - T_{i,j,k}) + \frac{\kappa_{x-}}{\Delta x^2}(T_{i-1,j,k} - T_{i,j,k}) \\
\kappa_y\frac{\partial^2 T}{\partial y^2} &= \kappa_y\frac{T_{i,j+1,k} - 2T_{i,j,k} + T_{i,j-1,k}}{\Delta y^2} \\
&= \frac{\kappa_{y+}}{\Delta y^2}(T_{i,j+1,k} - T_{i,j,k}) + \frac{\kappa_{y-}}{\Delta y^2}(T_{i,j-1,k} - T_{i,j,k}) \\
\kappa_z\frac{\partial^2 T}{\partial z^2} &= \kappa_z\frac{T_{i,j,k+1} - 2T_{i,j,k} + T_{i,j,k-1}}{\Delta z^2} \\
&= \frac{\kappa_{z+}}{\Delta z^2}(T_{i,j,k+1} - T_{i,j,k}) + \frac{\kappa_{z-}}{\Delta z^2}(T_{i,j,k-1} - T_{i,j,k})
\end{aligned}$$

where $T_{i,j,k}$ represents the temperature value at node (i,j,k), Δx, Δy, and Δz are the discretization steps along the x, y, z directions, respectively. Thus, the discretized form of (1) is

$$\begin{aligned}
\rho C_p\frac{dT}{dt} = &-\left(\frac{\kappa_{x+}}{\Delta x^2} + \frac{\kappa_{x-}}{\Delta x^2} + \frac{\kappa_{y+}}{\Delta y^2} + \frac{\kappa_{y-}}{\Delta y^2} + \frac{\kappa_{z+}}{\Delta z^2} + \frac{\kappa_{z-}}{\Delta z^2}\right)T_{i,j,k} \\
&+ \frac{\kappa_{x+}}{\Delta x^2}T_{i+1,j,k} + \frac{\kappa_{x-}}{\Delta x^2}T_{i-1,j,k} + \frac{\kappa_{y+}}{\Delta y^2}T_{i,j+1,k} \\
&+ \frac{\kappa_{y-}}{\Delta y^2}T_{i,j-1,k} + \frac{\kappa_{z+}}{\Delta z^2}T_{i,j,k+1} \\
&+ \frac{\kappa_{z-}}{\Delta z^2}T_{i,j,k-1} + g_{i,j,k,t}
\end{aligned}$$

where $g_{i,j,k,t}$ is the heat generation at node (i,j,k). Furthermore, the above discretized heat equation for the mesh

grid (i, j, k) can be rewritten as follows:

$$\begin{aligned}\rho C_p \Delta V \frac{dT}{dt} = &-(G_{x+} + G_{x-} + G_{y+} + G_{y-} + G_{z+} \\ &+ G_{z-})T_{i,j,k} + G_{x+}T_{i+1,j,k} + G_{x-}T_{i-1,j,k} \\ &+ G_{y+}T_{i,j+1,k} + G_{y-}T_{i,j-1,k} + G_{z+}T_{i,j,k+1} \\ &+ G_{z-}T_{i,j,k-1} + \Delta V g_{i,j,k,t}\end{aligned} \quad (3)$$

where $\Delta V = \Delta x \Delta y \Delta z$, $G_{x+} = \frac{\kappa_{x+}\Delta y \Delta z}{\Delta x}$, $G_{x-} = \frac{\kappa_{x-}\Delta y \Delta z}{\Delta x}$, $G_{y+} = \frac{\kappa_{y+}\Delta x \Delta z}{\Delta y}$, $G_{y-} = \frac{\kappa_{y-}\Delta x \Delta z}{\Delta y}$, $G_{z+} = \frac{\kappa_{z+}\Delta x \Delta y}{\Delta z}$, and $G_{z-} = \frac{\kappa_{z-}\Delta x \Delta y}{\Delta z}$ give the physics definitions of the thermal conductance along $x-$, $x+$, $y-$, $y+$, $z-$, and $z+$ directions. Since the method of calculating thermal conductance in $z-$ and $z+$ directions have been studied [11], in this paper, we will be focusing on the way to calculate the lateral thermal conductance in $x-$, $x+$, $y-$, and $y+$ direction, and apply it to FD thermal analysis through (3).

B. Thermal Resistance Modeling of TSVs

FD analysis method uses mesh grids to discretize the partial differential equations from the heat diffusion dynamics [15]. For thermal modeling of 3-D chip structure, it is important to incorporate TSVs into the thermal model as they significantly change the thermal profile of the 3-D chip [10], [12], [17]. However, to capture the small feature size of the TSV, like diameter of TSV and thickness of the insulation layer (liner) of TSV, very fine mesh grids are required. This significantly increases the model complexity and the cost of simulation. For example, the radius of a TSV typically ranges from 10 μm to 100 μm while the thickness of the liner ranges from 2% to 10% of the radius of the TSV [13], [18]. As a result, to make the thermal grids (cells) as small as a few μm can lead to very huge thermal equations or matrices, which typically is not necessary.

One strategy to overcome this problem is to use large mesh grids and use compact, accurate macromodel for each grid, which may contain one or more TSVs. One such example is shown in Fig. 1 in which a TSV is placed in one cell. In this cell, the vertical resistance for the TSV can be computed by

$$R_V = \frac{L}{kA} \quad (4)$$

where L is the TSV length in the vertical direction, $A = \pi r^2$ is the cross sectional area of the TSV cylinder in the vertical direction and k is the thermal conductivity of the effective TSV material, which consists of copper, liner materials, silicon [11]. But the lateral thermal resistance is more complicated. In this paper, we focus on developing the analytical expression for the thermal resistance in the lateral direction in terms of physical and material parameters. For a TSV array or farms, the vertical resistance can be computed as $R_{array,V} = L/k_{eff}A$, where k_{eff} is the effective thermal conductivity, which depends on the ratio of the TSV areas versus the total areas considered [11].

The structure view of a TSV cell is shown in Fig. 1. It consists of a TSV in the center of the cell surrounded by silicon region on either side. We assume the TSV is made of copper and is surrounded by a layer of silicon dioxide which acts as the insulation material. In the vertical direction, the copper core serves as a good thermal conductor for heat transfer from the inside. However, in the lateral direction, the insulation layer, although very thin, can have a large influence on the thermal resistance.

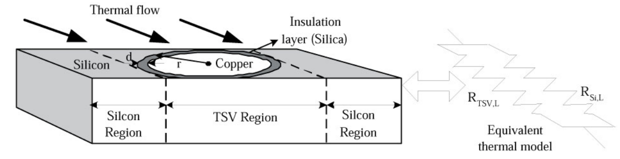


Fig. 1. Structure view of TSV cell with copper core and insulation layer.

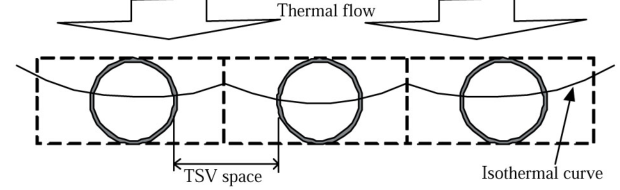


Fig. 2. Top view of TSV array built using individual TSV cells.

Let $R_{TSV,L}$ and $R_{Si,L}$ represent the lateral thermal resistances of the TSV region and the silicon region, respectively. The lateral thermal resistance of the TSV cell can be expressed as a parallel combination of the two resistances as shown in Fig. 1. The TSV cell shown in Fig. 1 can be used to build any TSV array as shown in Fig. 2. The space between two TSVs (TSV space) in the array is the total width of the silicon region of each TSV cell. The lateral thermal resistance model of one TSV cell can thus be extended to compute the lateral thermal resistance of a TSV array of any scale. The following section discusses the proposed closed form expression for the lateral thermal resistance of the TSV.

III. Analytical Expression for Lateral Thermal Resistance of TSVs

A. Mathematical Derivation of the Closed Form Expression

The heat transfer follows the fundamental heat diffusion (1). For many heat transfer problems with unknown boundary conditions, closed form expression cannot be found [19].

To determine the closed form expression for the lateral thermal resistance of the TSV region, we start with the following three major assumptions.

1) Inside the insulation layer, majority of the isothermal curve is parallel to the insulation layer, which means that the lateral thermal flow is always vertical to the insulation layer as shown in Fig. 3.
2) The lateral thermal resistance of the silicon region contributed by the four corners of the TSV region is small compared to the TSV and is not considered while formulating the closed form expression.
3) Inside the copper core, the heat flow is straight as shown in Fig. 3, and the detour of the heat flow close to the insulation layer is negligible.

With these assumptions, we can calculate the resistance across a small portion of the insulation layer of the TSV

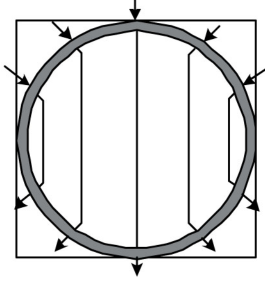


Fig. 3. Direction of lateral thermal flow (arrows) across the TSV region.

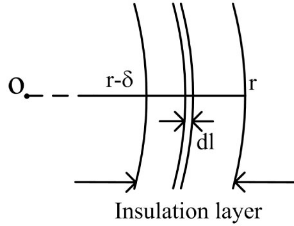


Fig. 4. Thermal resistance calculation across the insulation layer.

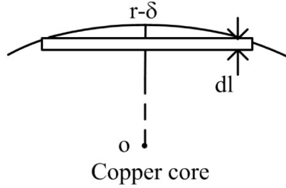


Fig. 5. Thermal resistance calculation across the TSV core.

as shown in Fig. 4. Considering the symmetry of the entire structure, the thermal resistance going through the insulation layer is [19]

$$R_{ins,L} = 2\int_{r-\delta}^{r} \frac{\rho_{ins} dl}{\pi l h} \tag{5}$$

where r is the radius of cross section of the TSV, δ is the thickness of the insulation layer, h is the height of the cell, l is the position variable across the insulation layer, ρ_{ins} is the thermal resistivity of the insulation material and $R_{ins,L}$ is the calculated lateral thermal resistance of the insulation layer.

Using $\alpha = \delta/r$ as the ratio of the insulation layer thickness to the TSV radius, (5) reduces to a closed form expression

$$R_{ins,L} = -\frac{2\rho_{ins} ln(1-\alpha)}{\pi h}. \tag{6}$$

Assuming the heat flow is straight as shown in Fig. 3 and considering the symmetry of the structure, the lateral thermal resistance across a small portion of the copper core as shown in Fig. 5 is given by

$$R_{cu,L} = \int_{0}^{r-\delta} \frac{\rho_{cu} dl}{h\sqrt{(r-\delta)^2 - l^2}} \tag{7}$$

where ρ_{cu} is the thermal resistivity of the copper core of the TSV, and $r-\delta$ is the radius of the copper core. Considering the symmetry of the entire structure, the lateral thermal resistance of the copper core is

$$R_{cu,L} = \frac{\rho_{cu}\pi}{2h}. \tag{8}$$

Therefore, from assumptions 1-3, the lateral thermal resistance in the TSV region in a TSV cell can be written as

$$R_{TSV,L} = -\frac{2\rho_{ins} ln(1-\alpha)}{\pi h} + \frac{\rho_{cu}\pi}{2h}. \tag{9}$$

Equation (9) shows that the value of lateral thermal resistance in the TSV region is proportional to $ln(1-\alpha)$ and $1/h$. This implies that the lateral thermal resistance is directly proportional to α and inversely proportional to the thickness.

The lateral thermal resistance of the entire TSV cell is the parallel combination of the lateral thermal resistance of $R_{TSV,L}$ and $R_{Si,L}$. This equivalent circuit model is shown in Fig. 1. As a result, for $R_{Si,L}$, we have

$$R_{Si,L} = \frac{2\rho_{si} r}{dh} \tag{10}$$

where d is the total width of two identical side silicon regions (with the width of each side equals to $d/2$). We further define $d = rP$, where P is the ratio of the TSV space to TSV radius r, neglecting the bending of isothermal lines close to TSVs, the lateral thermal resistance of the side silicon region can also be expressed as

$$R_{Si,L} = \frac{2\rho_{si}}{Ph}. \tag{11}$$

Therefore, the total lateral thermal resistance of the TSV cell is

$$R_{TSVcell,L} = R_{TSV,L} // R_{Si,L}. \tag{12}$$

Here, we assume that we have two identical side silicon regions with the same width and the TSV is in the middle.

B. Model Accuracy Analysis and Calibration

The derived analytical expression given in (12) is based on some assumptions and therefore will have some inaccuracies in some practical cases.

1) The lateral thermal resistance in (12) is based on the assumption that the isothermal curve is not bent in the silicon region in the TSV cell. However, due to the presence of TSVs, the isothermal curve has to be bent as shown in Fig. 2. Depending on the ratio of TSV space to TSV radius (P), the isothermal curve could be bent differently. Thus, the value of $R_{Si,L}$ depends on the ratio of TSV space to TSV radius. This has not been captured by the closed form model.
2) The thickness of the insulation layer can influence model accuracy. If the insulation layer is too thick, the isothermal profile in the insulation layer may change, and majority of the heat flow will no longer be vertical to the insulation surface. Thus, the thermal flow in the tangential direction inside the insulation layer will not be negligible. On the other hand, if the insulation layer is too thin, the model accuracy may go down. As the insulation layer gets thinner (for instance, as α tends to 0), the lateral thermal resistance from the silicon part in

the TSV region becomes significant and will need to be accounted for.

We first consider the impacts due to the spaces between two TSVs. This space is normally 2 to 6 times the radius of the TSV (the ratio of TSV space to TSV radius $P \in [2, 6]$) [1], [18], [20]. The isothermal curve is strongly influenced by this variation. Thus, to capture the influence of the space between the TSV arrays, model calibration based on numerical data is required to enhance the model accuracy. The modified lateral thermal resistance can be written as

$$R_{TSVcell,cal,L} = R_{TSVcell,L}\theta \tag{13}$$

where θ, the modification factor, can be written as a linear function of the ratio of TSV space to TSV radius (P)

$$\theta = \beta_1 P + \beta_2. \tag{14}$$

Currently, detailed numerical analysis using COMSOL or measurements on some specially design chips will still be required to obtain the two fitting parameters β_1 and β_2 in the calibration formula.

But our experiments show that the calibration formula does not need to be recalibrated again if the TSV structure is similar and the liner thickness is within a range as already shown by Fig. 9. Only if material changes, the model need to be recalibrated. But more research to find the closed form expressions for β_1 and β_2 in terms of TSV structure and material parameters will be still interesting and this can be future investigation.

We remark that in our proposed model in (12), the lateral thermal resistance $R_{TSVcell,L} = R_{TSV,L}//R_{Si,L}$ has two components, the resistance from TSV itself $R_{TSV,L}$ and the resistance from the two side silicon regions $R_{Si,L}$. The space between TSV here is also the half width of the two side silicon regions orthogonal to the heat flow direction as shown in Fig. 1. As a result, the larger the distance, or the larger P is, the smaller the resistance of the side silicon will be as shown in (11). The total lateral resistance $R_{TSVcell,L}$ hence will go down with the increasing distance as shown Fig. 9.

But according to (13), the change of $R_{TSVcell,cal,L}$ will grow as P increases. However, this is not the case practically. If we have TSVs which are far away, then the resistance of the side silicon will dominate the total lateral resistance as we can see. The resistive contribution of the TSV itself becomes less significant and less relevant. From practical point of view, this will not happen. First, such TSV with very long side silicon region will not exist in the FD analysis as such TSV will be decomposed into several smaller grids or cells. The grid with TSVs will have small TSV distance, thus small P. As a result, a TSV, which is far away from other TSVs, essentially corresponds to condition for a small or zero-valued width d of the side silicon region and $P = 0$. The meaningful values for P and thus width of the side silicon region d are typically small for the practical FD analysis framework.

Although the thickness of the insulation layer affects the model accuracy, its influence is limited to 2% to 10% of the TSV radius, the range of practical thickness of the insulation layer [13], [18]. Thus, (9) is valid since our assumptions for deriving it are not violated for the practical thickness of the insulation layer within this range. Experimental results will show that the calculated thermal resistance error of the TSV cell due to the variation of the insulation layer thickness in this range is acceptable and does not need further calibration.

TSV arrays of any dimension could be constructed by extending the fundamental TSV cells periodically in lateral directions. Hence, having established the lateral thermal model of each fundamental TSV cell, and assuming a TSV array has M TSVs in L direction and N TSVs in the direction that is perpendicular to it, the lateral thermal resistance in L direction could be calculated by using parallel and serial connection theory as

$$R_{TSVarray,L} = R_{TSVcell,cal,L}\frac{M}{N}. \tag{15}$$

Thus, once the lateral resistance of each TSV is calculated, estimating the lateral resistance of any TSV array is straightforward.

We expect that the proposed closed form model is a compact and robust one, the calibrated parameter β_1 and β_2 in (14) applies to TSV of any arbitrary radius in the silicon layer with different thickness. We will testify this in our experiments.

IV. Compact Thermal Model With Closed Form Lateral Thermal Resistance

By now, we have presented our proposed method of using closed form expression to calculate the thermal resistance of TSV and TSV arrays in lateral direction, which could be used to calculate the total lateral thermal resistance of a silicon structure with TSV array in it as

$$R_{tot,L} = R_{TSVarray,L} + R_{Si,L\sigma} \tag{16}$$

in which $R_{TSVarray,L}$ is the lateral thermal resistance contributed by the TSV array, and $R_{Si,L\sigma}$ is the serial lateral thermal resistance of the bulk silicon area with no TSVs and could be easily calculated by using

$$R_{Si,L\sigma} = \rho_{Si}\frac{L_\sigma}{A_\sigma} \tag{17}$$

in which L_σ is the length of the silicon in the direction of the heat flow, and A_σ is the cross area perpendicular to the direction of the heat flow. In vertical direction, the calculation of thermal resistance including the TSV and TSV arrays is more straightforward, which has already been discussed in many previous works like [11] and [13]. Using these approaches, the thermal resistance in vertical direction that considers the copper core and insulation liner in TSV array could be expressed as

$$R_V = R_{cu,V}//R_{ins,V}//R_{Si,V} \tag{18}$$

in which $R_{cu,V}$ represents the thermal resistance of the copper core of the TSV array, $R_{ins,V}$ represents the vertical thermal resistance of the insulation liner of the TSV array, and $R_{Si,V}$ represents the portion of the vertical thermal resistance from the remaining silicon bulk. Using the material and geometry parameters defined in Section III, assuming the TSV array is $M \times N$ (M TSVs in x direction and N TSVs in y direction) and the chip area that contains the TSV array is S, the vertical

thermal resistance due to copper core $R_{cu,V}$ of the TSV array can be calculated as

$$R_{cu,V} = \rho_{cu}\frac{h}{\pi r^2(1-\alpha)^2 MN} \quad (19)$$

and the $R_{ins,V}$ is

$$R_{ins,V} = \rho_{ins}\frac{h}{\pi r^2(1-(1-\alpha)^2)MN} \quad (20)$$

and the vertical thermal resistance due to the remaining bulk silicon $R_{Si,V}$ is

$$R_{Si,V} = \rho_{Si}\frac{h}{S-\pi r^2 MN}. \quad (21)$$

Similarly, using the definition of thermal capacitance in [16], the thermal capacitance of the chip area that contains the TSV array could be expressed as an added summation of thermal capacitance of different materials as

$$\begin{aligned} C_p &= c_{p,cu}h(\pi r^2(1-\alpha)^2 MN) \\ &\quad + c_{p,ins}h(\pi r^2(1-(1-\alpha)^2)MN \\ &\quad + c_{p,Si}h(S-\pi r^2 MN) \end{aligned} \quad (22)$$

in which $c_{p,cu}$ is the specific heat of the copper core in the TSV array, and $c_{p,ins}$ is the specific heat of the insulation liner, and $c_{p,Si}$ is the specific heat of the bulk silicon.

Hence, in the Cartesian coordinate, using R_{x+}, R_{x-}, R_{y+}, R_{y-} to denote the thermal resistance in lateral direction, and R_{z+}, R_{z-} to denote the thermal resistance in vertical direction, the complete compact model of a silicon structure that contains the TSV array, like the structure in Fig. 6(a), can be represented by complete thermal model shown in Fig. 6(b). In this model, the lateral thermal resistance considering TSV arrays is modeled using (15) and (16). For example, in $x+$ direction, the lateral thermal resistance R_x+ could be conveniently calculated as

$$R_{x+} = R_{TSVarray,x+} + R_{Si,x+} \quad (23)$$

in which $R_{TSVarray,x+}$ represents the lateral thermal resistance across the TSV array in $x+$ direction and could be calculated using (15); $R_{Si,x+}$ represents the total lateral thermal resistance of the remaining silicon bulk region that is equivalent to serial connection with the TSV array in $x+$ direction. Therefore, in (3), we have $G_{x+} = 1/R_{x+}$ in $x+$ direction, and $G_{x-} = 1/R_{x-}$, $G_{y+} = 1/R_{y+}$, $G_{y-} = 1/R_{y-}$, $G_{z+} = 1/R_{z+}$, $G_{z-} = 1/R_{z-}$ in all other directions, and the lateral thermal resistance in these direction could be obtained in similar way as that of R_{x+}.

We remark that we distinguish the lateral resistance in two x and two y directions (for instance $x+$ and $x-$ directions for x). Such anisotropic effect in the x and y directions actually comes from the observation that thermal behavior of TSV will affect each other when they are placed in an array or a farm form as we showed in the article. For instance, for a FD grid n, in its $x+$ direction, it has TSV arrays adjacent to it, but in its $x-$ direction, it has no TSV arrays adjacent to it. In this case, the lateral thermal resistance would be different in $x+$ direction and $x-$ direction.

Since the closed form expression of the lateral thermal resistance of the TSV array is used in the thermal modeling, the accuracy improvement in lateral direction is achieved without increasing computation cost. The final lumped thermal model is now shown in Fig. 6(b), which can be easily used by the FD method as one FD grid that contains one TSV or more TSVs. Such compact models will allow more efficient FD analysis without significant loss of temperature accuracy at both vertical and lateral directions for 3-D ICs.

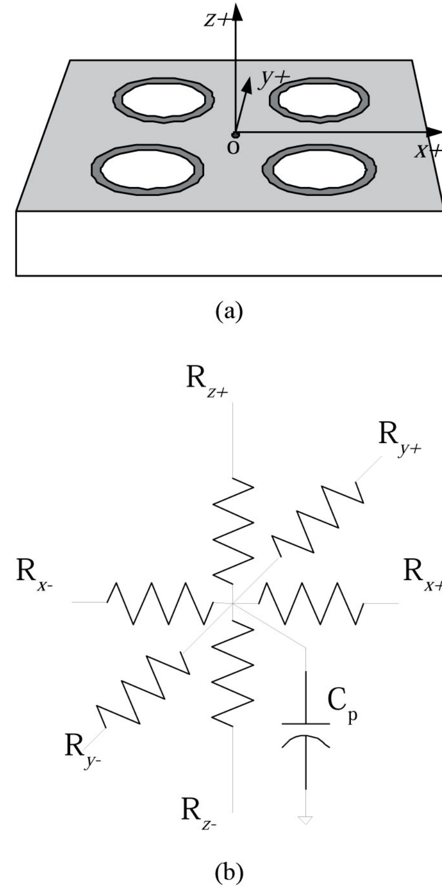


Fig. 6. Silicon structure containing TSV array and its compact thermal model considering thermal resistance of TSVs in 3-D Cartesian coordinate. (a) Silicon structure containing TSV array (A 2-by-2 TSV array). (b) Complete compact thermal model of the silicon structure with TSVs.

For practical TSV with bonding technology, a thermal TSV, fabricated by 3-D technology may span through several layers. For instance, a typical three-layer TSV structure and the corresponding thermal model (just the x and z directions and thermal capacitance is not shown here) is shown in Fig. 7. This TSV spans through three layers describing the silicon substrate (Si), the inter layer dielectric (ILD) and metal interconnects (i.e., the back end of line or BEOL), and the bonding layer, respectively [13]. Our proposed lateral thermal model is fully compatible with the existing layer by layer thermal modeling approach by just replacing the lateral thermal resistance computed in the silicon layer using the proposed method. For layers like ILD and bonding layer that primarily use insulation materials, traditional thermal modeling techniques that do not consider lateral thermal resistance could still be applied, since the lateral thermal resistance in these layers is orders of magnitude higher than that in the vertical direction of TSVs.

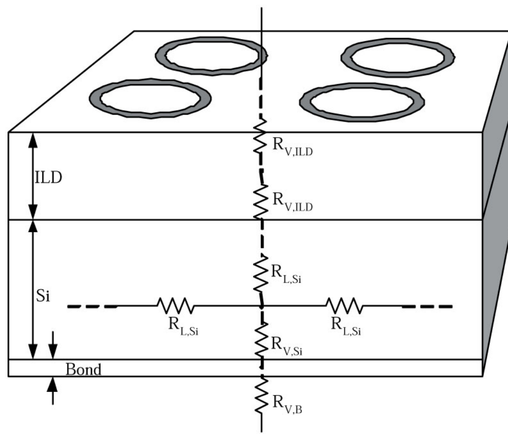


Fig. 7. Extending the proposed lateral model into more complicated TSV structures.

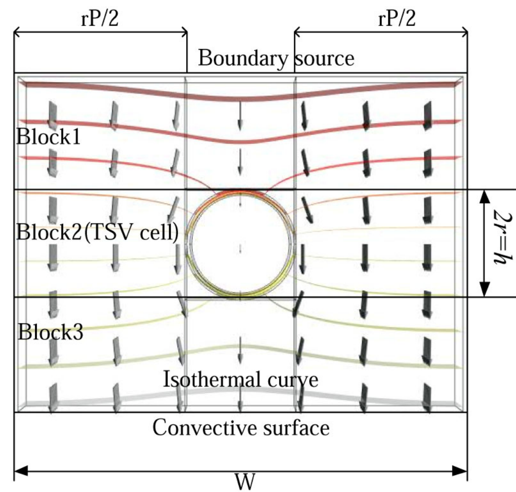


Fig. 8. Isothermal curve of the TSV cell under test.

We also remark that the TSVs shown in Fig. 7 are actually close to via-last TSVs. This paper focuses on modeling the behavior of general TSVs and it can be applied to TSVs built before transistors (via-first) or after the transistors (via-last). Also, inside silicon layer, both via-first and via-last TSVs have the same structure—copper core and insulation liner. Our work focuses on how to develop a compact lateral thermal resistance model for such a structure. We target at general TSVs, no matter they are via-first or via-last. The two types of TSVs may have differences in vertical ILD layers. As discussed already, we do not need to apply lateral thermal resistance model in ILD layer. Instead, the traditional vertical-only TSV thermal models should work in this case for the TSV portion in the ILD layers.

V. Numerical Results and Discussion

Experiments are performed using COMSOL 4.1 software on a Linux server with 1.6GHz quad-core CPU and 16GB memory and the results are compared against our proposed model.

A. Experimental Results of TSV Cell

1) Experimental Setup: To measure the lateral thermal resistance using COMSOL, we define a structure as shown in Fig. 8. A power source of $10^{-4}W$ is on the front face (top) of the structure and the convection surface with heat exchanging rate of $1000W/(m^2K)$ is on the back face (bottom). The back face is the only face that exchanges heat with the surroundings. All the other faces (left and right faces) have no heat exchange with the environment, and thus the lateral thermal resistance $R_{Therm,L}$ of the entire structure in the direction of thermal flow can be measured by

$$R_{Therm,L} = \frac{\Delta T}{q} \tag{24}$$

where ΔT is the temperature difference across the structure (from the front face to the back face), and q is the corresponding power flow.

The structure can be divided into three blocks where block1 and block3 are the silicon blocks, and block2 is the TSV cell block sandwiched between block1 and block3 as shown in Fig. 8. The figure also shows the isothermal curves from COMSOL simulation where the direction of thermal flow is represented by short arrows perpendicular to the isothermal curves. It can be seen that the isothermal curves are bent close to the location of TSV and the majority of the isothermal curves are at the location of the TSV overlapping with the insulation layer. This shows that most of the heat flow is perpendicular to the insulation layer which is in line with the assumptions made in the Section III. In our experiments, the radius of the TSV (from the center to the outer interface between silicon and insulator) is fixed at $r = 25$ μm and the height of the structure is fixed at $h = 50$ μm. The thickness of the insulation layer varies from 0.5 to 2.5 μm. The width of the silicon region, denoted by rP (r is the TSV radius, P is the ratio of TSV space to TSV radius) in Fig. 8, varies from 2 to 6 times the TSV radius. Physically, the value of P represents the space between the TSVs in a TSV array built with this TSV cell. We study how the variation of P influences the accuracy of the proposed model for a TSV cell.

The lateral thermal resistance of the TSV cell can be measured as

$$R_{TSVcell,M,L} = \frac{\Delta T}{q} - R_{SerSi} \tag{25}$$

where $R_{TSVcell,M,L}$ is the measured lateral thermal resistance of the TSV cell, and R_{SerSi} is the lateral thermal resistance of the silicon region in the thermal flow direction. This thermal resistance is in serial with the thermal resistance of the TSV cell. Here, $R_{SerSi} = 2\rho_{Si}/W$ represents the serial connection of the two silicon blocks where the thermal resistance of each one is denoted as ρ_{Si}/W. W is the width of the blocks in the thermal flow direction and this is shown in Fig. 8. In the following subsection, the calculated lateral thermal resistance is compared against the measured data based on FEM results to validate the proposed closed form thermal resistance model.

2) Result Analysis and Discussion: We first simulate the steady state temperature response of the structure using COMSOL. The lateral thermal resistance can be measured using (25). The modeled lateral thermal resistance before calibration can be calculated directly based on the material and

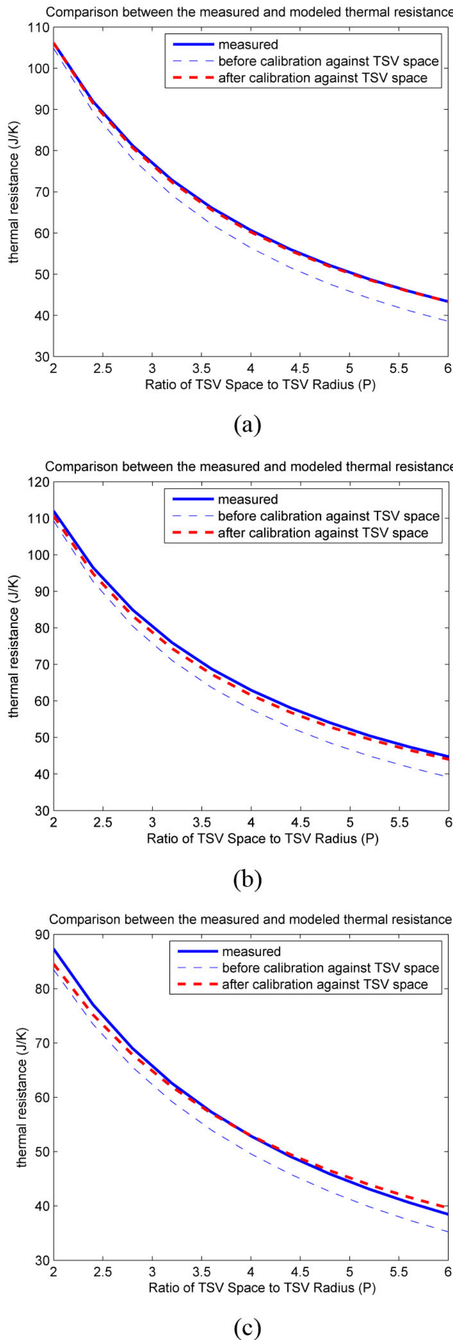


Fig. 9. Comparison of the proposed thermal model and the measured data for different TSV distances and different thicknesses of insulation layers. (a) Thickness of the insulation layer is 1.5 μm. (b) Thickness of the insulation layer is 2.5 μm. (c) Thickness of the insulation layer is 0.5 μm.

geometry of the structure using (12). To determine the coefficient of the calibration factor (β_1 and β_2), we need to use the measured thermal resistance data of at least two TSV cells with different P. The values of P we choose for model calibration are $P_1 = 2$ and $P_2 = 6$. To reduce the calibration error under different values of insulation layer thickness ranging from 0.5 to 2.5 μm, we choose the measured data of the structure with insulation layer thickness as 1.5 μm, which is in the middle of the range: 0.5 to 2.5 μm. Thus, the calculated coefficients of the linear function θ is computed as: $\beta_1 = 0.0279$, $\beta_2 = 0.956$.

In both Fig. 9(a) and (b), the solid line shows measured lateral thermal resistance, the finer dash line shows the calculated result from the model before calibration, and the bond dash line shows the calculated result from the calibrated model. Our observations are as follows.

1) The model before calibration deviates from the measured data because of the modified isothermal lines introduced by the presence of TSVs.
2) Model calibration significantly increases the accuracy of the modeled thermal resistance in the targeted range of TSV space.
3) Both the thickness of the insulation liner and the space between TSVs influence the lateral thermal resistance. Thicker insulation liner leads to higher lateral thermal resistance in general, and larger space between TSVs causes lower lateral thermal resistance.

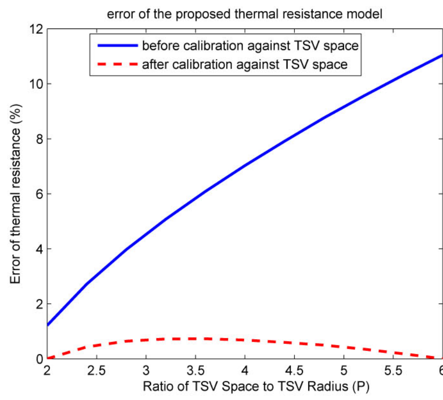
The relative model error with different TSV space is shown in Fig. 10. It indicates that without calibration, the error keeps increasing as the space between the TSVs increases. After applying the calibration, the model error reduces significantly and the smallest error is found for the structure that has insulation layer thickness of 1.5 μm. This is because the calibration is directly applied to the measured data of this type of structure. For structures with different insulation layer thickness on TSVs, the error increases and the maximum error is found to be 2% to 3%, which is an acceptable error margin. This result confirms that variation in the insulation layer thickness of TSVs (of 2% to 10% of TSV radius) does not bring in significant error to the model. Thus, it is not necessary to calibrate the model for various value of this parameter in most practical cases. Hence, once the lateral thermal resistance model of a TSV cell is calibrated with different P, it can be reused to build the model for any TSV array.

In addition, we remark that the existing lumped modeling approach presented in [13] does not consider the space between two TSVs and thus the model accuracy compromises under the cases when the space between two TSV changes. Fig. 11 shows a comparison of the proposed modeling method with the existing lumped modeling method, which clear illustrates this problem.

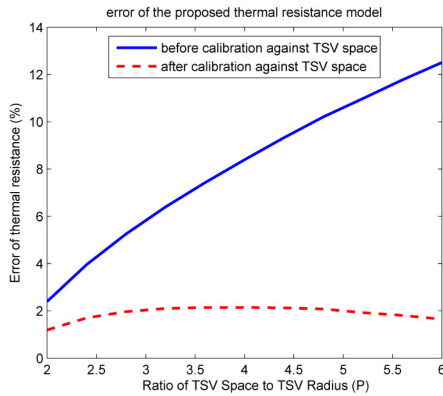
B. Experimental Results for TSV Arrays

1) Experimental Setup: Having validated the lateral thermal resistance model for a TSV cell in the previous section, we now compute the lateral thermal resistance in the thermal flow direction of a TSV array. For this purpose, we consider two examples: a 1-D TSV array and a 2-D TSV array as shown in Fig. 12 and compare the measured lateral thermal resistance against the modeled value for both the arrays. The heat source and the convection boundary is set up in the same way as before: $10^{-4}W$ at the front face and $1000W/(m^2K)$ at the back face. COMSOL 4.1 is used to simulate the temperature profile of the TSV array and the measured lateral thermal resistance across the TSV array is compared against the lateral thermal resistance modeled by (15).

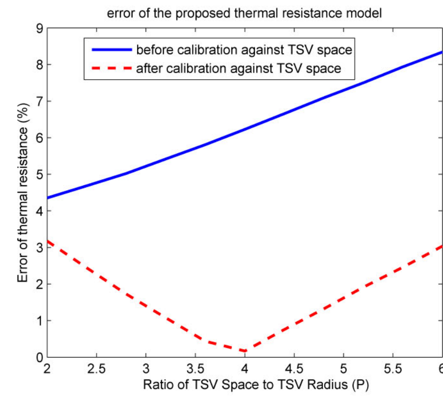
2) Result Analysis and Discussion: The results for the TSV array are obtained for a TSV radius of $r = 25$ μm, insulation layer thickness of $\delta = 2.5$ μm (10% of the TSV radius) and a



(a)



(b)



(c)

Fig. 10. Error of the proposed model (before calibration and after calibration). (a) Thickness of the insulation layer is 1.5 μm. (b) Thickness of the insulation layer is 2.5 μm. (c) Thickness of the insulation layer is 0.5 μm.

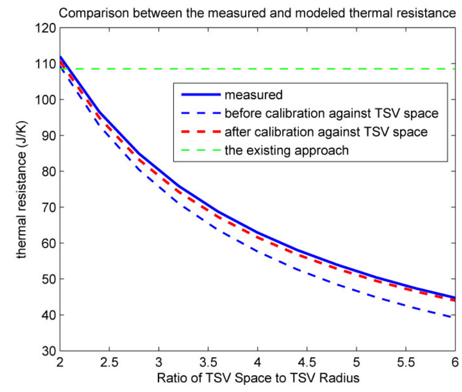


Fig. 11. Comparison of the proposed modeling method with the existing lumped modeling method.

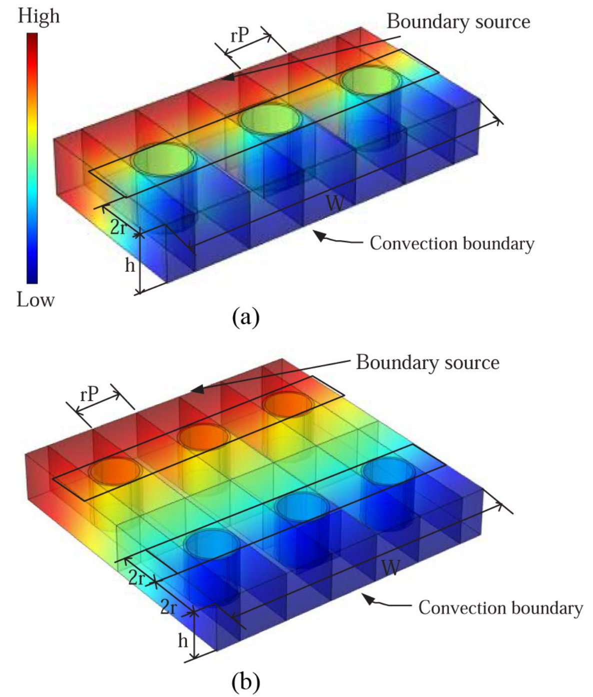


Fig. 12. TSV array structures used for lateral thermal resistance validation. (a) 1-D TSV array. (b) 2-D TSV array.

TABLE I
COMPARISON OF MODELED AND MEASURED LATERAL THERMAL RESISTANCE OF 1-D TSV ARRAY

P	Measured(K/J)	Modeled(K/J)	Error
2	37.30	36.87	1.15%
4	20.96	20.66	1.43%
6	14.91	14.66	1.68%

block height of $h = 50$ μm. The results for the 1-D and 2-D arrays are summarized in Tables I and II, respectively. The lateral thermal resistance is measured under different scenarios by varying the space between TSVs from 50 to 150 μm. This corresponds to the ratio of TSV space to radius (denoted as P) of 2 to 6.

For the 1-D TSV array shown in Fig. 12(a), Table I shows the measured lateral thermal resistance. The lateral thermal resistance is modeled using (12), (13), and (15). Since the TSV array is a parallel combination of three TSV cells, the modeled lateral thermal resistance for this array can be calculated as: $R_{TSVcell,cal,L}/3$ where $R_{TSVcell,cal,L}$ is calculated using (13). The results in Table I show that the modeled thermal resistance closely matches the measured data for the 1-D TSV array.

Table II shows the measured total lateral thermal resistance of the 2-D array as indicated by the enclosed region in Fig. 12(b). The lateral thermal resistance is modeled using (12), (13), and (15). The space between the two 1-D TSV arrays in Fig. 12 lines up with the direction of the thermal flow

TABLE II
COMPARISON OF MODELED AND MEASURED LATERAL THERMAL RESISTANCE OF THE 2-D TSV ARRAY

P	Measured(K/J)	Modeled(K/J)	Error
2	74.62	73.74	1.18%
4	41.35	41.32	0.07%
6	28.81	29.32	1.68%

TABLE III
COMPARISON OF MODELED AND MEASURED LATERAL THERMAL RESISTANCE OF THE MODIFIED 2-D TSV ARRAY

P	Measured(K/J)	Modeled(K/J)	Error
3	269.1	261.7	2.75%
4	207.72	205.20	1.2%
5	168.94	170.30	0.8%

and it does not influence the lateral thermal resistance because it does not change the lateral isothermal lines that are perpendicular to the thermal flow. Hence, the modeled resistance for the 2-D array is $2R_{TSVcell,cal,L}/3$, as it is a serial combination of two 1-D arrays shown in Fig. 12(a). The results show that the modeled thermal resistance closely matches the measured data for the 2-D TSV array as well.

As mentioned before, we expected that our proposed model is applicable to TSV of any arbitrary radius in silicon layer of different thickness. To test this, we perform the following changes to the array structure in Fig. 12.

1) Change the radius of TSV (r) to 10 μm, and the thickness of the insulation liner (δ) to 1 μm.
2) Change the thickness of silicon layer (h) to 10 μm, and keep the ratio of TSV space to TSV radius to be 3, 4, and 5 (set the space between two adjacent TSVs to be 30, 40, and 50 μm), respectively.

We repeat the experiment to measure the lateral thermal resistance contributed by the 2-D TSV array, and compare the data with the calculated model. In the procedure of calculating the modeled lateral thermal resistance, we use the same calibration parameter β_1 and β_2 obtained from our previous experiments to test their validity in a new structure. The result summarized in Table III confirms that the calculated thermal resistance closely matches its measured counterpart obtained from fine finite element simulation, which indicates the robustness of our proposed closed form model.

C. Experimental Results of Finite Difference Simulation

Finally, we demonstrate how the proposed model be used in finite difference thermal modeling method to improve modeling accuracy without incurring computation cost. As explained before, fine mesh grid modeling method is impractical for the thermal modeling of large scale TSV arrays. However, to demonstrate the accuracy improvement of our proposed method, it is very necessary to have golden results to compare with. In our experiment, we use COMSOL to build a scaled down chip structure with reduced number of TSV structures on it so that the fine grid finite element simulation tool could handle it and produce the thermal data that we could compare with. In this section, we use COMSOL to simulate two-layer stack structures connected by TSV arrays with different array dimensions.

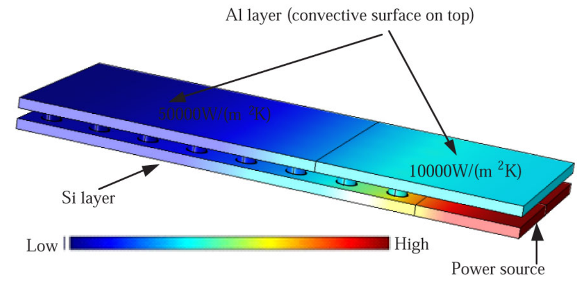


Fig. 13. Two layer chip structure with 4 × 8 TSV array and the temperature distribution simulated by COMSOL.

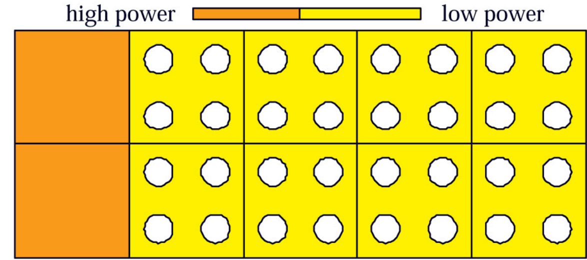


Fig. 14. 2-D bottom view of the 2 × 5 meshed chip and its power source configuration.

1) Temperature Responses of 4 × 8 TSV Array: The first structure used for temperature response test is shown in Fig. 13, which represents part of a 3-D stacked chip structure that could be built and simulated by COMSOL without incurring memory issue. Both the lateral dimensions of Si layer and the Al layer are 200 μm by 500 μm, and the thickness of Si layer is 10 μm, while the thickness of Al layer is 20 μm. The two layers are connected by a TSV array consists of 32 TSVs (4 × 8 array) in total as shown in Fig. 13. The radius of each TSV is 10 μm, the insulation liner thickness is 1 μm, and the space between two adjacent TSVs is 30 μm. The convective coefficient of the top surface of the Al layer is set to be 10 000 $W/(m^2K)$ and 50 000 $W/(m^2K)$ as shown in Fig. 13 to model the different convective cooling effects at different location of the chip package. We assume that the majority of the power sources should be located outside the TSV area, while inside the TSV area, the power density is relatively lower, creating energy flow in lateral direction that will be manifested by the lateral thermal resistance across the TSV arrays. In our setup, the step power sources of 3e6 W/m^2 are placed at the bottom of the silicon layer where there are no TSV arrays, and 1e6 W/m^2 power sources are placed at the area inside the TSV array as shown in Fig. 13. In this way, we could testify the lateral thermal effect of the TSV arrays in 3-D FD simulation using this reduced structure.

In this experiment, we compare the simulated temperature response from COMSOL with the one predicted by our proposed model, and we also compare the results from our proposed model against the existing one in [13]. In the FD method, coarse mesh grids are used to enable fast simulations, the bottom view of the 2 by 5 mesh grid is shown in Fig. 14. We remark that fine grid simulation could capture every details of the temperature gradient in the structure;

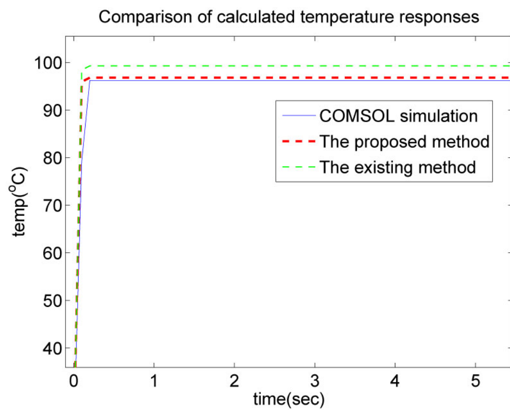


Fig. 15. Transient temperature responses of the two layer structure with 4 × 8 TSV array.

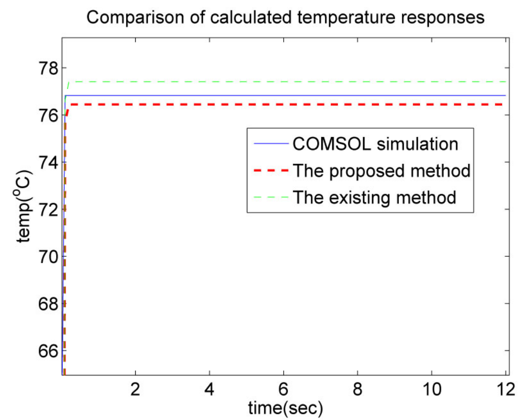


Fig. 16. Transient temperature responses of TSV grid in the two layer structure with 4 × 8 TSV array under reconfigured power sources.

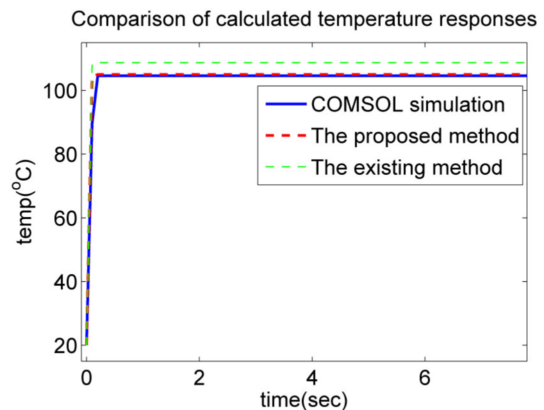


Fig. 17. Transient temperature responses of the two layer structure with 4 × 8 TSV array representing wide I/O memory.

however, the coarse grid method could only capture the average temperature of one mesh grid that has no TSVs in it, and capture the average temperature of silicon area for the grid with TSVs located inside. Normally, we are concerned with predicting the temperature of the locations where no TSVs present, because these are the locations where the temperature tends to exceed the alarming rate due to the less effective heat removal in these areas. Thus, we first compare the temperature responses of the silicon mesh grid.

The transient step temperature responses of one silicon mesh grid from different methods are plotted in Fig. 15. Clearly, we could see that the proposed model yield more accurate results because of its more accurate lateral thermal resistance model. The existing model does not consider the space between TSVs and thus overestimates the lateral thermal blockage effect, leading to 3.08 °C higher temperature prediction, while the proposed approach leads to only 0.6 °C deviations above the COMSOL simulation results.

We remark that the lateral thermal flow or gradient is important to manifest the effect of the lateral thermal resistance. If the lateral thermal flow is not significant, the effect and impacts of lateral thermal resistance will be reduced. To illustrate this, we reconfigure the power density, by swapping one high power source (3e6 W/m^2) on the silicon grid with its adjacent low power source (1e6 W/m^2) on a TSV grid. In this way, the majority of the heat generated by the high power source inside the TSV grid will flow vertically, because much less lateral thermal gradient is created under this power source configuration. Fig. 16 shows the comparison between the existing method and the proposed method for the temperature of the TSV grid that has high power source, which shows that the proposed method lead to limited accuracy gains (0.58 °C error using the existing method comparing with 0.38 °C error using the proposed method).

However, normally, the transistor devices needs to be placed away from TSVs for reliability concerns, and thus, the power in the array of TSV array should be lower, in which case large lateral thermal gradient would be formed, and the proposed model needs to be used. In some application cases, such as representing the TSV arrays for wide I/O memory in 3-D ICs, it is reasonable to assume that heat sources locate at the boundary of the TSV array, but not inside the array because the power of wide I/O memory is orders of magnitude lower than that of the arithmetic processor. And this is also the case when the lateral heat flow across the TSV array is maximized, and thus the influence of the lateral thermal resistance across the TSV arrays need to be carefully modeled. To represent this case, we reuse this structure with 4×8 TSV array, and place 5×10^6 W/m^2 power sources at the bottom of the silicon area where there is no TSV arrays, while inside the silicon area of TSV arrays, the source is set to be 0 W/m^2. In this case, the transient step temperature responses of one silicon mesh grid from different methods are plotted in Fig. 17. The existing model leads to 4.11 °C higher temperature prediction comparing with the COMSOL simulation results, which clearly demonstrates increased error (comparing with error of 3.08 °C in the previous test case) because the accuracy of the lateral thermal resistance of the TSV array displays more significant effect due to the increased lateral thermal flow in this configuration, while the error of the proposed approach is just 0.44 °C.

In both examples, the modeling and simulation time (using 120 time steps) of the proposed compact model is only 0.79 s, while the COMSOL simulation takes 2468 s, which is more than 3000 times longer, and thus unaffordable if simulating even larger structures. Hence, building compact model using accurate closed form lateral TSV model is very important to

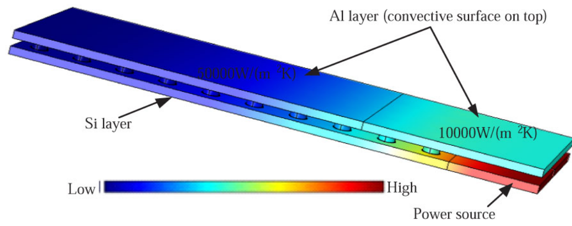


Fig. 18. Two layer chip structure with 4×10 TSV array and the temperature distribution simulated by COMSOL.

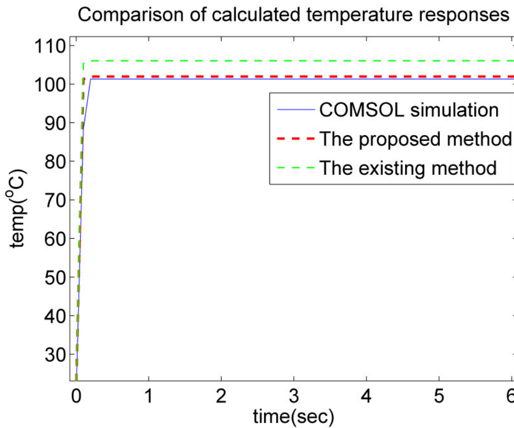


Fig. 19. Transient temperature responses of the two layer structure with 4×10 TSV array representing wide I/O memory.

capture the thermal response of 3-D chip with large numbers of TSVs.

2) Temperature Responses of 4×10 TSV Array: We remark that the small difference between the existing model and the proposed model on a reduced dimension structure may accumulate to more significant temperature differences in larger structure with much larger scale of TSVs and TSV arrays, which could not be built and simulated by fine grid simulation tools like COMSOL. However, to demonstrate this trend, we build a larger structure with 4×10 TSV arrays to show how the lateral thermal effect would be accumulated over the distances, and lead to increased temperature error if not properly considered. The structure built in COMSOL with 4×10 TSV array is shown in Fig. 18, in which the dimension of TSVs are still the same, the dimension of both Si layer and Al layer is $20\ \mu\text{m} \times 60\ \mu\text{m} \times 10\ \mu\text{m}$ to cover the 4×10 TSV arrays.

We assume that the TSV array represents low power wide I/O memory as it is the case when modeling lateral thermal resistance is more demanded. Like in the previous test case of wide I/O memory, we place $5 \times 10^6\ \text{W/m}^2$ sources at the bottom silicon layer outside of the area covered by TSV array. The simulated temperature response is shown in Fig. 19. The result using the existing model shows 4.75 °C differences away from the COMSOL simulation, which is about 0.64 °C error increment comparing with the wide I/O memory testing case with 4×8 TSV arrays (4.11 °C error) in the previous subsection, while the result using proposed model shows only 0.66 °C deviations away from the COMSOL simulation.

VI. Conclusion

In this paper, we have proposed a simple yet accurate physics-based analytical thermal resistance model for lateral TSV thermal resistance. Our research shows that lateral TSV model is not only a function of the geometry of the TSV such as radius and thickness of liner, but also strongly depends on the space between TSVs because of changes in the isothermal curves when TSVs are placed at different locations with respect to each other. With the proposed lateral TSV thermal resistance model and thus the new complete TSV model, one can build more compact grids for FD based analysis that considers the thermal impacts of TSVs. The compact models can be also used for architecture and system level thermal design and management. Experimental results show that the proposed TSV model, which is a function of the TSV geometry and space between TSVs, can lead to very small errors compared to the detailed numerical analysis, and thus improved the accuracy of FD thermal simulation. It also compares favorably with recently proposed TSV model in terms of accuracy.

References

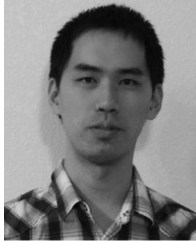
[1] J. Burns, "TSV-based 3D integration," in *Three Dimensional System Integration*, A. Papanikolaou, D. Soudris, and R. Radojcic, Eds. New York, NY, USA: Springer, Nov. 2010, pp. 13–22.
[2] R. Patti, "3D integration: New opportunities for advanced packaging," in *Proc. Electr. Perform. Electron. Package Syst. (EPEPS)*, Oct. 2011, pp. 1–41.
[3] P. Benkart *et al.*, "3D chip stack technology using through-chip interconnects," *IEEE Des. Test Comput.*, vol. 22, no. 6, pp. 512–518, Nov./Dec. 2005.
[4] G. H. Loh, Y. Xie, and B. Black, "Processor design in 3D die-stacking technologies," *IEEE Micro*, vol. 27, no. 3, pp. 31–48, May/Jun. 2007.
[5] B. Kim, C. Sharbono, T. Ritzdorf, and D. Schmauch, "Factors affecting copper filling process within high aspect ratio deep vias for 3D chip stacking," in *Proc. 56th Electron. Compon. Technol. Conf.*, San Diego, CA, USA, 2006.
[6] M. Motoyoshi, "Through-silicon via (TSV)," *Proc. IEEE*, vol. 97, no. 1, pp. 43–48, Jan. 2009.
[7] J. Cong, G. Luo, and Y. Shi, "Thermal-aware cell and through-silicon-via co-placement for 3D ICs," in *Proc. Design Autom. Conf. (DAC)*, San Diego, CA, USA, 2011, pp. 670–675.
[8] Y. Shang *et al.*, "Thermal-reliable 3D clock-tree synthesis considering nonlinear electrical-thermal-coupled TSV model," in *Proc. 2013 18th Asia South Pacific Design Autom. Conf. (ASP-DAC)*, Yokohama, Japan, pp. 693–698.
[9] M. Sai, H. Yu, Y. Shang, C. S. Tan, and S. K. Lim, "Reliable 3-D clock-tree synthesis considering nonlinear capacitive TSV model with electrical-thermal-mechanical coupling," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 32, no. 11, pp. 1734–1747, Nov. 2013.
[10] A. Jain, R. E. Jones, R. Chatterjee, and S. Pozder, "Thermal modeling and design of 3D integrated circuits," in *Proc. 11th Intersoc. Conf. Thermal Thermomech. Phenom. Electron. Syst.*, Orlando, FL, USA, May 2008, pp. 1139–1145.
[11] J. L. Ayala, A. Sridhar, and D. Cuesta, "Thermal modeling and analysis of 3D multi-processor chips," *Integr. VLSI J.*, vol. 43, pp. 327–341, Sep. 2010.
[12] Y. Chen, E. Kursun, D. Motschman, C. Johnson, and Y. Xie, "Analysis and mitigation of lateral thermal blockage effect of through-silicon-via in 3D IC designs," in *Proc. 17th IEEE/ACM Int. Symp. Low-Power Electron. Design (ISLPED)*, Piscataway, NJ, USA, 2011, pp. 397–402.
[13] H. Xu, F. V. Pavlidis, and D. G. Micheli, "Analytical heat transfer model for thermal through-Silicon vias," in *Proc. Eur. Design Test Conf. (DATE)*, Grenoble, France, 2011, pp. 1–6.
[14] (2014, Jul. 10). *COMSOL Mutiphysics: User Guide*, Version 4.1 [Online]. Available: www.comsol.com
[15] M. N. Ozisik, *Finite Difference Methods in Heat Transfer*. Boca Raton, FL, USA: Taylor & Francis, 1994.
[16] Y.-K. Cheng, C.-C. Teng, S.-M. Kang, and C.-H. Tsai, *Electrothermal Analysis of VLSI Systems*. New York, NY, USA: Cambridge Univ. Press, 2000.

[17] H. Qian, H. Liang, C. H. Chang, W. Zhang, and H. Yu, "Thermal simulator of 3D-IC with modeling of anisotropic TSV conductance and microchannel entrance effects," in *Proc. Asia South Pacific Design Autom. Conf. (ASPDAC)*, Yokohama, Japan, 2013.

[18] Z. Chen, X. Luo, and S. Liu, "Thermal analysis of 3D packaging with a simplified thermal resistance network model and finite element simulation," in *Proc. Electron. Packag. Technol. High Density Packag.*, Xi'an, China, 2010, pp. 737–741.

[19] T. Bergman, A. Lavine, F. P. Incropera, and D. P. DeWitt, *Fundamentals of Heat and Mass Transfer*, 7th ed. New York, NY, USA: Wiley, 2011.

[20] J. Xie, B. Xie, and M. Swaminathan, "Electrical-thermal modeling of through-silicon via (TSV) array in interposer," *Int. J. Numer. Model. Electron. Netw. Devices Fields*, vol. 26, no. 6, pp. 545–559, Nov./Dec. 2013.



Zao Liu received the M.S. degree in electrical and computer engineering from Northeastern University, Boston, MA, USA, in 2010, and the Ph.D. degree with the University of California, Riverside, Riverside, CA, USA, in 2014.

He is currently with Intel Corporation, Santa Clara, CA, USA. His current research interests include package level thermal modeling and reliability management for VLSI chip and multicore processor systems.

Sahana Swarup was born in India in 1984. She received the B.E. degree in electrical engineering from the M. S. Ramaiah Institute of Technology, Bangalore, India, in 2006, and the M.S. degree in electrical engineering from California State University, Northridge, Northridge, CA, USA, in 2009. She is currently pursuing the Ph.D. degree in electrical engineering from the University of California, Riverside, Riverside, CA, USA.

Her current research interests include thermal and electromagnetic modeling of 3-D stacked ICs and IC design.

Sheldon X.-D. Tan (S'96–M'99–SM'06) received the B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, IA, USA, in 1999.

He is a Professor with the Department of Electrical Engineering, University of California, Riverside, Riverside, CA, USA. He has been an Associate Director of Computer Engineering Program, Bourn College of Engineering, University of California, Riverside (UCR), Riverside, CA, USA, since 2009. He is also a Cooperative Faculty Member with the Department of Computer Science and Engineering at UCR. His current research interests include reliable and robust nanometer chip design techniques, fast thermal analysis, modeling and dynamic thermal management for microprocessors and platform systems, parallel circuit simulation techniques based on GPU and multicore systems, and embedded system designs based on FPGA platforms, and statistical modeling, simulation and optimization of mixed-signal/RF/analog circuits. He also co-authored five books, including *Symbolic Analysis and Reduction of VLSI Circuits* (Springer/Kluwer, 2005), and *Advanced Model Order Reduction Techniques for VLSI Designs* (Cambridge University Press, 2007), and *Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs* (Springer, 2012).

Dr. Tan was serving as an Associate Editor for three journals: *ACM Transaction on Design Automation of Electronic Systems*, *Integration*, *The VLSI Journal*, and *Journal of VLSI Design*. He received the Outstanding Oversea Investigator Award from the National Natural Science Foundation of China in 2008, the NSF CAREER Award in 2004, the Best Paper Award from the 2007 IEEE International Conference on Computer Design (ICCD'07), three Best Paper Award Nominations from the 2005, 2009, and 2014 IEEE/ACM Design Automation Conferences, and the Best Paper Award from the 1999 IEEE/ACM Design Automation Conference. He served as a Technical Program Committee Member or Sub-Topic Chair for DAC, ICCAD, ASPDAC, ICCD, and ISLPED.

Hai-Bao Chen received the B.S. degree in information and computing sciences, and the M.S. and Ph.D. degrees in applied mathematics from Xi'an Jiaotong University, Xi'an, China, in 2006, 2008, and 2012, respectively.

He then joined Huawei Technologies, where he focused on cloud computing and big data. He was a Post-Doctoral Research Fellow with Electrical Engineering Department, University of California, Riverside, Riverside, CA, USA, from 2013 to 2014. He is currently a Lecturer with the School of Microelectronics, Shanghai Jiao Tong University, Shanghai, China. His current research interests include model order reduction, system and control theory, circuit simulation, cloud computing and big data, and electromigration reliability.

Hai Wang received the B.S. degree from the Huazhong University of Science and Technology, Wuhan, China, in 2007, and the M.S. and Ph.D. degrees from the University of California, Riverside, Riverside, CA, USA, in 2008 and 2012, respectively.

He is currently an Associate Professor with the University of Electronic Science and Technology of China, Chengdu, China. His current research interests include electrical/thermal verification and optimization of VLSI circuits and systems. He has published around 30 peer-reviewed papers in related research fields.

Dr. Wang serves as a Technical Program Committee Member of several international conferences, including DATE, ASP-DAC, and ISQED, and also serves as a Reviewer of many journals, including the IEEE TRANSACTIONS ON COMPUTERS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS II, and *ACM Transaction on Design Automation of Electronic Systems*.