Fast Variational Analysis of On-Chip Power Grids by Stochastic Extended Krylov Subspace Method

Ning Mi, *Student Member, IEEE*, Sheldon X.-D. Tan, *Senior Member, IEEE*, Yici Cai, *Member, IEEE*, and Xianlong Hong, *Fellow, IEEE*

***Abstract*—This paper proposes a novel stochastic method for analyzing the voltage drop variations of on-chip power grid networks, considering lognormal leakage current variations. The new method, called *StoEKS*, applies Hermite polynomial chaos to represent the random variables in both power grid networks and input leakage currents. However, different from the existing orthogonal polynomial-based stochastic simulation method, extended Krylov subspace (EKS) method is employed to compute variational responses from the augmented matrices consisting of the coefficients of Hermite polynomials. Our contribution lies in the acceleration of the spectral stochastic method using the EKS method to fast solve the variational circuit equations for the first time. By using the reduction technique, the new method partially mitigates increased circuit-size problem associated with the augmented matrices from the Galerkin-based spectral stochastic method. Experimental results show that the proposed method is about two-order magnitude faster than the existing Hermite PC-based simulation method and many order of magnitudes faster than Monte Carlo methods with marginal errors. StoEKS is scalable for analyzing much larger circuits than the existing Hermit PC-based methods.**

***Index Terms*— Extended Krylov subspace method, on-chip power grids, statistic analysis.**

I. Introduction

PROCESS-INDUCED variability becomes the major design concern in the current 65-nm and coming 45-nm very large scale integration (VLSI) technologies [28]. The process-induced variations manifest themselves from wafer to wafer, die to die, and device to device within a die [4], [19], [20]. Some of the variations are systematic, like those caused by lithograph processes. Some are purely random, like the doping density of impurities and edge or thickness roughness due to the chemical etching and chemical mechanical polishing processes. As the technology moves to 65 nm and even to 45 nm, the variation will become more and more significant.

Manuscript received August 28, 2007; revised February 18, 2008 and May 13, 2008. Current version published October 22, 2008. This work was supported in part by National Science Foundation awards under No. CCF-0448534, No. OISE-0623038, and in part by National Natural Science Foundation of China (NSFC) under Grant No. 60828008. Some preliminary results of this paper were presented at the Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) [18]. This paper was recommended by Associate Editor J. R. Phillips.

N. Mi and S. X.-D. Tan are with the Department of Electrical Engineering, University of California at Riverside, Riverside, CA 92521 USA (e-mail: nmi@ee.ucr.edu; stan@ee.ucr.edu).

Y. Cai and X. Hong are with the Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCAD.2008.2006077

One important variation is the threshold voltage $V_{\rm th}$ variation. One reason is that subthreshold leakage current has a rapid increasing rate (about 5 to 10 times increase per technology generation [5]). Moreover, subthreshold leakage current is highly sensitive to threshold voltage $V_{\rm th}$ variation, as the leakage current has exponential dependence on the threshold voltage $V_{\rm th}$. If we model $V_{\rm th}$ as a random variable with Gaussian distribution from interdie or intradie process variations, the leakage currents will have a lognormal distribution, as shown in [23]. As a result, leakage currents should be considered for variational analysis for important global interconnects like power grid networks.

A number of research works have been proposed recently to address the voltage-drop-variation issues in the on-chip power delivery networks under process variations. The voltage drop of power grid networks subject to the leakage current variations was first studied in [6] and [7]. This method assumes that the lognormal distribution of the node voltage drop is caused by lognormal leakage current inputs and is based on a localized Monte Carlo [(MC); sampling] method to compute the variance of the node voltage drop. However, this localized sampling method is limited to the static dc solution of power grids modeled as resistor-only networks. Therefore, it can only compute the responses to the standby leakage currents. However, the dynamic leakage currents become more significant, particularly when the sleep transistors are intensively used nowadays for reducing leakage powers. In [21] and [24], impulse responses are used to compute the means and variances of node voltage responses due to general current variations. However, this method needs to know the impulse responses from all the current sources to all the nodes, which is expensive to compute for a large network. This method also cannot consider the variations of the wires in the power grid networks.

Recently, a number of analysis approaches based on the so-called spectral stochastic analysis method have been proposed for analyzing interconnect and power grid networks [9], [10], [15], [26]. This method is based on the orthogonal polynomial chaos expansion of random processes and the Galerkin theory to represent and solve for the stochastic responses of statistical linear dynamic systems. The orthogonal polynomial method, also known as the spectral stochastic method, only needs to solve for some coefficients of the orthogonal polynomials by using normal transient simulation of the original circuits. The research work in [26] applied the spectral stochastic method to compute the variational delay of interconnects. In [9] and [10], the spectral stochastic method has been applied to compute the voltage drop variations caused by Gaussian-only variations in

the power grid wires and input currents (approximating them as Gaussian variations by using first-order Taylor expansion). Intradie variations can be considered in [9]. Recently, the authors extended the spectral stochastic method by specifically considering the lognormal leakage variations to solve for the variational voltage drops in on-chip power grid networks [15], [16]. Spatial correlations were also considered in [17].

In this paper, we propose a new stochastic method for analyzing the voltage drop variations of on-chip power grid networks with lognormal leakage current variations. The new method, called *StoEKS*, still applies the spectral stochastic method to solve for the variational responses. However, different from the existing spectral–stochastic-based simulation method, the extended Krylov subspace (EKS) method [25], [27] is employed to compute variational responses using the augmented matrices consisting of the coefficients of Hermite polynomials. Our work is inspired by recent spectral–stochastic-based model order reduction method [30]. We apply this work to the variational analysis of on-chip power grid networks, considering the variational leakage currents with the lognormal distribution.

Our contribution lies in the acceleration of the spectral stochastic method using the EKS method to fast solve the variational circuit equations for the first time. By using the Krylov-subspace-based reduction technique, the new method partially mitigates the increased circuit-size problem associated with the augmented matrices from the Galerkin-based spectral stochastic method. We will show how the coefficients of Hermite PCs are computed for variational circuit matrices and for the current moments used in EKS with lognormal distribution. Experimental results show that the proposed StoEKS is about two-order magnitude faster than the existing Hermite PC-based simulation method, having similar error compared with MC method. StoEKS can analyze much larger circuits than the existing Hermite PC method in the same computation platform.

The rest of this paper is organized as follows. Section II first presents the variational power grid models and the problem we plan to solve. Section III reviews the orthogonal polynomial chaos-based stochastic simulation method and the improved EKS (IEKS) method. Section IV presents our new statistical power grid simulation method. Section V presents the experimental results, and Section VI concludes this paper.

II. Problem Formulation

In this section, we first present the model of power grids used in this paper. We then present the modeling issue of leakage currents under intradie variation. After this, we present the problem that we try to solve.

A. On-Chip Power Grid Network Models

The power grid networks in this paper are modeled as RC networks with known time-variant current sources, which are obtained by the gate-level logic simulations of the VLSI systems. For a power grid (versus the ground grid), some nodes have known voltages modeled as constant voltage sources. For C4 power grids, the known voltage nodes can be nodes inside the power grid. Given a known deterministic vector of current sources $u(t)$, the node voltages can be obtained by solving the following linear differential equation, which is formulated using modified nodal analysis (MNA) approach

$$Gv(t) + C\frac{dv(t)}{dt} = Bu(t) \tag{1}$$

where $G \in R^{m\times m}$ is the conductance matrix, and $C \in R^{m\times m}$ is the admittance matrix resulting from storage elements. $B \in R^{m\times l}$ and $u(t) \in R^{l\times 1}$ are vectors of time-varying node currents. m is the size of the given circuit, and l is the number of input ports.

B. Variational Power Grid Models

The G, C matrices and input currents $u(t)$ depend on the circuit parameters, such as metal wire width, length, metal thickness on power grids, and transistor parameters, such as channel length, width, gate oxide thickness, etc. Process-induced random variations can be roughly classified into interdie (die to die) and intradie variations. In interdie variations, all the parameter variations are correlated. The worst case corner can be easily found by setting the parameters to their range limits (mean plus 3σ). The difficulty lies in the intradie variations, where the circuit parameters are not correlated or spatially correlated. Intradie variations also consist of local and layout dependent deterministic components and random components.

In this paper, we focus on the random variations, which typically are modeled as multivariate Gaussian process with spatial correlations [2]. In this paper, we focus on the strongly correlated random variables. The reasons are that weakly or uncorrelated random variations have smaller impacts on the leakage and wire variations than that of the highly correlated random variables, as the variance of the sum of n independent random variables is $\sim n\sigma^2$ while the variance of the sum of n highly correlated random variables is $\sim n^2\sigma^2$. Hence, for computing efficiency [by using principal component analysis (PCA)], ignoring those uncorrelated variations in the presence of strongly correlated variations will not lead to large errors in the final results.

In this paper, we assume that we have a number of independent (uncorrelated) transformed orthonormal Gaussian random variables $\xi_i(\theta)$, where $i = 1, \ldots, n$, which actually model the channel length and the device threshold voltage variations. The spatial correlation in the intradie variation can be processed by using the Karhunen–Loeve (K–L) transformation PCA method, which is the discretized version of K–L method [14], to transform the correlated variables into uncorrelated variables before spectral statistical analysis [10], [15].

Let Θ denote the process sampling space. Let $\theta \in \Theta$, $\xi_i : \theta \to R$ denote a normalized Gaussian variable, and $\xi(\theta) = [\xi_{1d}(\theta), \ldots, \xi_{rd}(\theta)]$ is a vector of r Gaussian variables. After an orthogonal transformation operation, we obtain independent random variable vectors $\xi = [\xi_1, \ldots, \xi_n]$. Notice that $n \leq r$ in general. The PCA method can be either used to strongly correlated dependent or weak correlated random variables. The

difference between the two circumstances is the number of independent variables, which is denoted as n here. After doing PCA, strongly correlated random variables and the independent random variable vector $\xi = [\xi_1, \ldots, \xi_n]$ are in small size. In other words, the number of random variables are reduced a lot, while for weak correlated, the number of independent random variables is not reduced a lot. Our method can deal with both strongly and weak correlated random variables.

Therefore, given the process variations, the MNA equation for (1) becomes

$$G(\xi)v(t,\xi) + C(\xi)\frac{dv(t,\xi)}{dt} = Bu(t,\xi). \tag{2}$$

In this paper, we assume that the variational current source in (2) $u(t,\xi)$ consists of two components

$$u(t,\xi) = u_d(t) + u_v(t,\xi) \tag{3}$$

where $u_d(t)$ is the dynamic current vector from circuit switching, which is still modeled as deterministic currents as we only consider the leakage variations. $u_v(\xi,t)$ is the variational leakage current vector, which is dominated by subthreshold leakage currents, and it may also change over time. $u_v(t,\xi)$ follows the lognormal distribution.

The problem we need to solve is to efficiently find the mean and variance of voltage $u(t,\xi)$ at any node at any time instance without using the time-consuming sampling-based method, such as MC.

III. Review of Spectral Stochastic and EKS Methods

In the following, we briefly reviewed the spectral–stochastic-based simulation with Hermite polynomial chaos (HPC) used in [9], [10], and [15].

A. Concept of HPC

Hermite PC utilizes a series of orthogonal polynomials (with respect to the Gaussian distribution) to facilitate stochastic analysis [29]. These polynomials are used as the orthogonal basis to decompose a random process in the similar way as sine and cosine functions are used to decompose a periodic signal in Fourier series expansion.

For a random variable $v(t,\xi)$ with limited variance, where $\xi = [\xi_1, \xi_2, \ldots, \xi_n]$ is a vector of n independent orthonormal Gaussian random variables with zero mean. Then, the random part can be approximated by truncated Hermite PC expansion as follows [8]:

$$v(t,\xi) = \sum_{k=0}^{P} a_k(t) H_k^n(\xi) \tag{4}$$

where $H_k^n(\xi)$ is the n-dimensional Hermite polynomials, and $a_k(t)$ is the deterministic coefficient. Since the random variables ξ are independent with time, the coefficients $a_k(t)$ are changed with time. The number of terms P is given by

$$P = \sum_{k=0}^{p} \frac{(n-1+k)!}{k!(n-1)!} \tag{5}$$

where p is the order of the Hermite PC. In general, the pth order Hermite polynomial is defined as

$$H_p(\alpha_1, \alpha_2, \ldots, \alpha_p) = (-1)^p e^{\xi^2/2} \frac{\partial^p}{\partial\alpha_1, \partial\alpha_2, \ldots, \partial\alpha_p} e^{-\xi^2/2} \tag{6}$$

where α_i is any set of p variables chosen from the set $[\xi_1, \xi_2, \ldots, \xi_n]$, allowing repetitions. When one random variable is considered, the first, second, and third Hermite polynomials are defined as

$$H_0^1(\xi)=1,\ H_1^1(\xi)=\xi,\ H_2^1(\xi)=\xi^2-1,\ H_3^1(\xi)=\xi^3-3\xi, \ldots \tag{7}$$

Hermite polynomials are orthogonal with respect to Gaussian weighted expectation (the superscript n is dropped for simple notation)

$$\langle H_i(\xi), H_j(\xi)\rangle = \langle H_i^2(\xi)\rangle\, \delta_{ij} \tag{8}$$

where δ_{ij} is the Kronecker delta, and $\langle {}^*, {}^* \rangle$ denotes an inner product defined as follows:

$$\langle f(\xi), g(\xi)\rangle = \frac{1}{\sqrt{(2\pi)^n}} \int f(\xi) g(\xi) e^{-\frac{1}{2}\xi^{\mathrm{T}}\xi}\, d\xi. \tag{9}$$

Like Fourier series, the coefficient a_k can be found by a projection operation onto the Hermite PC basis

$$a_k(t) = \frac{\langle v(t,\xi), H_k(\xi)\rangle}{\langle H_k^2(\xi)\rangle} \quad \forall k \in \{0, \ldots, P\}. \tag{10}$$

B. Simulation Approach Based on Hermite PCs

Suppose that $v(t,\xi)$ is an unknown random variable vector (with unknown distributions) like node voltages in (2), the coefficients can be computed by using the Galerkin method, which states that the best approximation of $v(t,\xi)$ is obtained when the error $\Delta(t,\xi)$, which is defined as

$$\Delta(t,\xi) = G(\xi)v(t) + C(\xi)\frac{dv(t)}{dt} - Bu(t,\xi) \tag{11}$$

is orthogonal to the approximation. That is

$$\langle \Delta(t,\xi), H_k(\xi)\rangle = 0, \quad i = 0, 1, \ldots, P. \tag{12}$$

In this way, we transform the stochastic analysis process to a deterministic process, where we only need to compute the coefficients of the Hermite PCs for responses we are interested in.

Algorithm: EKS ALGORITHM
Input: G,C,B,$u(t)$ and moment order q
Output: Orthogonal basis $V = \{\hat{v}_0, \hat{v}_2, ...\hat{v}_{q-1}\}$

```
1  v̂_0 = α_0 v_0, where v_0 = G^{-1} B u_0, α_0 = 1/norm(v_0);
2  set h_s = 0;
3  for i = 1 : q − 1
4      v_i = G^{-1}{Π_{j=0}^{i-1} α_j B u_i − C(v̂_{i-1} + α_{i-1} h_s)};
5      h_s = 0;
6      for j = 0 : i − 1
7        h = v̂_j^T v_i;
8        h_s = h_s + h v̂_j;
9      end
10     v̄_i = v_i − h_s;
11     α_i = 1/norm(v̄_i);
12     v̂_i = α_i v̄_i
13 end
```

Fig. 1. EKS algorithm.

C. EKS Methods

In this section, we briefly review the EKS method in [12] and [27] for the fast computation of responses from linear dynamic systems.

The EKS method uses the Krylov-like reduction method to speed up the simulation process. Different from the Krylov-based model order reduction method, EKS performs the reduction, considering both system matrices and input signals before the simulation (so that the subspace is no longer Krylov subspace). Thus, it essentially is a simulation approach using the Krylov subspace reduction method. It assumes that input signals can be represented by piecewise linear (PWL) sources.

Let $V = [\hat{v}_1, \hat{v}_2, \ldots, \hat{v}_k]$ be an orthogonal basis for moment subspace $(m_0, m_1, \ldots, m_k)$ of input $u(t)$. Fig. 1 shows the high-level description of the EKS algorithm [27].

Then, the original circuit described by (1) can be reduced to a smaller system

$$\hat{G}z + \hat{C}\frac{dz(t)}{dt} = \hat{B}u \tag{13}$$

where

$$\hat{G} = V^{\mathrm{T}}GV \qquad \hat{C} = V^{\mathrm{T}}CV$$
$$\hat{B} = V^{\mathrm{T}}B \qquad v(t) = Vz(t).$$

After the reduced system in (13) has been solved for the given input $u(t)$, the solution $z(t)$ can then be mapped back into the original space by $v(t) = Vz(t)$.

As the EKS models a PWL source as a sum of delayed ramps in Laplace domain, the terms, however, contain $1/s$ and $1/s^2$ moments [27], while the traditional Krylov space starts from zeroth moment. Therefore, moment shifting must be made in EKS, which would cause complex computation and more errors. This problem is resolved in [12] in the IEKS algorithm, which shows that the moments of $1/s$ and $1/s^2$ are zeros for PWL input sources.

Assume that we want to obtain a single input source $u_j(s)$ in the following moment form:

$$u_j(s) = u_1 + u_2 s + u_3 s^2 + \cdots + u_L s^{L-1}.$$

A PWL source $u_j(t)$ is represented by a series of value–time pairs such as $(a_1, \tau_1), (a_2, \tau_2), \ldots, (a_{K+2}, \tau_{K+2})$ and L moments needed to be calculated. As proposed in [12], the mth moment for current source $u_j(t)$ in a current source vector $u(s)$ can be calculated as

$$u_{j,m} = \left(a_1 - \alpha_1 \frac{\tau_1}{m+1}\right)\beta_1^{(m)} - \sum_{i=1}^{k}(\alpha_i - \alpha_{i+1})\beta_{i+1}^{(m+1)}$$
$$- \left(a_{K+2} - \alpha_{K+1}\frac{\tau_{k+2}}{m+1}\right)\beta_{K+2}^{(m)}, \qquad m = 1, \ldots, L. \tag{14}$$

Here

$$\beta_i^{(m)} = \frac{(-\tau_i)^m}{m!} \qquad \alpha_i = \frac{a_{i+1} - a_i}{\tau_{i+1} - \tau_i}.$$

The EKS/IEKS method, however, has its limitations. One major drawback is that current sources have to be represented in the explicit moment form, which may not be accurate and not numerically stable when high order moments are employed for high-frequency rich current waveforms owning to the well-known problem in the explicit moment matching method [22].

Recently, a more stable and accurate algorithm, called the extended truncated balanced realization, has been proposed [13], which is based on more accurate fast truncated balanced reduction method. It uses a frequency spectrum to represent the current sources and thus is more flexible and accurate. Since our contribution in this paper is not about improving the EKS method, we just use EKS as a baseline algorithm for StoEKS.

IV. New Stochastic EKS Method—StoEKS

In this section, we present the new stochastic simulation algorithm StoEKS, which is based on both the spectral stochastic method and the EKS method [27]. The main idea is that we use the spectral stochastic method to convert the statistical simulation into a deterministic simulation problem. Then, we apply EKS to solve the converted problem.

A. StoEKS Algorithm Flowchart

First, we present StoEKS algorithm flowchart, which is shown in Fig. 2. The algorithm starts with variational $G(\xi)$, $C(\xi)$, and input source $u(t, \xi)$. Then, it applies spectral stochastic method to convert the variational system (2) into a deterministic system, which consists of augmented matrices of $G(\xi)$ and $C(\xi)$ and position matrix B in (2) with new unknowns. Then, we generate the first L moments of coefficients of the Hermite polynomial of current sources U_L with lognormal distribution. Finally, we apply EKS/IEKS to solve the obtained deterministic system for response Z using the computed projection matrix V. After this, we get back to the transient response of the original augmented system by $v(t) = Vz(t)$. Finally, we compute the mean and variance of any voltage nodes from $v(t)$.

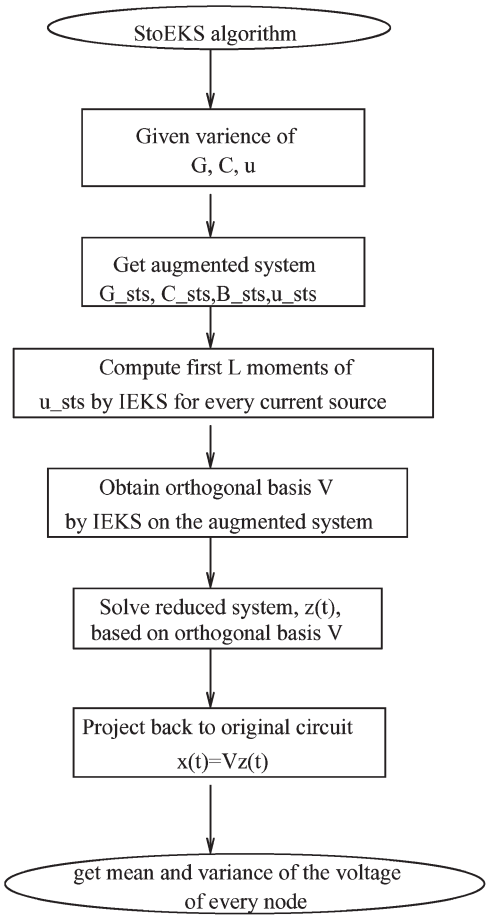


Fig. 2. Flowchart of the StoEKS algorithm.

In the following sections, we present the detailed descriptions for some critical steps of the StoEKS algorithm.

B. Generation of the Augmented Circuit Matrices

We first show how we convert the variational circuit equation into a deterministic one, which is suitable for EKS. This paper follows the recent proposed stochastic model order reduction (SMOR) method [30]. SMOR is based on HPC and the Krylov-based projection method.

We first assume that $G(\xi)$, $C(\xi)$, and $u(t,\xi)$ in (2) are represented in Hermite PC forms with a proper order P

$$G(\xi) = G_0 + G_1 H_1(\xi) + G_2 H_2(\xi) + \cdots + G_P H_P(\xi)$$

$$C(\xi) = C_0 + C_1 H_1(\xi) + C_2 H_2(\xi) + \cdots + C_P H_P(\xi)$$

$$u(t,\xi) = (u_0(t) + u_d(t)) + u_1(t) H_1(\xi) + \cdots + u_P(t) H_P(\xi).$$

Here, $H_i(\xi)$ denotes the Hermite PC basis functions for $G(\xi)$, $C(\xi)$, and $u(t,\xi)$. P is also the number of these basis functions, which depends on the number of random variables n and the expansion order p in (5). G_i, C_i, and u_i are the Hermite polynomial coefficients of conductance, capacitors, and current source, respectively. G_0 and C_0 are the mean values of conductance and capacitors, respectively. G_i and C_i are variational parts for conductance and capacitors, respectively.

Ideally, to obtain the G and C in the HPC format, i.e., to compute G_i and C_i from the width and length variables, one can use stochastic spectral analysis method [11], which is a fast MC method or other extraction methods. For this paper, we simply assume that we obtain such information, The detail of how G_i and C_i are obtained is as follows:

$$G_i = a_i * G_0$$
$$C_i = a_i * C_0, \qquad i = 1, \ldots, P \tag{15}$$

a_i is the variational percentage for H_i.

Substitute (15) into (2), the system equations become

$$\sum_{i=0}^{P-1}\sum_{j=0}^{P-1} G_i v_j H_i H_j + s \sum_{i=0}^{P-1}\sum_{j=0}^{P-1} C_i v_j H_i H_j = u_d(t) + \sum_{i=0}^{P-1} u_i(t) H_i. \tag{16}$$

Here, v_i denotes the coefficient of Hermite polynomial of node voltages $v(t,\xi)$ as

$$v(t,\xi) = v_0(t) + v_1(t) H_1 + v_2(t) H_2 + \cdots + v_{P-1}(t) H_{P-1} \tag{17}$$

After performing the inner product of H_k on both sides of (16), it will become

$$\sum_{i=0}^{P-1}\sum_{j=0}^{P-1} G_i v_j \langle H_i H_j, H_k\rangle + s \sum_{i=0}^{P-1}\sum_{j=0}^{P-1} C_i v_j \langle H_i H_j, H_k\rangle = \sum_{i=0}^{P-1} u_i \langle H_i, H_k\rangle + \langle H_k, 1\rangle v_d(t), \qquad k = 0, 1, \ldots, P-1 \tag{18}$$

where $\langle H_i H_j, H_k\rangle$ is the inner product of $H_i H_j$ and H_k. On the right-hand side of (18), the inner product is calculated based on H_i and H_k.

Notice that $\langle H_k, 1\rangle = 1$, when $k = 0$; $\langle H_k, 1\rangle = 0$, when $k \neq 0$. In general, the coefficients of $H_i H_j$ are calculated in (16), and the inner product is defined as

$$\langle H_i H_j, H_k\rangle = \int_{-\infty}^{+\infty} H_i H_j H_k \, d\xi \tag{19}$$

considering the independent of Hermite polynomial H_i, H_j, and H_k. Moreover, the inner product is similar for

$$\langle H_i, H_j\rangle = \int_{-\infty}^{+\infty} H_i H_j \, d\xi. \tag{20}$$

The inner product is a constant and can be computed *a priori* and stored in a table for fast computation. Based on the

P equations and the orthogonal nature of the Hermite polynomials, these equations can be written in matrix form as

$$(G_{sts}+sC_{sts})V = B_{sts}u_{sts} \tag{21}$$

$$G_{sts} = \begin{bmatrix} G_{00} & \cdots & G_{0P-1} \\ \vdots & \ddots & \vdots \\ G_{P0} & \cdots & G_{P-1P-1} \end{bmatrix}$$

$$C_{sts} = \begin{bmatrix} C_{00} & \cdots & C_{0P-1} \\ \vdots & \ddots & \vdots \\ C_{P-10} & \cdots & C_{P-1P-1} \end{bmatrix}$$

$$u_{sts} = \begin{bmatrix} u_0(t)+u_d(t) \\ u_1(t) \\ \vdots \\ u_{P-1}(t) \end{bmatrix} \qquad V = \begin{bmatrix} V_0(t) \\ V_1(t) \\ \vdots \\ V_{P-1}(t) \end{bmatrix} \tag{22}$$

$$B_{sts} = \begin{bmatrix} B_0 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & B_{P-1} \end{bmatrix} \tag{23}$$

$$B_i = B$$

$$G_{kj} = \sum_{i=0}^{P-1} G_i \langle H_i H_j, H_k \rangle$$

$$C_{kj} = \sum_{i=0}^{P-1} C_i \langle H_i H_j, H_k \rangle$$

where $G_{sts} \in R^{mP\times mP}$, $C_{sts} \in R^{mP\times mP}$, $B_{sts} \in R^{mP\times l}$, m is the size of the original circuit, and P is the number of Hermite polynomials. In [30], PRIMA-like reduction is performed on (21) to obtain the reduced variational system.

C. Computation of the Hermite PCs of Current Moments With Lognormal Distribution

In this section, we show how to compute the Hermite coefficients for the variational leakage currents and their corresponding moments used in the augmented equation (21).

Let $u_v^i(t,\xi)$ be the ith current in the current vector $u_v(t,\xi)$ in (3), which is a function of the normalized Gaussian random variables $\xi = [\xi_1, \xi_2, \ldots, \xi_n]$ and time t

$$u_v^i(t,\xi) \sim e^{g(t,\xi)} = e^{\sum_{j=0}^{n} g_j(t)\xi_j}. \tag{24}$$

The leakage current sources are therefore following the lognormal distribution. We can then present $u_v^i(t,\xi)$ by using Hermite PC expansion form

$$\begin{aligned} u_v^i(t,\xi) &= \sum_{k=0}^{P} u_{vk}^i(t) H_k^n(\xi) \\ &= u_{v0}^i(t)\left(1 + \sum_{i=1}^{n} \xi_i g_i(t) \right. \\ &\qquad \left. + \sum_{i=1}^{n}\sum_{j=1}^{n} \frac{(\xi_i\xi_j - \delta_{ij})}{\langle (\xi_i\xi_j - \delta_{ij})^2 \rangle} g_i(t) g_j(t) + \cdots \right) \end{aligned} \tag{25}$$

where

$$u_{v0}^i(t) = e^{g_0(t)+\frac{1}{2}\sum_{i=1}^{n} g_i(t)^2} \qquad P = \sum_{k=0}^{p} \frac{(n-1+k)!}{k!(n-1)!}. \tag{26}$$

n is the number of random variables, and p is the order of Hermite PC expansion.

As a result, the variational variable $u(t,\vec{\xi})$ leads to the u_{sts} in (21)

$$u_{sts} = \left[u_0(t)^{\mathrm{T}} + u_d(t)^{\mathrm{T}}, u_1(t)^{\mathrm{T}}, \ldots, u_{P-1}(t)^{\mathrm{T}}\right]^{\mathrm{T}}. \tag{27}$$

Note that $u_d(t)$ is the deterministic current source vector.

In the EKS method, we need to compute the moments of input sources in frequency domain. Suppose that (a_{i1}, τ_{i1}), $(a_{i2}, \tau_{i2}), \ldots, (a_{iK+2}, \tau_{iK+2})$ denotes the PWL series of value–time pairs for $u_i(t)$ or $u_0(t) + u_d(t)$ in (27). Using (14), we can get the first L moments for each u_i, $i = 1, 2, \ldots, P$ in (27), respectively, and we have

$$u_i(s) = m_{u_{i1}} + m_{u_{i2}} s+, \ldots, m_{u_{iL}} s^{L-1} \tag{28}$$

where $m_{u_{ik}}$ is the kth order moment vector of Hermite PC coefficient for u_i. In this way, we can compute the moments of Hermite PC coefficients for every current sources.

D. StoEKS Algorithm

Given the G_{sts}, C_{sts}, and u_{sts} in moment forms, we can obtain the orthogonal V using the EKS algorithm. The reduced systems can then be obtained by these orthogonal basis V from (14). The reduced system will become

$$\hat{G}_{sts} z(t) + \hat{C}_{sts} \frac{dz(t)}{dt} = \hat{B}_{sts} u_{sts}. \tag{29}$$

Here

$$\hat{G}_{sts} = V^{\mathrm{T}} G_{sts} V \qquad \hat{C}_{sts} = V^{\mathrm{T}} C_{sts} V \qquad \hat{B}_{sts} = V^{\mathrm{T}} B_{sts}. \tag{30}$$

The reduced system can be solved in the time domain by any standard integration algorithm. The solution of the reduced system $z(t)$ can then be projected back to original space by $\tilde{v}(t) = Vz(t)$.

By solving the augmented equation in (21), we can obtain the mean and variance of any node voltage $v(t)$ by

$$E\left(v(t)\right) = E\left(v_0(t) + \sum_{i=1}^{P-1} v_i(t) H_i\right) = v_0$$

$$\mathrm{var}\left(v(t)\right) = \mathrm{var}\left(v_0(t) + \sum_{i=1}^{P-1} v_i(t) H_i\right) = \sum_{i=1}^{P-1} v_i(t)^2 \mathrm{var}(H_i).$$

Algorithms: StoEKS

Input: augmented system G_{sts}, C_{sts}, B_{sts}, u_{sts}
Output: the HPC coefficients of node voltage, v

1 Get the first L moments of u_{sts} for each current source
2 Compute the orthogonal basis of subspace from (22) V
3 Obtain the reduced system matrix from $\hat{G} = V^T G_{sts} V$, $\hat{C} = V^T C_{sts} V$, $\hat{B} = V^T B_{sts}$
4 Solve $\hat{G}z(t) + \hat{C}\frac{dz(t)}{dt} = \hat{B}u_{sts}(t)$
5 Project back to original space to get v(t) = Vz(t)
6 Compute the variational values (means, variance) of the specified nodes

Fig. 3. Proposed StoEKS algorithm.

Furthermore, the distribution of $v(t)$ can also be easily calculated by the characteristic of Hermite PC and the distribution of $\xi_1, \xi_2, \ldots, \xi_N$. Fig. 3 is the StoEKS algorithm for the given G_{sts}, C_{sts}, B_{sts}, and u_{sts}.

E. Walk-Through Example

In the following, we consider a simple case where we only have three independent variables to illustrate the method. We assume that there are three independent variables ξ_g, ξ_c, and ξ_I associated with matrices G and C and input sources, respectively, in the circuit.

We assume that the variational component in (3) $u_v(t, \xi_I)$ follows the lognormal distribution as

$$u_v(t, \xi_I) = e^{g(t,\xi_I)} \qquad g(t, \xi) = \mu_I(t) + \sigma_I(t)\xi_I. \tag{31}$$

Then, (2) becomes

$$G(\xi_g)v(t) + C(\xi_c)\frac{dv(t)}{dt} = Bu(t, \xi_I). \tag{32}$$

The variation in width W and thickness T will cause variation in conductance matrix G and storage matrix C, while variation in threshold voltage will cause variation in leakage currents $u(t, \xi_I)$. Thus, the resulting system can be written as [10]

$$G(\xi_g) = G_0 + G_1\xi_g \qquad C(\xi_c) = C_0 + C_1\xi_c. \tag{33}$$

G_0 and C_0 represent the deterministic components of conductance and capacitance of the wires, respectively. G_1 and C_1 represent the sensitivity matrices of the conductance and capacitance, respectively. ξ_g and ξ_c are the random variables with normalized Gaussian distribution, representing process variations in wires of conductance and capacitor, respectively.

ξ_I is a normalized Gaussian distribution random variable representing variation in threshold voltage.

Using Galerkin method as in [16] with second-order Hermite PCs, we end up solving the following:

$$G_{sts}v(t) + C_{sts}\frac{dv(t)}{dt} = B_{sts}u_{sts}(t) \tag{34}$$

where

$$G_{sts} = \begin{bmatrix} G_0 & G_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ G_1 & G_0 & 0 & 0 & 2G_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_0 & 0 & 0 & 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_0 & 0 & 0 & 0 & 0 & G_1 & 0 \\ 0 & G_1 & 0 & 0 & G_0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 & 0 & 0 & 0 & G_0 & 0 & 0 \\ 0 & 0 & 0 & G_1 & 0 & 0 & 0 & 0 & G_0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_0 \end{bmatrix}$$

$$C_{sts} = \begin{bmatrix} C_0 & 0 & C_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_0 & 0 & 0 & 0 & 0 & 0 & C_1 & 0 & 0 \\ C_1 & 0 & C_0 & 0 & 0 & 2C_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_0 & 0 & 0 & 0 & 0 & 0 & C_1 \\ 0 & 0 & 0 & 0 & C_0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 & C_0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & C_0 & 0 & 0 & 0 \\ 0 & C_1 & 0 & 0 & 0 & 0 & 0 & C_0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_0 & 0 \\ 0 & 0 & 0 & C_1 & 0 & 0 & 0 & 0 & 0 & C_0 \end{bmatrix}$$

$$u_{sts}(t) = [u_0(t) + u_d(t), 0, 0, u_3(t), 0, 0, u_6(t), 0, 0, 0]^{\mathrm{T}}.$$

One observation we have is that, although the augmented circuit matrices are much bigger than before, they are very sparse and also consist of repeated coefficient matrices from the HPC. As a result, the reduction techniques can significantly improve the simulation efficiency.

F. Computational Complexity Analysis

In this section, we analyze the computing costs for both StoEKS and HPC methods and show the theoretical advantage of StoEKS over the nonreduction-based HPC method.

First, if the PCA operation is performed, which essentially uses singular value decomposition on the covariance matrix, its computation cost is $O(ln^2)$. Here, l is the number of original correlated random variables, and n is the first n dominant singular values, which is also the number of independent random variables after PCA. Since the random variable l is typically much smaller than the circuit size, the running time of PCA is not significant for the total cost.

After we transform the original circuit matrices into the augmented circuit matrices in (21), which are still very sparse, the matrix sizes grow from $m \times m$ to $Pm \times Pm$, where P is the number of Hermite polynomials used. The number is dependent on the Hermite polynomial order and the number of variable used, as shown in (5).

Typically, solving an $n \times n$ linear matrix takes $O(n^\alpha)$ (typically, $1 \leq \alpha \leq 1.2$ for sparse circuits), and matrix factorizations take $O(n^\beta)$ (typically, $1.1 \leq \beta \leq 1.5$ for sparse circuits). For HPC, assuming that we need to compute w time steps in transient analysis (taking w forward and backward substitutions after one LU decomposition), the computing cost is then

$$O\left(w(mP)^\alpha + (mP)^\beta\right). \tag{35}$$

while for StoEKS, we only need to approximately take q, which is the order of the reduced model, steps (after the one LU decomposition) to compute the projection matrix V. Thus, the total computational cost is

$$O\left(q(mP)^{\alpha}+(mP)^{\beta}+mPq^2+q^3+wq^2\right) \tag{36}$$

without considering the cost of the PCA operations $(\ln^2)$ as we did not perform the PCA in our experiments. The last three items are the costs of performing the reductions (QR operation) and transient simulation of the reduced circuit (which have very dense matrices) in time domain. Since $q \ll w$, the computing cost of StoEKS can be significantly lower than HPC. Moreover, the proposed method can be further improved by using the hierarchical EKS method [3].

V. Experimental Results

This section describes the simulation results of circuits with both the capacitance and conductance variation and the leakage current variation. The leakage current variation follows log-normal distribution. The capacitance and conductance variation follows Gaussian distribution.

All the proposed methods have been implemented in Matlab 7.0. All the experimental results are carried out on a Dell PowerEdge 1900 workstation (using a Linux system) with Intel Quadcore Xeon CPUs with 2.99 GHz and 16-GB memory. To solve large circuits in Matlab, an external linear solver package UMFPACK [1] has been used, which is linked with Matlab using Matlab mexFunction.

As mentioned in Section II-B, we assume that the random variables used in this paper for G and C and current sources are independent after the PCA transformation.

First, we assume a time-variant leakage model, in which we assume that $u_v^i(t,\xi)$ in (24) is a function of time t and further assume that $g_j(t)$, which is the standard deviation (s.d.), is a fixed percentage, for example, 10%, of $v_d(t)$ in (3), i.e., $g_i(t)=0.1u_{di}(t)$, where $u_{di}(t)$ is the ith component of the PWL current $v_d(t)$.

Figs. 4–6 show the results at one particular node under this configuration.

Fig. 4 shows the node voltage distribution at one node of a ground network with 280 nodes, considering variation in conductance, capacitance, and leakage current (with three random variables). The s.d. of the lognormal current sources with one Gaussian variable is $0.1u_{di}(t)$. The s.d. values in conductance and capacitance are also 0.1 of the mean. The mean and s.d. are computed by the Hermite PC method; Hermite PC with EKS are also marked in the figure, which fit very well with the MC results. In Fig. 4, the dotted lines are the mean and s.d. calculated by MC. The solid lines are the mean and s.d. by the algorithm [15], which is named as HPC. The dashed line is the results from the new StoEKS. The MC results are obtained by 3000 samples. The reduced order for EKS is five, $q=5$.

Fig. 5 shows the distribution at one node of a ground network with 2640 nodes. The parameter $g_i(t)$ value is set to the same

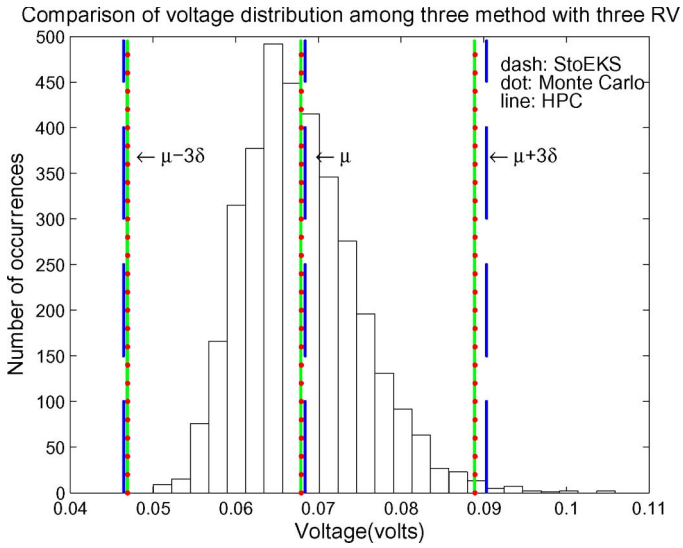


Fig. 4. Distribution of the voltage variations in a given node by StoEKS, HPC, and MC of a circuit with 280 nodes with three random variables. $g_i(t)=0.1\,u_{di}(t)$.

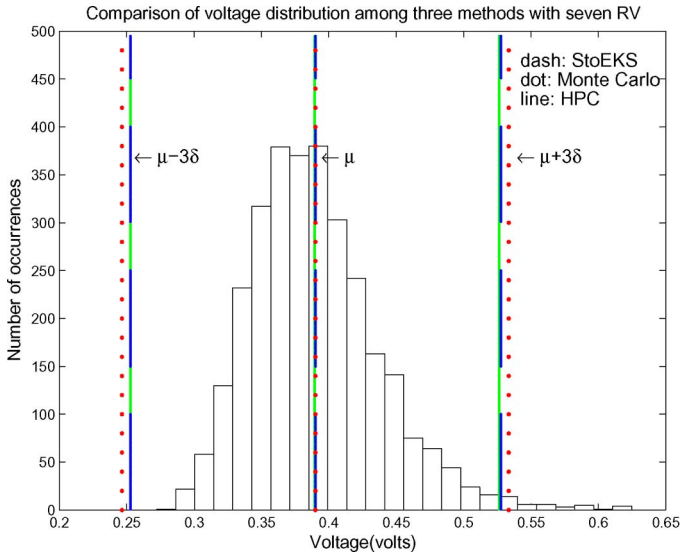


Fig. 5. Distribution of the voltage variations in a given node by StoEKS, HPC, and MC of a circuit with 2640 nodes with seven random variables. $g_i(t)=0.1\,u_{di}(t)$.

as the ones in the circuit with 280 nodes. The s.d. values in conductance are 0.02, 0.05, and 0.1 of the mean for three variables. The s.d. values in capacitance are 0.02, 0.02, and 0.1 of the mean for three variables. There are totally seven random variables. The dotted lines represent the MC results. Moreover, the dashed lines represent the results given by StoEKS. From these two figures, we can only see marginal difference between the three different methods. The reduced order for EKS is also five, $q=5$.

Fig. 6 shows the distribution at one node of a ground network with 280 nodes. However, the variation setting of parameters is different. The standard divisions in conductance are set to 0.02, 0.02, 0.03, 0.05, and 0.05 of the mean for five variables, respectively, i.e., their a_1's in (15) are set to those values. The standard divisions in capacitances are set to 0.02, 0.03, 0.04,

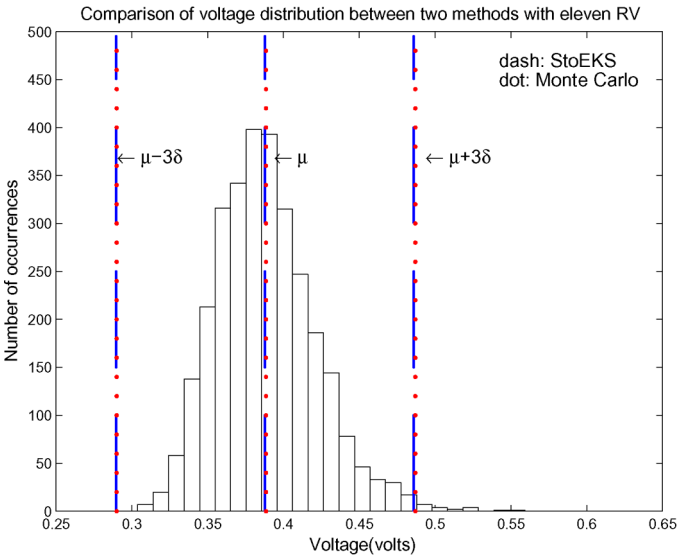


Fig. 6. Distribution of the voltage variations in a given node by StoEKS and MC of a circuit with 2640 nodes with 11 random variables. $g_i(t) = 0.1\, u_{di}(t)$.

TABLE I
CPU TIME COMPARISON OF STOEKS AND HPC WITH THE MC METHOD. $g_i(t) = 0.1\, u_{di}(t)$

#nodes	#RV	MC	StoEKS	speedup	HPC [15]	speedup
280	3	694.35	0.3	2314.5	2.37	292.97
280	7	671.46	2.37	283.31	227.94	2.94
280	11	684.88	24.26	28.23	914.34	0.74
2640	3	5925.7	4.33	1368.5	55.35	107.1
2640	7	5927.6	25.02	236.9	1952.2	3.04
2640	11	6042.2	693.27	8.72	–	–
12300	3	3.54×10^4	21.62	1637.4	298.84	118.5
12300	7	3.30×10^4	151.71	217.65	–	–
119600	3	–	258.21	–	–	–
119600	7	–	2074.8	–	–	–
1078800	3	–	1830.4	–	–	–

0.05, and 0.05 of the mean for five variables, respectively, also. The standard deviation of the lognormal current sources is 0.1 of the mean. There are 11 random variables in all. It is even harder for HPC to compute the mean and s.d. of the circuit. The dotted lines represent the MC results. Moreover, the dashed lines represent the results given by StoEKS. The reduced order for EKS is ten.

Table I shows the speedup of the StoEKS and HPC methods over MC method under different numbers of random variables. In the table, *#RV* is the number of random variables used. In the table, there are 3, 7, and 11 random variables. The variation value setup of three random variables is the same as the circuit used in Fig. 4. The variation value setup of seven random variables is the same as the circuit used in Fig. 5. The variation value setup of 11 random variables is the same as the circuit used in Fig. 6. The first *speedup* is the speedup of StoEKS over MC, and the second *speedup* is the speedup of StoEKS over HPC.

From the table, we observe that we cannot obtain the results from HPC or MC when the circuit becomes large enough in reasonable time. Meanwhile, StoEKS can deliver all the results.

We remark that the intradie variations are typically very spatially correlated [4]. After the transformation like PCA, the number of variables can be significantly reduced. As a result, in our examples, we do not assume large number of variables.

TABLE II
ACCURACY COMPARISON OF DIFFERENT METHODS—STOEKS, HPC, AND MC. $g_i(t) = 0.1\, u_{di}(t)$

#nodes	#RV	Mean			Std Dev		
		MC	StoEKS	HPC	MC	StoEKS	HPC
280	3	0.047	0.047	0.047	0.0050	0.0048	0.0048
2640	3	0.39	0.39	0.39	0.048	0.046	0.046
12300	3	1.66	1.66	1.66	0.16	0.17	0.17
280	7	0.047	0.047	0.047	0.0056	0.0055	0.0055
2640	7	0.39	0.39	0.39	0.048	0.046	0.046
12300	7	2.56	2.56	–	0.31	0.30	–
280	11	0.047	0.047	0.047	0.0039	0.0039	0.0040
2640	11	0.39	0.39	–	0.033	0.033	–

TABLE III
ERROR COMPARISON OF STOEKS AND HPC OVER MC METHODS. $g_i(t) = 0.1\, u_{di}(t)$

#nodes	#RV	StoEKS % Error in	HPC % Error in	StoEKS % Error in	HPC % Error in
280	3	0.19	0.28	3.14	3.10
2640	3	1.23	1.05	4.31	4.51
12300	3	0.10	0.08	2.95	2.98
280	7	0.063	0.17	1.12	1.54
2640	7	0.076	0.11	4.18	4.60
12300	7	0.23	–	0.23	–
280	11	0.42	0.21	0.18	0.52
2640	11	0.18	–	0.30	–

Tables II and III show the mean and s.d. comparison of different methods over the MC method for several circuits. Again, *#RV* is the number of random variables used. Table II contains the values we obtain from different methods, and Table III presents the error comparison of *StoEKS* and HPC over MC, respectively. We can see that StoEKS only has marginal difference from MC while it is able to perform simulation on much larger circuit than the existing HPC method on the same platform.

Finally, we use a time-invariant leakage model, in which we assume that $u_v^i(\xi)$ in (24) is not a function of time t and further assume that g_j, which is the standard deviation, is a fixed percentage, of a constant current value in (3). In our test cases, we use the peak current $I_p \approx 41$ mA, as shown in Fig. 7, as the constant value. Fig. 8 shows the results in this configuration.

VI. CONCLUSION

In this paper, we have proposed a fast stochastic method for analyzing the voltage drop variations of on-chip power grid networks. The new method, called *StoEKS*, applies HPC to represent the random variables in both power grid networks and input leakage currents with lognormal distribution. This HPC method transforms a statistical analysis problem into a deterministic analysis problem where increased augmented circuit matrices are created. The augmented circuit matrices consist of the coefficients of Hermite polynomials representing both variational parameters in circuit matrices and input sources. We then applied the EKS method to compute variational responses from the augmented circuit equations.

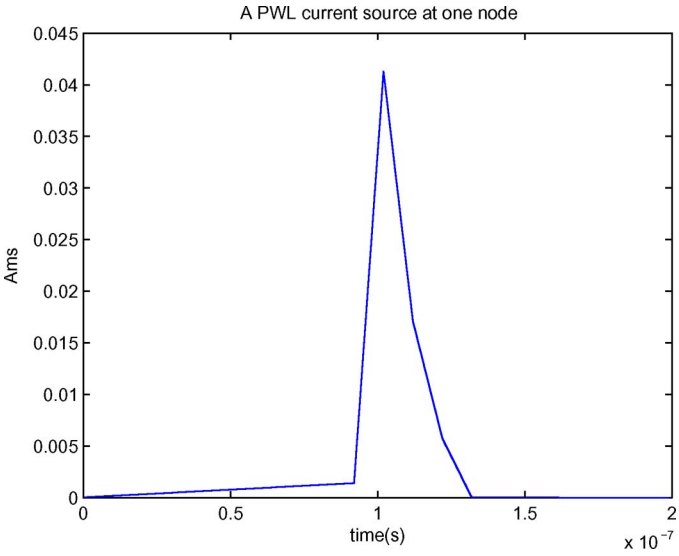


Fig. 7. PWL current source at certain node.

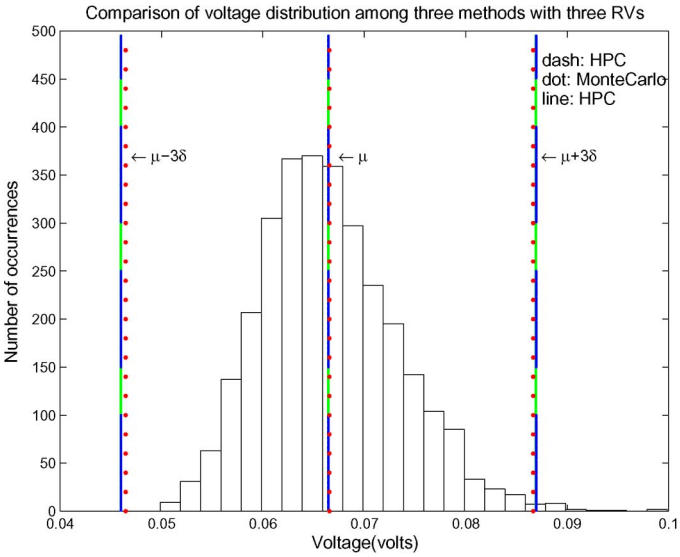


Fig. 8. Distribution of the voltage variations in a given node by StoEKS, HPC, and MC of a circuit with 280 nodes with three random variables using the time-invariant leakage model. $g_i = 0.1\ I_p$.

The proposed method does not require any sampling operations, as used by collocation-based spectral stochastic analysis method. Experimental results have shown that the proposed method is about two-order magnitude faster than the existing Hermite PC-based simulation method and more order of magnitudes faster than MC method with marginal errors. StoEKS also increases the analysis capacity of previous statistical simulation methods based on the spectral stochastic method.

REFERENCES

[1] *Umfpack*. [Online]. Available: http://www.cise.ufl.edu/research/sparse/umfpack/

[2] A. B. Kahng, "DFM tools and methodologies for 65 nm and below," in *Proc. ASPDAC*, 2006. tutorial.

[3] Y. Cao, Y. Lee, T. Chen, and C. C. Chen, "HiPRIME: Hierarchical and passivity reserved interconnect macromodeling engine for RLKC power delivery," in *Proc. DAC*, 2002, pp. 379–384.

[4] C. Chiang and J. Kawa, *Design for Manufacturability*. New York: Springer-Verlag, 2007.

[5] V. De and S. Borkar, "Technology and design challenges for low power and high performance," in *Proc. ISLPED*, Aug. 1999, pp. 163–168.

[6] I. A. Ferzli and F. N. Najm, "Statistical estimation of leakage-induced power grid voltage drop considering within-die process variations," in *Proc. DAC*, 2003, pp. 856–859.

[7] I. A. Ferzli and F. N. Najm, "Statistical verification of power grids considering process-induced leakage current variations," in *Proc. ICCAD*, 2003, pp. 770–777.

[8] R. G. Ghanem and P. D. Spanos, *Stochastic Finite Elements: A Spectral Approach*. New York: Dover, 2003.

[9] P. Ghanta, S. Vrudhula, and S. Bhardwaj, "Stochastic variational analysis of large power grids considering intra-die correlations," in *Proc. DAC*, Jul. 2006, pp. 211–216.

[10] P. Ghanta, S. Vrudhula, R. Panda, and J. Wang, "Stochastic power grid analysis considering process variations," in *Proc. Eur. Design Test Conf. (DATE)*, 2005, vol. 2, pp. 964–969.

[11] Y. S. Kumar, J. Li, C. Talarico, and J. Wang, "A probabilistic collocation method based statistical gate delay model considering process variations and multiple input switching," in *Proc. Eur. Design Test Conf. (DATE)*, 2005, pp. 770–775.

[12] Y. Lee, Y. Cao, T. Chen, J. Wang, and C. Chen, "HiPRIME: Hierarchical and passivity preserved interconnect macromodeling engine for RLKC power delivery," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 6, pp. 797–806, Jun. 2005.

[13] D. Li, S. X.-D. Tan, and B. McGaughy, "ETBR: Extended truncated balanced realization method for on-chip power grid network analysis," in *Proc. Eur. Design Test Conf. (DATE)*, 2008, pp. 432–437.

[14] M. Loeve, *Probability Theory*, 4th ed. New York: Springer-Verlag, 1977.

[15] N. Mi, J. Fan, and S. X.-D. Tan, "Analysis of power grid networks considering lognormal leakage current variations with spatial correlation," in *Proc. IEEE ICCD*, 2006, pp. 56–62.

[16] N. Mi, J. Fan, and S. X.-D. Tan, "Simulation of power grid networks considering wires and lognormal leakage current variations," in *Proc. IEEE Int. Workshop BMAS*, 2006, pp. 73–78.

[17] N. Mi, J. Fan, S. X.-D. Tan, Y. Cai, and X. Hong, "Statistical analysis of on-chip power delivery networks considering lognormal leakage current variations with spatial correlation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 2064–2075, Aug. 2008.

[18] N. Mi, S. X.-D. Tan, P. Liu, J. Cui, Y. Cai, and X. Hong, "Stochastic extended Krylov subspace method for variational analysis of on-chip power grid networks," in *Proc. ICCAD*, 2007, pp. 48–53.

[19] S. Nassif, "Delay variability: Sources, impact and trends," in *Proc. IEEE Int. Solid State Circuits Conf.*, San Francisco, CA, Feb. 2000, pp. 368–369.

[20] S. Nassif, "Design for variability in DSM technologies," in *Proc. ISQED*, San Jose, CA, Mar. 2000, pp. 451–454.

[21] S. Pant, D. Blaauw, V. Zolotov, S. Sundareswaran, and R. Panda, "A stochastic approach to power grid analysis," in *Proc. DAC*, 2004, pp. 171–176.

[22] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 9, no. 4, pp. 352–366, Apr. 1990.

[23] R. Rao, A. Srivastava, D. Blaauw, and D. Sylvester, "Statistical analysis of subthreshold leakage current for VLSI circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 2, pp. 131–139, Feb. 2004.

[24] A. Srivastava, R. Bai, D. Blaauw, and D. Sylvester, "Modeling and analysis of leakage power considering within-die process variations," in *Proc. ISLPED*, Aug. 2002, pp. 64–67.

[25] S. X.-D. Tan and L. He, *Aanced Model Order Reduction Techniques in VLSI Design*. Cambridge, U.K.: Cambridge Univ. Press, 2007.

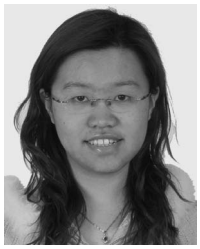
[26] J. Wang, P. Ghanta, and S. Vrudhula, "Stochastic analysis of interconnect performance in the presence of process variations," in *Proc. ICCAD*, Nov. 2004, pp. 880–886.

[27] J. M. Wang and T. V. Nguyen, "Extended Krylov subspace method for reduced order analysis of linear circuits with multiple sources," in *Proc. DAC*, 2000, pp. 247–252.

[28] T. W. Williams, "EDA to the rescue of the silicon roadmap," in *Proc. ISQED*, Mar. 2007, pp. 115–118. keynote speech.

[29] D. Xiu and G. Karniadakis, "Modeling uncertainty in flow simulations via generalized polynomial chaos," *J. Comput. Phys.*, vol. 187, no. 1, pp. 137–167, May 2003.

[30] Y. Zou, Y. Cai, Q. Zhou, X. Hong, S. Tan, and L. Kang, "Practical implementation of stochastic parameterized model order reduction via Hermite polynomial chaos," in *Proc. ASPDAC*, 2007, pp. 367–372.



Ning Mi (S'05) received the B.S. degree in electrical engineering from the Peking University, Beijing, China, in 2005 and the M.S. degree in electrical engineering from the University of California, Riverside, in 2007, where she is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical Engineering.

Her research interests include power grid analysis and model order reduction considering process variations.

Sheldon X.-D. Tan (S'96–M'99–SM'06) received the B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical and computer engineering from The University of Iowa, Iowa City, in 1999.

He is an Associate Professor with the Department of Electrical Engineering, University of California, Riverside. He was a Faculty Member with the Electrical Engineering Department, Fudan University, from 1995 to 1996. He also coauthored the book "Symbolic Analysis and Reduction of VLSI Circuits" (Springer/Kluwer, 2005). His research interests include modeling and simulation of analog/RF/mixed-signal and interconnect circuits, analysis and optimization of high performance power and clock distribution networks, architecture level thermal, power, modeling, and simulation for multicore microprocessors and embedded system designs based on FPGA platforms.

Dr. Tan was the recipient of National Science Foundation (NSF) CAREER Award in 2004. He received a Best Paper Award from the 2007 International Conference on Computer Design, Best Paper Award Nomination from the 2005 IEEE/Association for Computing Machinery (ACM) Design Automation Conference, the Best Paper Award from the 1999 IEEE/ACM Design Automation Conference, and the Best Poster Award from the 1999 Spring Meeting of the NSF Center for Design of Analog and Digital Integrated Circuits. He is an Associate Editor for the *Journal of VLSI Design* and served as a technical program committee member for the ACM/IEEE Asia and South Pacific Design Automation Conference, IEEE International Behavioral Modeling and Simulation Conference, IEEE International Symposium on Quality Electronic Design, and International Conference on Computer-Aided Design.

Yici Cai (M'05) received the B.S. degree in electronic engineering and the M.S. degree in computer science and technology from Tsinghua University, Beijing, China, in 1983 and 1986, respectively, and the Ph.D. degree in computer science from the University of Science and Technology of China, Hefei, China, in 2007.

She has been a Professor with the Department of Computer Science and Technology, Tsinghua University. Her research interests include physical design automation for very large scale integration integrated circuits algorithms and theory, interconnection planning and optimization, and low-power physical design.

Xianlong Hong (F'04) received the B.S. degree in computational mathematics from Tsinghua University, Beijing, China, in 1964.

Since 1964, he has been with Tsinghua University, where he is currently a Professor in the Department of Computer Science and Technology. He was a Visiting Scholar in the University of California, Berkeley, from 1991 to 1992 and in the University of Californina, Los Angeles, in 1995. As a Technical Leader, he organized and managed to develop three generations of very large scale integration computer-aided design (VLSI CAD) system, which are the national projects in China from 1981 to 1991. His research interest is physical design for VLSI circuits. He has authored and coauthored over 200 papers and five books around his area.

Prof. Hong served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and the Technical Program Committee Cochair of Asia and South Pacific Design Automation Conference in 1999–2004 and 2005. Due to his contribution in developing VLSI CAD systems, he was awarded more than 15 Science and Technology Achievement Prizes from the Science and Technology Ministry and Education Ministry of China.