2025 21st International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuits Design (SMACD) | 979-8-3315-2395-4/25/$31.00 ©2025 IEEE | DOI: 10.1109/SMACD65553.2025.11092195

EMSpice 2.1: A Coupled EM and IR Drop Analysis Tool with Joule Heating and Thermal Map Integration for VLSI Reliability

Subed Lamichhane[1], Haotian Lu[1] and Sheldon X.-D. Tan[1]
[1]Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521
slami002@ucr.edu, hlu123@ucr.edu, stan@ece.ucr.edu

***Abstract*—Electromigration (EM) remains a critical reliability concern in current and future copper-based VLSI circuits. As technology scales down, EM-induced IR drop becomes increasingly severe. While several EM-aware IR drop analysis tools have been proposed, few incorporate the real impact of temperature distribution on both EM and IR drop effects. In this work, we introduce *EMSpice 2.1*, an enhanced tool built upon the existing coupled IR-EM analysis framework, EMSpice 2.0, for EM-aware IR drop analysis. For the first time, *EMSpice 2.1* uniquely integrates Joule heating effects and practical thermal maps derived from actual chip conditions. Additionally, it features improved interoperability with commercial EDA tools, facilitating more comprehensive EM and IR drop sign-off analysis. Our findings demonstrate that specific hotspot patterns significantly impact the lifetime of interconnects and overall chip reliability due to EM failures. Furthermore, our tool exhibits strong agreement with industry-standard tools such as COMSOL, achieving a speedup of over 200× while maintaining high accuracy.**

***Index Terms*—Electromigration, Full-Chip, Thermal-Aware**

I. Introduction

For nanometer VLSI chips with copper-based interconnects, increasing current density and shrinking interconnect dimensions, exacerbate reliability concerns related to electromigration (EM)-induced aging and failure. As technology advances, EM sign-off becomes essential steps to ensure the long-term reliability of integrated circuits. Therefore, the development of an accurate and efficient EM analysis tool is crucial for modern semiconductor design and verification.

The current EM models, such as those proposed by Black [1] and Blech [2], are facing criticism for being overly cautious and performing inadequately at the level of individual wire segments. Korhonen et al. [3] introduced a set of physics-based partial differential equations (PDEs) designed to compute the stress in each interconnect wire segment. Various analytical and numerical methods have been developed to solve Korhonen's equations for assessing EM-induced failures. Cook et al. [4] suggested a numerical approach, *FastEM*, based on the finite difference method (FDM). This method initially discretizes the PDE into linear time-invariant ordinary differential equations (ODEs) and then employs Krylov subspace-based reduction techniques to accelerate the computations. Furthermore, Chen et al. [5] offered an analytical solution to the PDE, providing insights into the stress evolution within interconnect structures.

This work is supported in part by NSF grant under No.CCF-2007135 and in part by NSF grant CCF-2305437.

Most existing analytical and numerical solutions overlook the impact of spatial temperature gradients. Recent research highlighted in [6] suggests that thermomigration (TM) effects can rival those of electromigration. With advancements in technology leading to increased power density, greater Joule heating, and higher thermal resistances, these challenges are expected to intensify [7]. To mitigate these issues, Kavousi et al. [7] proposed an EM stress analysis method that incorporates the effects of thermomigration. However, this method assumes uniform boundary temperatures across all wires when calculating temperature distribution, which does not reflect the varied spatial temperatures found in actual chip operations.

In this paper, we introduce a full-chip TM-aware EM failure analysis tool designed for integrated physics-based EM-TM and electronic analysis. Our tool processes power grid netlists from the Synopsys ICC flow, delivering outcomes such as failed EM wires, their resistance changes, and the resultant IR drops in power grids over specified aging periods, considering Joule heating effects. A key innovation in *EMSpice 2.1* is its ability to incorporate actual spatial temperature distributions across the chip into our evaluations.

The novel contributions of this work include:

- Integration with standard EDA tools, allowing the use of standard post-layout parasitic extraction files to supply electrical and geometric layout information to the tool.
- Unlike other temperature-aware methods, our tool uniquely reads and utilizes the spatial temperature distribution of the chip, enabling more accurate temperature considerations for immortality filtering, Thermomigration assessments, and lifetime predictions.
- The tool offers a comprehensive array of User Interfaces (UIs)—including a Command Line Interface (CLI), a Graphical User Interface (GUI), and remote online portal—providing users with versatile options to input data and receive EM analysis results in interactive visual formats.

Authorized licensed use limited to: Univ of Calif Riverside. Downloaded on June 24,2026 at 00:51:45 UTC from IEEE Xplore. Restrictions apply.

II. Conceptual Review

EM occurs from the ongoing interactions between metal atoms and conducting electrons in power grids, leading to atom migration and resulting in tensile and compressive stresses at cathode and anode nodes. This can cause voids and hillocks that potentially lead to wire failures due to increased resistance or open circuits. Initially, the nucleation phase sees the formation of voids, followed by the post-voiding phase. Primarily, electromigration (EM), stress migration (SM), and thermomigration (TM) are key forces altering metal atom concentrations, heavily influenced by thermal effects [8], [9].

A. Temperature modeling

Starting with the first law of thermodynamics, as characterized by [10], we can derive the stationary condition temperature distribution on a VLSI interconnect segment as [11]:

$$k_{cu}\nabla^2 T - (Q_{jh} + Q_{conv}) = 0 \tag{1}$$

Here, $Q_{jh} = j^2 \cdot \rho$ is the contribution from the Joule heating effect where j is the current density in the interconnect and ρ denotes resistivity of the metal wire. $Q_{conv} = k_{cu}(T - T_0)/\Gamma^2$ is the heat convection component, where k_{cu} represents the thermal conductivity of metal wire, and Γ is the thermal characteristic length influenced by the geometry and topology of the environment which can be estimated as described in [8]:

$$\Gamma^2 = t_{cu} t_{ILD} \frac{k_{cu}}{k_{ILD}} \tag{2}$$

Where t_{cu} refers to the thickness of wire, while t_{ILD} and k_{ILD} represent the thickness and conductivity of the dielectric.

Eq. (1) can be resolved numerically through methods like FDM and FEM to obtain the spatial temperature distribution. Additionally, the temperature profile for a single wire, subject to boundary conditions $T(-L/2) = T_1$ and $T(+L/2) = T_2$, can be approximated as described in [8], [9]:

$$T(x) = T_0 + T_m \left[1 - \frac{cosh\left(\frac{x}{\Gamma}\right)}{cosh\left(\frac{L}{2\Gamma}\right)}\right] + T_n \left[\frac{sinh\left(\frac{x}{\Gamma}\right)}{sinh\left(\frac{L}{2\Gamma}\right)}\right] \tag{3}$$

where $T_0 = (T_1 + T_2)/2$, $T_m = \rho \cdot j^2 \cdot \Gamma^2 / k_{Cu}$ and $T_n = (T_1 - T_2)/2$. Existing methods use fixed values for T_1 and T_2 in temperature calculations, diverging from real-world conditions [7], [11] that T_1 and T_2 may vary with time and are non-identical from wire to wire. In contrast, *EMSpice 2.1* derives T_1 and T_2 from actual temperature data, allowing for accurate $T(x)$ calculations for each interconnect segment using Eq. (3).

B. Temperature-aware immortal wires filtering

During the nucleation phase of EM, if the steady-state stress at the cathode node (σ_{steady}) remains below the critical threshold (σ_{critical}), the interconnect tree is considered immortal. To assess immortality considering temperature effects, a voltage-based check is employed, as outlined by Sun and Demircan [12] and Sun and Cook [13]. This work has been extended to consider the Joule heating in [7], which will be used in this work. The only difference is that we will consider both Joule heating and given initial thermal distributions at the same time.

C. Coupled multiphysics analysis

The electromigration (EM) stress, σ, accounting for electromigration (EM), stress migration (SM), and thermomigration (TM), is described by Korhonen's equation [14]:

$$\text{PDE: } \frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa(x)\left(\frac{\partial \sigma}{\partial x} - S - M\right)\right], \quad t > 0 \tag{4}$$

$$\text{BC: } \kappa(x_b)\left(\left.\frac{\partial \sigma}{\partial x}\right|_{x=xb} - S - M\right) = 0, \quad 0 < t < t_{\text{nuc}} \tag{5}$$

$$\text{IC: } \sigma(x, 0) = \sigma_T \tag{6}$$

Here, $S = \frac{eZ\rho j}{\Omega}$ denotes the EM flux, and $M = \frac{Q}{\Omega T}\frac{\partial T}{\partial x}$ represents the TM flux. The position-dependent diffusivity is described by $\kappa(x) = D_a(T(x))B\Omega/(k_b T(x))$, influenced by non-uniform temperature distributions. $D_a = D_0 \exp(-E_a k_b T(x)))$ is the atomic diffusion coefficient, with D_0 as a constant and E_a as the activation energy. Additionally, σ_T is the initial thermally induced residual stress, and x_b marks the block terminals.

Korhonen's equation (Eq. (4)), incorporating electromigration (EM), stress migration (SM), and thermomigration (TM), is solved using the Finite Difference Time Domain (FDTD) method. This method analyzes stress over time in each multi-segment interconnect tree by transforming the differential equation, along with its boundary conditions (BCs) and initial conditions (ICs), into a linear time-invariant (LTI) system:

$$\begin{aligned} C\dot{\sigma}(t) &= A\sigma(t) + Bj(t) - D \\ \sigma(0) &= [\sigma_1(0), \sigma_2(0), \ldots, \sigma_n(0)] \end{aligned} \tag{7}$$

In this model, $\sigma(t)$ is the stress vector, with C and A as $n \times n$ matrices. D is an $n \times 1$ matrix for thermomigration (TM) effects, and B is an $n \times p$ input matrix. A Krylov subspace method solves the ordinary differential equation (ODE) for stress evolution in a linear time-invariant (LTI) system, starting from initial stress $\sigma(0)$, which includes residual and previously computed stresses. The coupled EM-TM-IR drop equations addressed in this paper are structured as follows:

$$\begin{aligned} & C\dot{\sigma}(t) = A\sigma(t) + Bj(t) - D \\ & V_v(t) = \int_{\Omega_L} \frac{\sigma(t)}{B} dV \\ & G(t) \times u(t) = Pj(t) \\ & \sigma(0) = [\sigma_1(0), \sigma_2(0), \ldots, \sigma_n(0)] \end{aligned} \tag{8}$$

$V_v(t)$ estimates the void volume within a wire, Ω_L is the volume of the remaining wire, and V is the wire's total volume. For IR drop calculations, a resistance network is derived from the power grid, and Modified Nodal Analysis (MNA) is used, detailed in Eq. (8). $G(t)$, the admittance matrix, changes over time with the wire resistance, influenced by electromigration (EM) and thermomigration (TM).

For the post-voiding phase, the PDE is identical to the nucleation phase, using the stress at $t = t_{nuc}$ as the IC. The BC at the void nucleation site is defined as follows:

$$\left.\frac{\partial \sigma}{\partial x}\right|_{x=x_{\text{nuc}}} = \frac{\sigma(x_{\text{nuc}}, t)}{\delta}, \quad t_{\text{nuc}} < t < \infty \tag{9}$$

Authorized licensed use limited to: Univ of Calif Riverside. Downloaded on June 24,2026 at 00:51:45 UTC from IEEE Xplore. Restrictions apply.

Here, x_{nuc} indicates the void nucleation site, and δ is surface thickness. An LTI ODE system, similar to Eq. (8), is set up with this BC for the post-voiding phase.

During the post-voiding phase, as voids exceed the critical volume V_{crit}, wire resistance increases, affecting current density across the more resistive T_a/T_aN barrier. This resistance change is approximated in [15],

$$\Delta R(t) = \frac{V_\nu - V_{crit}}{WH}\left[\frac{\rho_{T_a}}{h_{T_a}(2H+W)} - \frac{\rho_{C_u}}{HW}\right] \quad (10)$$

where W denotes the wire width, H and h_{Ta} represents copper thickness and barrier layer thickness, respectively. ρ_{Cu} and ρ_{Ta} mark the resistivity of copper and T_a/T_aN barrier, respectively. During FDTD EM-TM simulations, $\Delta R(t)$ is recalculated at each timestep, along with current distribution, to reflect changes in resistance due to void growth.

III. EMSpice 2.1 Algorithm Flow

EMSpice 2.1 integrates with standard EDA tools like Synopsys and Cadence, as outlined in Fig. 1. The process begins with design layout and parasitic extraction using these tools. *EMSpice 2.1* inputs the layout files and a parameters file detailing simulation time and material properties. Uniquely, it also accepts real temperature distribution files.

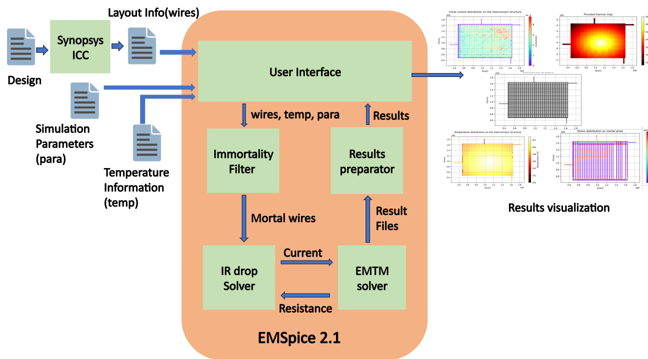


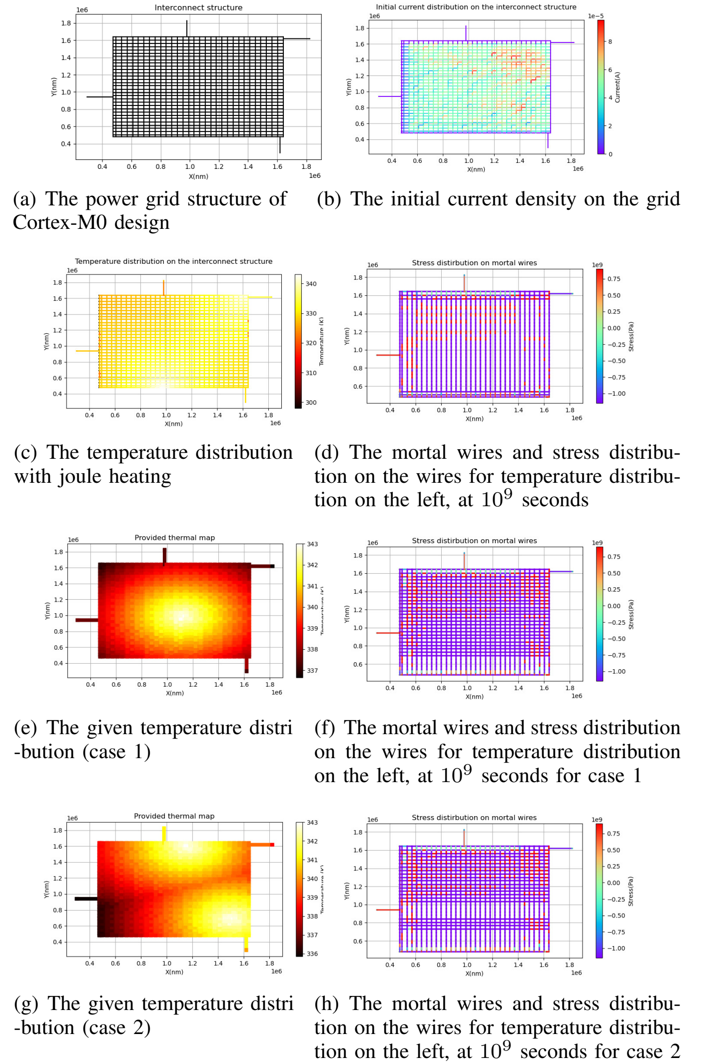
Fig. 1. Overall framework of the proposed method

This tool offers three user interfaces (UI): a Command Line Interface (CLI), a Graphical User Interface (GUI), and an online portal for remote access without installation. Users input files through these UIs, which are then parsed to extract initial resistance, current information of the nets, initial temperature distribution, and simulation parameters, serving all other tool modules.

Techniques from Section II filter out immortal trees that are impervious to electromigration effects. Mortal wires then proceed to the coupled FDTD-based EM-TM and linear network IR-drop solver, as detailed in Fig. 1. This solver updates resistances based on time-dependent current densities affected by EM-TM effects. Simulation parameters like total time and step size are set in a user-provided parameters file. Post-simulation, the EM-TM solver outputs stress distributions and void locations in accessible formats. These results are processed for interactive visualization through the tool's UIs, as shown in Fig. 1.

IV. Numerical Results and Discussions

In this section, we present the numerical results from the proposed tool *EMSpice 2.1* and examine temperature gradients' impact on interconnect mortality and lifetime of the chips. We use the *Cortex-M0* power grid, depicted in Fig. 2, as a case study.



(a) The power grid structure of Cortex-M0 design

(b) The initial current density on the grid

(c) The temperature distribution with joule heating

(d) The mortal wires and stress distribution on the wires for temperature distribution on the left, at 10^9 seconds

(e) The given temperature distri -bution (case 1)

(f) The mortal wires and stress distribution on the wires for temperature distribution on the left, at 10^9 seconds for case 1

(g) The given temperature distri -bution (case 2)

(h) The mortal wires and stress distribution on the wires for temperature distribution on the left, at 10^9 seconds for case 2

Fig. 2. The existing temperature map impacts on EM of power grid of Cortex-M0 design

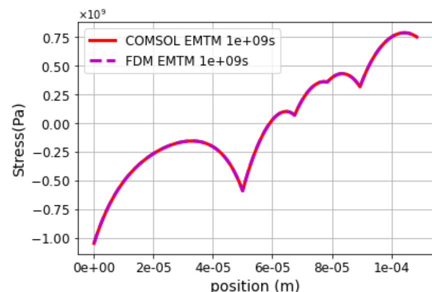
Fig. 2(a) shows the design's power grid structure with 68 trees across two metal layers, averaging 31 segments per tree. Fig. 2(b) displays the initial current distribution. Fig. 2(c) depicts the temperature distribution, considering only internal Joule heating and an ambient temperature equal to the averages in Fig. 2(e) and Fig. 2(g).

Fig. 2(d) shows mortal wires and stress distribution at 1×10^9 seconds, identifying 41 mortal wires out of 68. Temperature-aware filtering omits immortal wires, as discussed in Section II. We evaluated power grid lifetimes under various temperature scenarios using $TTF = t_{life} = t_{nuc} + t_{inc} + t_{growth}$, following [15]. The lifetime was found to be approximately 5×10^8 seconds, or about 16 years.

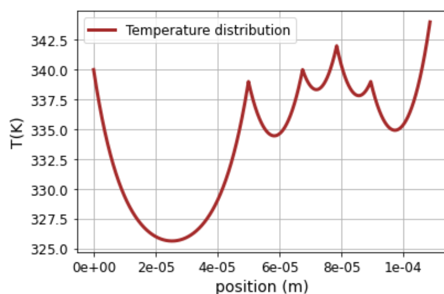
Authorized licensed use limited to: Univ of Calif Riverside. Downloaded on June 24,2026 at 00:51:45 UTC from IEEE Xplore. Restrictions apply.

Fig. 2(e) presents a thermal map case 1 with a distinct temperature gradient, leading to 58 mortal wires and a reduced lifetime of 3.8×10^8 seconds, or roughly 12 years. Fig. 2(g) and Fig. 2(h) show another temperature map case 2 and its impact on 51 mortal wires, with an average lifetime of about 4.4×10^8 seconds, or 14 years.

To assess the accuracy of our EM-TM stress solver, we analyzed 20 randomly selected trees from the *Cortex-M0* power grid using COMSOL. The stress results from our temperature-aware FDM approach showed strong correlation with those from COMSOL [16], as shown in Fig. 3. We featured a five-segment tree from *Cortex-M0* for clear illustration. Fig. 3(b) displays the temperature distribution within this tree. Stress levels ranged from -1.1×10^9 Pa to 0.8×10^9 Pa. The RMSE for our method against COMSOL was 3.42×10^7, demonstrating an average error of only about 1.8%.



(a) Comparison of stress distribution result from the proposed method against COMSOL



(b) Temperature distribution used in the above stress calculation

Fig. 3. Stress result comparison and temperature distribution used for the stress

To further evaluate the performance of our method, we analyzed 20 randomly selected interconnect trees with 33 branches on average from the *Cortex-M0* power grids using COMSOL. Our tool derived accurate solution in an averaged 1.6 seconds per tree, while COMSOL took about 315 seconds on the same task. This shows our efficient FDTD-based method achieves more than $200\times$ speedup over the FEM-based COMSOL.

V. Conclusions

In this paper, we introduced *EMSpice 2.1*, a coupled EM-aware IR drop analysis tool that, ***for the first time***, accounts for both electromigration (EM) and thermomigration (TM) by incorporating actual spatial temperature distributions. The tool uniquely integrates Joule heating effects and practical thermal maps derived from real chip conditions, enhancing accuracy in EM and IR drop analysis. Additionally, *EMSpice 2.1* offers improved interoperability with commercial EDA tools, enabling more comprehensive sign-off analysis. Our results show that specific hotspot patterns significantly affect interconnect lifetime and overall chip reliability due to EM failures. Moreover, our tool demonstrates strong agreement with industry-standard tools such as COMSOL while achieving over $200\times$ speedup without compromising accuracy.

References

[1] J. R. Black, "Electromigration—a brief survey and some recent results," *IEEE Transactions on Electron Devices*, vol. 16, no. 4, pp. 338–347, 1969.

[2] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *Journal of Applied Physics*, vol. 47, no. 4, pp. 1203–1208, 1976.

[3] M. A. Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li, "Stress evolution due to electromigration in confined metal lines," *Journal of Applied Physics*, vol. 73, no. 8, pp. 3790–3799, 1993.

[4] C. Cook, Z. Sun, E. Demircan, M. D. Shroff, and S. X.-D. Tan, "Fast electromigration stress evolution analysis for interconnect trees using krylov subspace method," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 5, pp. 969–980, 2018.

[5] H.-B. Chen, S. X.-D. Tan, X. Huang, T. Kim, and V. Sukharev, "Analytical modeling and characterization of electromigration effects for multibranch interconnect trees," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 11, pp. 1811–1824, 2016.

[6] L. Chen, S. X.-D. Tan, Z. Sun, S. Peng, M. Tang, and J. Mao, "A fast semi-analytic approach for combined electromigration and thermomigration analysis for general multisegment interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 2, pp. 350–363, 2021.

[7] M. Kavousi, L. Chen, and S. X.-D. Tan, "Fast electromigration stress analysis considering spatial joule heating effects," in *2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 208–213, 2022.

[8] A. Abbasinasab and M. Marek-Sadowska, "Rain: A tool for reliability assessment of interconnect networks—physics to software," in *Proceedings of the 55th Annual Design Automation Conference*, pp. 133:1–133:6, 2018.

[9] M. Kavousi, L. Chen, and S. X.-D. Tan, "Electromigration immortality check considering joule heating effect for multisegment wires," in *2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, pp. 1–8, 2020.

[10] H. S. Carslaw and J. C. Jaeger, *Conduction of heat in solids, 2nd ed.* Oxford: Oxford University Press, 1959.

[11] S. Lamichhane, M. Kavousi, and S. X.-D. Tan, "Emspice 2.0: Multi-physics electromigration analysis tool for beyond moore ics," in *2024 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 571–576, 2024.

[12] Z. Sun, E. Demircan, M. D. Shroff, T. Kim, X. Huang, and S. X.-D. Tan, "Voltage-based electromigration immortality check for general multi-branch interconnects," in *2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 1–7, 2016.

[13] Z. Sun, E. Demircan, M. D. Shroff, C. Cook, and S. X.-D. Tan, "Fast electromigration immortality analysis for multisegment copper interconnect wires," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3137–3150, 2018.

[14] R. de Orio, H. Ceric, and S. Selberherr, "Physically based models of electromigration: From black's equation to modern tcad models," *Microelectronics Reliability*, vol. 50, no. 6, pp. 775–789, 2010. 2009 Reliability of Compound Semiconductors (ROCS) Workshop).

[15] Z. Sun, S. Yu, H. Zhou, Y. Liu, and S. X.-D. Tan, "Emspice: Physics-based electromigration check using coupled electronic and stress simulation," *IEEE Transactions on Device and Materials Reliability*, vol. 20, no. 2, pp. 376–389, 2020.

[16] C. Multiphysics, "Heat transfer module user's guide," *COMSOL version, vol. 4*, 2014.

Authorized licensed use limited to: Univ of Calif Riverside. Downloaded on June 24,2026 at 00:51:45 UTC from IEEE Xplore. Restrictions apply.