Accelerating Electromigration Wear-out Effects Based on Configurable Sink-Structured Wires

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***Abstract*—In this work, we propose a novel electromigration (EM) wear-out acceleration technique for fast EM reliability-testing and aging-analysis of practical VLSI chips. The new acceleration technique is based on the observation that sink structures have a significant impact on the lifetime of multi-segment interconnect wires. We develop a new configurable sink-structured interconnect wire in which the current in the sink segment can be activated/deactivated dynamically during operation. Using this method, we show how an interconnect structure, which is initially immortal to EM effects, can be induced to fail very quickly. Furthermore, we use a robust failure scheme which considers both early and late failures depending on the wire topology and current direction. The most significant contribution of the proposed work is that it enables EM accelerated testing at low temperature and voltage. This feature enables the testing of EM wear-out in isolation without invoking other reliability effects which are also accelerated by the traditional stressing conditions. Using the proposed method, we can achieve a lifetime reduction from 10+ years to a few days, or even hours, at relatively low temperatures, which is very desirable for practical EM testing of typical nanometer CMOS ICs.**

I. INTRODUCTION

As technology advances, electromigration (EM) has become one of the top reliability concerns for copper dual damascene interconnects. The primary reasons for this trend are increasing current densities and shrinking wire geometries due to aggressive integration. On the other hand, integrated circuits, especially those used in industrial automation, medical devices and IoT applications, have very demanding reliability requirements. As a result, testing and verification of reliability, especially EM-reliability, of VLSI chips used in these applications is critical.

For many practical applications, reliability of 10 years or more is typically expected [1]. However, testing a chip for the duration of its projected lifetime is not practical. Hence, designers need to find accelerated testing and stressing conditions to shorten the validation process. If an acceleration from 10 years to few hours is expected, one needs a time-to-failure (TTF) reduction in the order of 10^4. However, this is quite challenging to achieve in practical VLSI chips, especially when we want the chip to fail only under EM wear-out. The reason is that the traditional acceleration methods, using stressing-conditions based on high temperature and voltage, also accelerate other reliability effects. Moreover these stressing conditions are limited by the underlying physics of semiconductor chips. For instance, there exist some thermal upper limit for practical MOSFET-based microprocessors [2].

To mitigate these problems, recently a configurable reservoir-based wire structure and stressing method was proposed [3]. This method allows for accelerated testing of EM effects under relatively low temperature and does not require any increase in the operational voltage. It was shown that a significant lifetime reduction can be achieved using this method. However, this can only be applied to the ground networks of the chip.

In this article, we propose a novel sink-enhanced EM acceleration technique, in which a configurable sink-structured interconnect wire is exploited for the tests. The sink-based EM acceleration can be applied to the power networks naturally. The new acceleration technique is based on the observation that adding a sink to a multi-segment wire has a significant impact on its lifetime. Fig. 1 shows the hydrostatic stress evolution at the cathode of a straight wire with and without a passive sink attached to its anode (Fig. 2). The geometry and current density of the active wire remain the same in both cases, the only difference being the presence of the passive sink. We can see the wire without the sink is immortal as the stress saturates before it reaches the critical level. However, with the passive sink, critical stress is reached very quickly, leading to void nucleation.

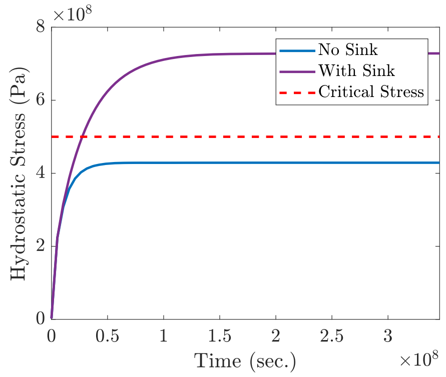

Fig. 1. Stress evolution at cathode with and without a passive sink

It is obvious that we cannot add a sink segment to a wire after fabrication in order to induce a chip to fail quickly on our command. However, we will show how the same effect can be achieved by designing a two segment wire, such as the one shown in Fig. 2, where the current flow through the sink segment can be activated or deactivated dynamically during operation. Using such a simple trigger (i.e. deactivating current in a wire) we can reduce the lifetime of the proposed structure from 10+ years to a few days or even hours. Moreover, this technique requires no increase in operating voltage and very little increase in temperature compared to standard accelerated testing. Therefore, using the proposed method, EM wear-out can be tested in isolation without the concern of accelerating other reliability effects. We believe these features make the proposed method very desirable for practical EM testing of typical nanometer CMOS ICs.

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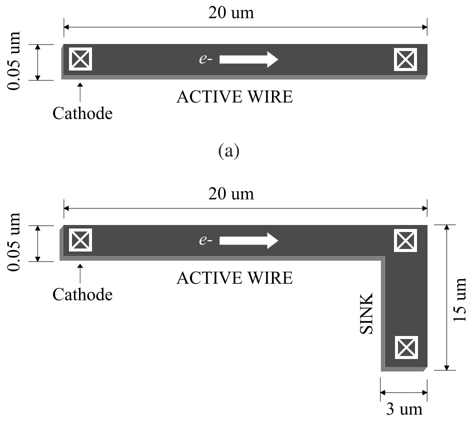


(a)

(b)

Fig. 2. (a) Active wire segment (b) Active wire with passive sink at the anode

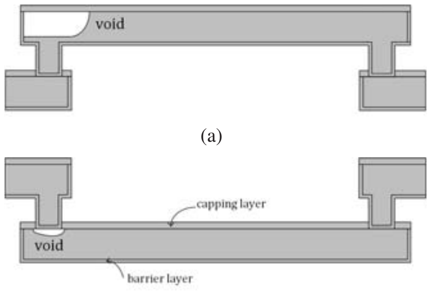
II. REVIEW OF EM PHYSICS AND 3-PHASE EM MODEL

Before we present our new sink-enhanced EM acceleration method, we first briefly review a recently proposed 3-phase EM model, which provides the basis for the proposed work.

Traditionally, EM effects were modeled by the Black-Blech equations [4], [5]. However, Black's model is under growing criticism since the extracted parameters are not consistent when tested under different stressing conditions. On the other hand, the Blech's model is not applicable to general multi-segment interconnects, such as the ones found in typical ICs. To mitigate these problems, a number of new physics-based EM models have been recently proposed [6]–[8]. In these models, the EM failure process consists of two phases: the nucleation phase, in which a void is generated after the critical stress is reached, and the growth phase, in which the void starts to grow.

However, such a simple EM model ignores the fact that, when the void is nucleated or formed, it will not change the wire resistance immediately. It is observed experimentally that there exists a so-called *critical void size* [9], [10], which is typically the via-diameter or cross sectional area of the interconnect wire. When the void is smaller than the critical void size for the wire, no resistance change is observed, this period is called the incubation phase. Based on this observation, a more accurate 3-phase EM model has been recently proposed [11], [12]. In this model, the EM wear-out process consists of three phases: (a) nucleation phase; (b) incubation phase; (c) growth phase. During the three phases, the stress in the confined copper wire is modeled by the stress diffusion equations [13] with blocked material flux boundaries at the via terminals. In the nucleation phase, stress starts to build-up over time. When it exceeds critical stress, void will be formed and we enter the incubation phase. When the void is larger than the critical size for the wire, the wire resistance starts to change and we enter the growth phase. The growth phase persists until the void reaches its saturation volume [14]. The new 3-phase EM model gives a more accurate time to failure estimation and can be applied to more general multi-segment wires since it is based on the stress diffusion physics in confined copper wires.

The proposed three phase EM model also allows us to consider a robust multi-mode failure scheme. Typically, only parametric failures, or late-failures (LF), are considered for EM wear-out where, as the void grows, resistance of the wire slowly increases and reaches a point where the circuit can no longer function as intended. This type of failure occurs in the so called via-below structures as shown in Fig. 3(a), where the flow of electrons is from a lower metal layer to a higher one (hence this structure is also called an upstream structure). In this case, even when the void grows to its critical size (cross sectional area or via diameter), current can still flow through the barrier layer, but, at a much higher resistance. Here the the wire can be considered as failed at the end of the growth phase, which, typically, is the point where the wire increases in resistance by 10% (or other user defined criteria). However, there exist another type of failure, called early-failure (EF), which is observed in the so called via-above structures as shown in Fig 3(b). Here the electron flow is from a higher metal layer to a lower one (hence it is also called a downstream structure). Since a non-conductive capping layer is applied between layers of metallization in the dual damascene process, once the void reaches the critical size, we instantly see an open circuit because current cannot flow though the dielectric capping layer. Therefore, in such structures the wire fails at the end of the incubation phase. This critical distinction can only be accounted for accurately using the new 3-phase EM model. More detailed study on these failure modes can be found in [9], [10].



(a)

(b)

Fig. 3. Via-below or upstream (a) and Via-above or downstream (b) wire structures showing void formation locations.

III. ACCELERATING EM INDUCED FAILURE WITH ATOMIC SINKS

The impact of atomic reservoir and sink structures in manipulating EM induced stress on active interconnect segments have been studied in the past [15], [16]. These structures are good candidates for accelerated testing of EM effects for two reasons. Firstly, they already exist in today's VLSI circuits, and secondly, their impact on EM induced stress can be easily altered by varying the current flow through them. Having the ability to activate/deactivate the current flow through these structures can have a significant impact on the EM lifetime of the active wire segments they are attached to. In this section we will discuss two methods of triggering EM induced failure, at an accelerated rate, on structures that are immortal to EM in their default state.

A. Active wire to passive sink

First let us consider the structure shown in Fig. 4, where two active wires share a common anode. Let us assume the length of the wires (L_W and L_S) are 20um and 15 um respectively. Let us also assume the current densities (J_W and J_S) are both $1.20 \times 10^{10} A/m^2$. Note, these specifications conform to the valid range allowed in the M1 layer of the 32 nm technology node [17].

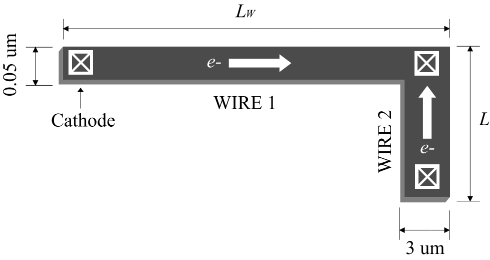


Fig. 4. Immortal 2-segment interconnect structure

Before we discuss the acceleration technique, let us confirm that this structure is indeed immortal to EM by examining the hydrostatic stress evolution at the cathode node of wire 1. Fig. 5 shows that the tensile stress at the cathode node saturates below the critical level, therefore avoiding void nucleation. This structure, at its current operating state, will exceed the typical projected lifetime of VLSI chips (about 10 years).

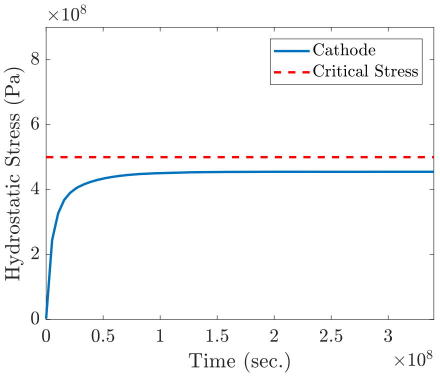


Fig. 5. Stress evolution at cathode (default state)

In order to induce failure in this structure, we simply turn-off the current flow in wire 2. This effectively reverses the direction of flux in wire 2, turning it into a passive sink, and consequently adding to the stress on the cathode end of wire 1 (Fig. 6).

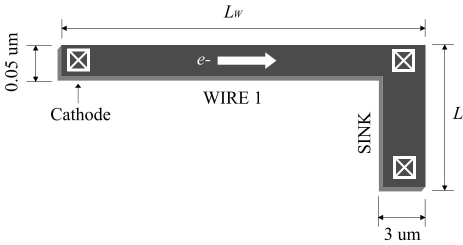


Fig. 6. Wire 2 disabled (converted to a passive sink)

Looking at the stress evolution in this stage (Fig. 7), we see that the critical stress is reached very quickly. This test was repeated on similar structures with different wire lengths and current densities. The results in Table I show that the desired TTF can be easily achieved by simply configuring these parameters accordingly. Note, TTF_{EF} is the TTF for early failure and TTF_{LF} is the TTF for later failure. Using this technique alone, we were able to reduce the lifetime of this structure from 10+ years to 2.45 months, which is an acceleration of $48.98X$. Bear in mind, this was achieved at an operating temperature of only $353°K (79.85°C)$. The circuit was not subjected to high temperatures or current densities. Later we will show how the lifetime can be decreased to a matter of days or even hours using relatively low increase in temperature compared to traditional accelerated testing.

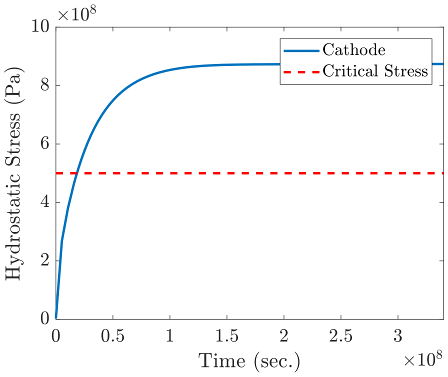


Fig. 7. Stress evolution at cathode (accelerated state)

TABLE I
TTF ACCELERATION: ACTIVE WIRE TO PASSIVE SINK

$L_M(um)$	$L_S(um)$	$J(A/m^2)$	$TTF_{EF}(hrs)$	$TTF_{LF}(hrs)$
100	60	2.90×10^9	1.15×10^5	2.36×10^5
50	30	4.10×10^9	6.76×10^4	1.10×10^5
30	20	6.80×10^9	2.92×10^4	4.47×10^4
20	15	1.20×10^{10}	1.25×10^4	1.83×10^4
15	10	1.60×10^{10}	7.99×10^3	1.13×10^4
10	7	3.10×10^{10}	3.41×10^3	4.54×10^3
8	6	3.80×10^{10}	2.62×10^3	3.36×10^3
7	4	5.30×10^{10}	1.79×10^3	2.25×10^3

B. *Passive sink to active sink*

For the second method let us consider our initial structure to be the one shown in Fig. 6, with the same wire lengths as before. Let us assume the current densities of wire 1 and the sink are $J_W = 6.80 \times 10^9 A/m^2$ and $J_S = 0A/m^2$. In this case the structure already has a passive sink, but it is designed such that the flux through the sink is not enough to cause the steady-state stress at the cathode to reach the critical level. We will once again confirm that this structure is indeed immortal in its default state, then test the effect of acceleration. In this case, acceleration can be achieved by activating current flow in the sink such that the electron flow originates from the anode of wire 1. This turns the passive sink into an active sink, increasing the rate of flux. The increased flux in the sink further enhances the tensile stress at the cathode node of wire 1, consequently accelerating nucleation time as shown in Fig. 8. Similar to the previous method, the desired TTF can be achieved by configuring the dimensions and current densities in these wires as shown in Table II for both early failure and later failure cases.

IV. RESULTS AND DISCUSSION

In this section, we will consider the combined effects of sink-based and temperature-based accelerations. Subjecting the circuit to high temperatures and current densities (high voltage) is a common technique used in accelerated testing. However, this is not a reliable means of testing EM wear-out in isolation since other reliability effects, such as time-dependent-dielectric-breakdown (TDDB), are also accelerated

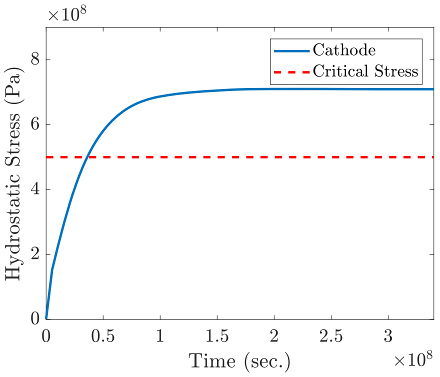


Fig. 8. Stress evolution at cathode (accelerated state)

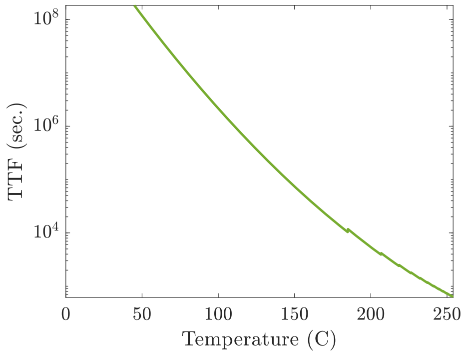


Fig. 9. Enhanced acceleration using temperature

TABLE II
TTF ACCELERATION: PASSIVE SINK TO ACTIVE SINK

$L_M(um)$	$L_S(um)$	$J(A/m^2)$	$TTF_{EF}(hrs)$	$TTF_{LF}(hrs)$
100	60	2.80×10^9	1.16×10^5	2.41×10^5
50	30	3.00×10^9	8.78×10^4	1.46×10^5
30	20	4.30×10^9	4.91×10^4	7.36×10^4
20	15	6.80×10^9	2.26×10^4	3.29×10^4
15	10	9.60×10^9	1.49×10^4	2.03×10^4
10	7	1.60×10^{10}	7.17×10^3	9.35×10^3
8	6	2.20×10^{10}	4.53×10^3	5.80×10^3
7	4	2.80×10^{10}	3.42×10^3	4.29×10^3

with temperature and high voltage. Alternatively, using the proposed sink based acceleration technique, we do not need to increase the temperature above 150°C, which is considered to be the maximum allowed temperature for working CMOS circuits, to get the same or even better acceleration. This allows us to test EM wear-out alone, without the concern of triggering other reliability effects.

Let us once again consider the structure shown in Fig. 4 with $L_W = 7$um, $L_S = 4$um, and $J = 3.10\times10^{10}$. Previously, with the same parameters, we achieved a TTF of 1.79×10^3 hrs (about 2.45 months) as shown in Table. I. However, this was at the temperature of 80°C. A recent study showed that for EM wear-out, 10% increase in temperature, typically will lead to 10X reduction in lifetime [3]. Fig. 9 shows this exponential relationship between TTF and temperature for the structure mentioned above. However, at the same time we do not wish to use extremely high temperatures in these tests for the reasons discussed previously, hence the motivation behind this work. Using the proposed sink based acceleration method, we are able to lower the TTF of the proposed structure to 6.1 days at only 120°C. If slightly higher temperatures are permissible, then even more impressive acceleration can be achieved. For instance, at 150°C, TTF can be lowered to only 20.38 hrs. These results show significant TTF acceleration achieved at relatively low temperatures for accelerated testing.

V. CONCLUSION

In this study, we proposed a novel acceleration technique that allows for the effects of EM to be tested in a controlled manner without the concern of triggering other reliability effects. Taking advantage of the atomic sink structures, which are already present in today's circuits, we were able to show how accelerated EM testing can be done without using the traditional high temperature and voltage testing conditions. Our experimental results show that the proposed method combined with limited temperature acceleration can achieve a lifetime reduction in the order of 10^4, which is very desirable for practical EM testing of typical nanometer CMOS ICs.

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