2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) | 979-8-3503-3265-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/SMACD58065.2023.10192234

Long-Term Aging Impacts on Spatial On-Chip Power Density and Temperature

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***Abstract*—Long-term reliability, such as bias temperature instability (BTI) and hot-carrier injection (HCI), electromigration, etc., significantly impact the chip's performance and lifetime. The existing approaches mainly focus on performance, such as delay and timing impacts, or only consider the BTI impacts on threshold voltage (V_T). However, the impact of BTI on power, specifically on the spatial power density and resulting thermal profile of a functional unit design, has not been thoroughly investigated. In this study, we evaluate the impact of BTI on both the spatial power density and temperature profiles of VLSI chips by considering its effects on multiple parameters of CMOS devices. Our findings show that BTI aging can lead to significant benefits in terms of on-chip temperature and the reduction of hot spots, especially at high operating temperatures, due to the decrease in power density. In this study, we focus on the impact of BTI aging on widely used circuits, such as dot product and dual-port synchronous RAM using a 45nm technology node. To account for the worst-case impact of BTI degradation, we utilized degradation-aware cell libraries that incorporate the maximum ΔV_T of 63mV, i.e., is equivalent to 10 years of operation at V_{dd}=1.2V and T=130°C. Our results indicate that after 10 years of operation, there is a significant impact on maximum power density for both the dot product and RAM circuits, with a reduction of around 5% and 7%, respectively. Similarly, there are noticeable maximum temperature changes, with a decrease of about 10% for the dot product and 6% for the RAM circuits.**

***Index Terms*— Aging, BTI, reliability, power, temperature**

I. Introduction

In today's era of deep nanotechnology, technology scaling has caused the electric properties of transistors to become increasingly vulnerable to various aging mechanisms. These include Bias temperature instability (BTI) and Hot carrier injection (HCI) for devices and electromigration for interconnects. Among these, BTI is the dominant aging effect for CMOS devices in sub-45nm and below.

The effect of BTI on timing and delay has been extensively studied in [4], [6], [7]. Furthermore, [10], [9] have demonstrated that the effect of BTI on timing errors can be observed even in shorter times duration like in order of milliseconds or microseconds. The idea of an accurate timing guard-band estimation using aging-aware timing analysis has been proposed in [4].

It should be noted that less research has been done on the impact of BTI on power. It has been shown in [8] and [11] that BTI can lead to power reduction due to the increase in the transistor threshold voltage; hence circuits can largely get benefits from BTI aging. The author in [8] performed HPSICE simulations on the ring oscillator of 10 FO4 cascaded inverters showed that static power could be reduced to 50% only in one month of operation and can reach up to 78% after 10 years. Additionally, [11] showed SRAM can approximately have a 30% leakage energy reduction in FPGA-based circuits. The existing models considered the BTI impact only on threshold voltage(V_T). However, according to recent research in [5], BTI affects many CMOS device parameters, primarily carrier mobility(μ), sub-threshold slope(SS), gate-drain capacitance(C_{gd}). Therefore, neglecting the impact that BTI has on these important parameters, as the state of the art (e.g., [8]) did, can result in an inaccurate estimation of the effect that BTI has on power. Furthermore, [4] and [5] have shown that impact of BTI aging on the performance of standard cells is non-uniform and depends upon operating conditions (input signal slew and output capacitance), not only on the duty cycle of the transistor.

However, most of those existing methods only considered the BTI impact on the total power consumption. Most importantly, no study showed BTI degradation effect on the spatial power density and the resulting temperature profile of a chip, which is important for future run-time aging- aware thermal and power management/optimization. Hence we performed a detailed study to show the BTI impacts on the on-chip spatial power density and temperature, which we proved is very significant.

In this work, for the first time, we investigated the BTI aging impact on the spatial power density, thermal profile, and hot spots of most widely used circuit blocks (i.e., Dot product, Dual port synchronous RAM) considering multi-parameter BTI impacts.

Our key contributions to this paper are as follows:

1. Unlike other studies, which considered the BTI impacts on total power, our work examined the effects of BTI on the on-chip spatial power density and thermal profile of VLSI chips.
2. To analyze the impact of BTI on power, we have performed aging-aware power analysis for the most widely used circuits like Dot product and the synchronous RAM circuits with commercial EDA tools based on the Nangate 45 nm degradation-aware standard cell library [5].
3. We developed the python-based power map generator to obtain spatial power density, which was then utilized in a thermal model based on the finite element method (FEM) to produce an on-chip spatial thermal map.
4. Our study demonstrates that over time, aging can reduce both the power density and hot spots of the circuits. However, we discovered that while the locations of hot spots differ between these circuits, the location remains unchanged due to BTI aging for a particular circuit.
5. For BTI degradation at V_{dd}=1.2V and T=130°C. The resulting designs lead to maximum ΔV_T=63mV for 10 years of operation. Our study further shows that the 10 year aging can lead to significant maximum power density changes: close to 7% for synchronous RAM, around 5% for Dot product circuits respectively and corresponding maximum temperature changes: nearly 10% for dot product and 6% for RAM circuits.

II. Proposed method for aging effect analysis

In this section, we will present the methodology to investigate the aging effect of BTI on the on-chip spatial power density and temperature. First, we will show the aging-aware power analysis and spatial power density map estimation method. Afterwards, we will present the aging-aware thermal map estimation using a finite element method (FEM) based multi-physics tool.

This work is supported in part by NSF grant under No. CCF-2007135 and in part by NSF grant CCF-2113928.

A. Degradation aware cell libraries

This work used 45nm degradation-aware Cell Libraries from the NanGate Open cell library [3]. Each cell in these degradation-aware libraries have been taken into account for 7x7 combinations of input signal slew and output capacitance. To account for the worst-case BTI degradation impacts on static and dynamic power, V_{dd}=1.2V and T=130°C have been considered in these libraries, which evaluates to a maximum ΔV_T=63mV for 10 years of operation at this operating corner as the author described in [5]. These libraries have taken into account the BTI effect on various crucial parameters of transistors: carrier mobility(μ), sub-threshold slope(SS), gate-drain capacitance(C_{gd}) instead of only accounting for the effect on V_{TH}, which gives us an accurate estimation of the BTI effect on static and dynamic power [5]. These degradation-aware cell libraries can be obtained from the Karlsruhe Institute of Technology (KIT) [1].

B. Aging aware power analysis

Temperature distribution and power density map (on-chip power density distribution) have a very close relationship. In this study, we first performed an aging-aware power analysis using commercial EDA tools, similar to the flow in [5]. The idea for the aging-aware power analysis approach is explained in Fig 1. As shown in Fig 1, we have obtained the synthesized netlist by providing the register transfer level (RTL) description and constraints along with the original library (aging-free) as an input to a synthesis tool (i.e., Synopsys Design Compiler). Afterwards, we passed the synthesized netlist, physical library reference, and constraints to the layout tool (Cadence Innovus) to perform automatic placement and route (APR) to acquire post-layout netlist and RC parasitic information. To verify the functionality, we have performed simulations on various stages of the flow: RTL simulation, gate-level simulation (GLS) on gate-level netlist and post-layout netlist. Finally, the accurate power analysis was performed using the sign-off power analysis tool (Synopsys PrimePower). We have provided the post layout netlist, RC parasitic information, and degradation-aware library reference as input to this tool to obtain the power output under BTI Degradation. On the post-layout netlist, we have performed the gate-level simulation to annotate the netlist with switching activity for precise power analysis. The final stage compared the total power in the aging and no-aging scenarios to determine the power difference.

C. Power density map estimation

We developed a python script based power density map generator to obtain surface power density. The generator receives three inputs: the chip's coordinates, cell placement information from the layout tool, and power data from the sign-off power tool. The generator now divides the chip geometry into 100x100 grids and provides the power density distribution for each grid using the power statistics of the cells and their locations. Although we have used a grid size of 100x100 for more granularity, the generator is extendable to different grid sizes of $N \times N$. If the finer granularity is required, the value of N can be increased. This approach is highlighted in Fig. 2.

D. Temperature map estimation based on thermal model of commercial chips

This subsection will describe thermal modeling based on the finite element method to generate the thermal map. Since packaging information is required to perform thermal simulation. So, we created a heat transfer model that mimics the geometry of actual CPU packaging in COMSOL multiphysics. The reason for using the finite element approach for thermal simulations are that the author in [12] demonstrated that it achieves an accuracy of 1.8°C root mean square error (RMSE).

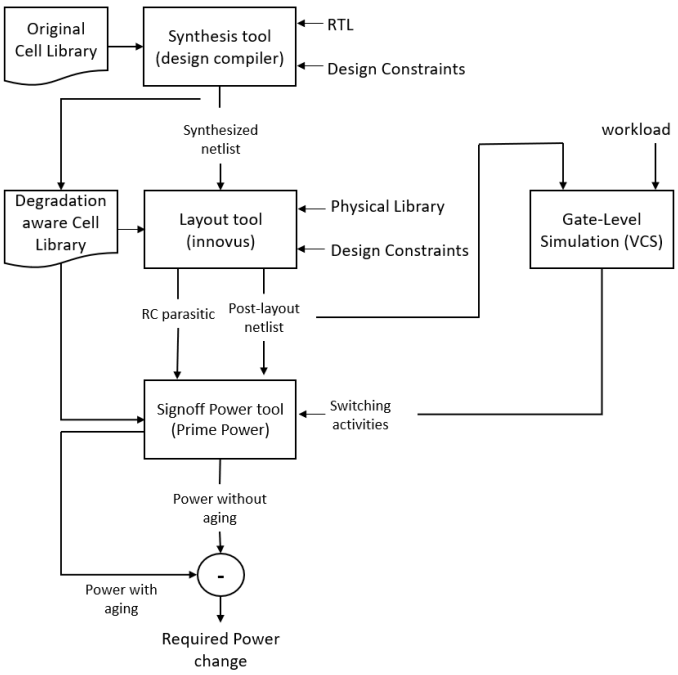


Fig. 1: The proposed aging-aware power analysis flow

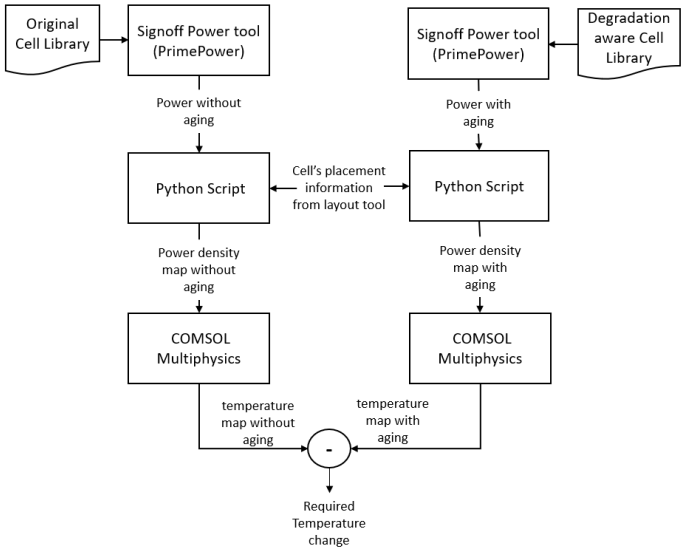


Fig. 2: The proposed aging-aware power density and temperature map estimation flow

This heat transfer model contains four main components: the heat sink, processor baseboard, motherboard, CPU processor die. We have used the measurements relating to these four components to mimic the geometry of the real Intel i7-8650U chip since the geometry for this chip is open-sourced and accessible via the WikiChip group [2].

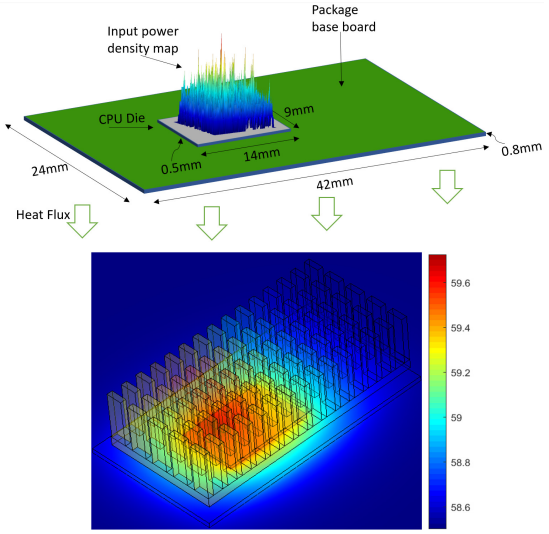
The CPU package dimensions are 42×24×1.3mm, with a baseboard thickness of 0.8mm. There is a CPU die soldered on the baseboard, which is the concern of our study, and has dimensions of 14×9×0.5mm as described in Fig 3a). In our COMSOL model, the material used for the CPU die is silicon, and the material for the package baseboard is FR4. The package base board applies convective heat flux, which simulates the heat flow from the CPU package through the motherboard to the heat sink.

COMSOL utilizes the power density information from our power map generator along with boundary conditions to pro-

vide spatial thermal maps, as highlighted in Fig. 2. Since the circuits used for our proposed idea's evaluation have smaller dimensions than the Intel i7-8650U chip, we used our power map generator to divide the geometry of both chips into 100x100 grids and then mapped the power density of each grid in both chips.

The crucial boundary condition parameters for finite element method based thermal simulations are: ambient temperature and the heat sink's convective heat transfer rate of the heat sink (h_c) to ambient. The procedure for calculating this boundary conditions are described in [12], which utilized sensor temperature data and CPU power information under both workloads and idle states, and this is just a one-time setup for this specific thermal model. Additionally, the identical boundary conditions are employed in our analysis for both the no-aging and the with-aging scenarios, so the impact of the boundary conditions is nullified when calculating the temperature difference due to BTI aging.

Afterwards, thermal simulations were performed for both no-aging and aging cases to evaluate the temperature difference because of BTI aging. Since the same thermal model has been used for both no-aging and with-aging scenarios, it gives a fair estimation of BTI aging's impact on temperature change. The convective heat transfer coefficient h_c is 29.5W·m^{-2}.^{o}C^{-1} and the ambient temperature is 33°C [12]. Fig. 3b shows the 3D view of the thermal map estimated using COMSOL with a transparent heat sink.



(b)

Fig. 3: (a) Thermal model based on the commercial Intel i7-8650U chip (b) 3D view for the heat sink used for thermal model

III. Experimental results and discussions

This section presents the numerical results of the aging impacts on both power density and thermal map of widely used design blocks (i.e., Dot product, Dual port RAM).

A. Impact of BTI on the on-chip power density

It can be observed in Fig 4a that the maximum power density for a RAM circuit without aging approaches nearly 8000MW/m^3 and is reduced to approximately 7500MW/m^3 for 10 years of BTI aging, as shown in Fig. 4b. Additionally, Fig. 4c shows the power density difference map for the RAM circuit. Similar results we noticed with the dot product circuit, where the maximum power density for the dot product circuit approached 650 MW/m^3, as indicated in Fig 5a, and declined to almost 600 MW/m^3 in Fig. 5b in case of aging. The power density difference map for the dot product circuit is displayed in Fig. 5c. This analysis revealed that the location of maximum power density for a specific circuit remains unchanged due to aging, but the location of maximum power density can differ for different circuits due to the workload the circuit is operating on.

B. Impact of BTI for on-chip temperature map

Fig 6 and 7 display the on-chip spatial temperature maps that result in both non-aging and aging situations, as well as maps of the spatial temperature differences for both circuits.

It was observed in Fig. 6a that the maximum temperature without aging approached 127°C and dipped to approximately 123°C for the RAM circuit with 10 years of BTI aging as depicted in Fig. 6b. According to Fig. 6c for the temperature difference map, the maximum temperature difference approached closer to 4°C for the RAM circuit, which is quite noteworthy.

Similarly, for the Dot product circuit, Fig. 7a indicates the maximum temperature of almost 96°C for the non-aging scenario, closer to 86°C in case of aging in fig. 7b. The temperature difference map for the Dot product circuit in Fig. 7c indicates a maximum temperature difference of approximately 10°C.

IV. Conclusions

In this article, we investigated the BTI aging impact on the on-chip spatial power density and temperature for two most widely used circuits (Dual port RAM, Dot product) at V_{dd}=1.2V and T=130°C to account for the worst-case BTI degradation. We demonstrated that the maximum power density reduction for both of these circuits is approximately 7% and 5% respectively. Furthermore, to analyze the BTI impact on spatial temperature, we built the heat transfer model using multiphysics tool to imitate a real chip (Intel i7-8650U) and performed the thermal simulations to evaluate spatial thermal map. The resulting maximum temperature reduction for both these circuits are approximately 6% and 10%, respectively, which is quite significant. Our analysis revealed that the location of maximum power density and the hot spot for a specific circuit remains unchanged due to aging, but the location can differ for different circuits due to the workload the circuit is operating on.

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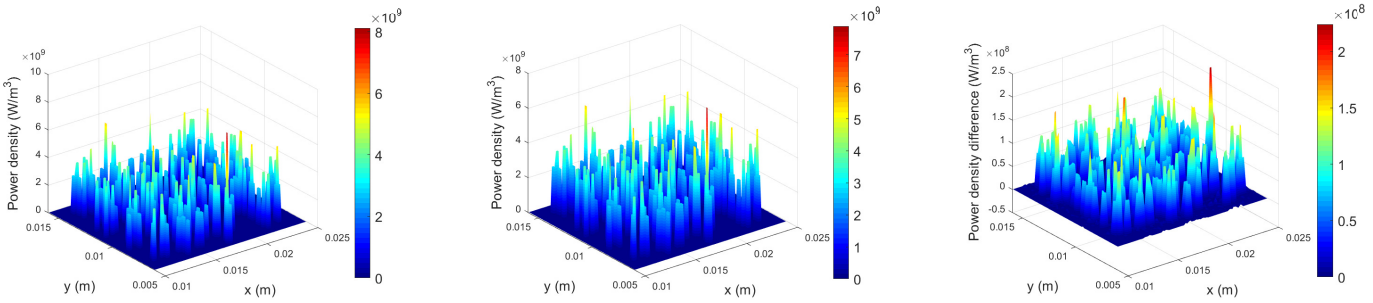
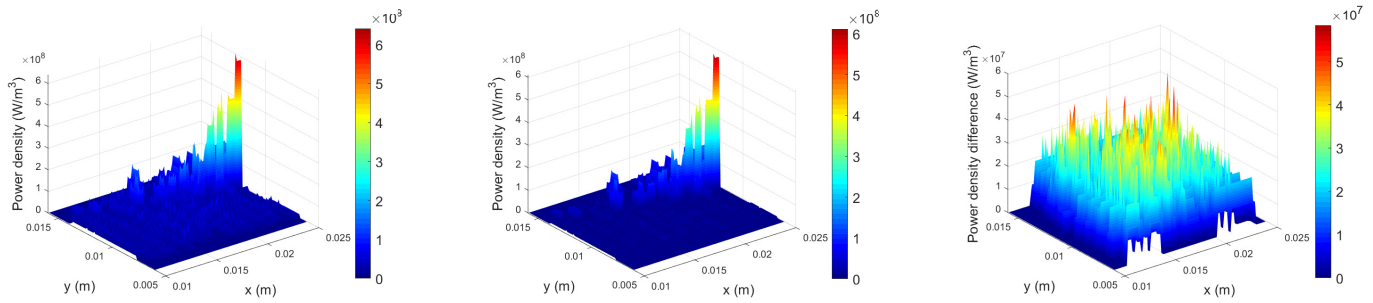


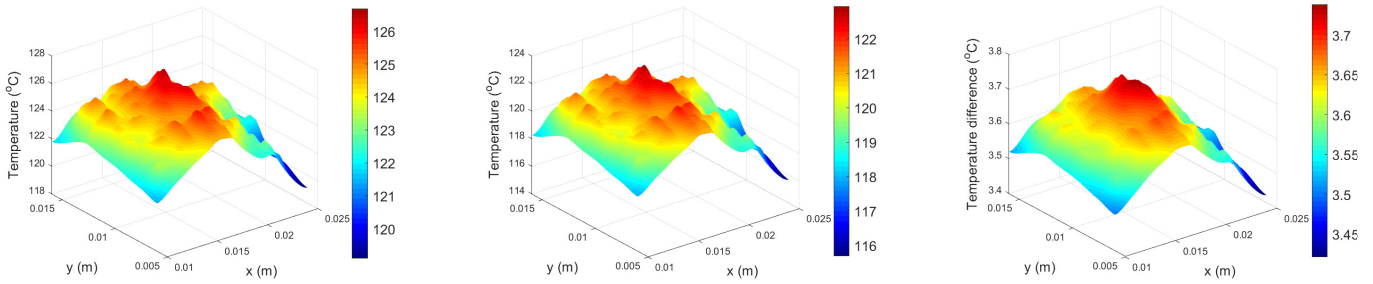
(a) RAM non-aging power density (b) RAM with-aging power density (c) RAM power density difference

Fig. 4: On-chip spatial power density and power density difference maps for RAM circuit



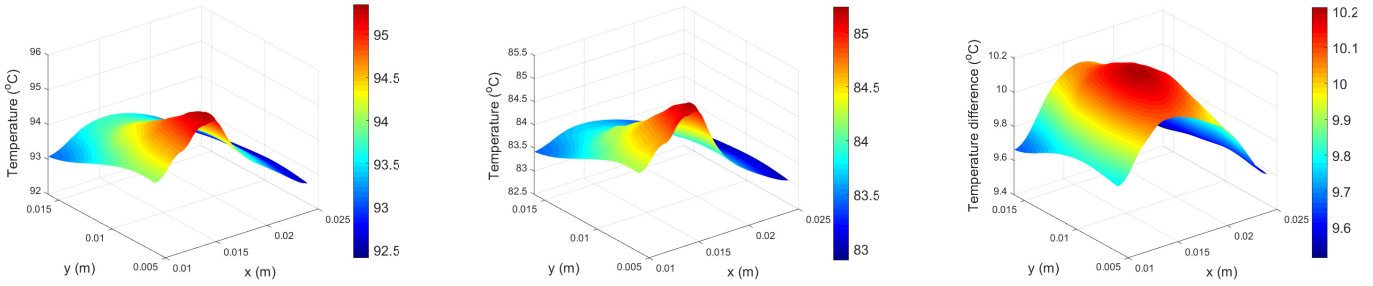
(a) Dot product non-aging power density (b) Dot product with-aging power density (c) Dot product power density difference

Fig. 5: On-chip spatial power density and power density difference maps for Dot product circuit



(a) RAM non-aging thermal map (b) RAM with-aging thermal map (c) RAM temperature difference map

Fig. 6: On-chip spatial temperature and temperature difference maps for Dual port RAM circuit



(a) Dot product non-aging thermal map (b) Dot product with-aging thermal map (c) Dot product thermal difference map

Fig. 7: On-chip spatial temperature and temperature difference maps for Dot product circuit