A New Voltage Binning Technique for Yield Improvement Based on Graph Theory *

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ABSTRACT

In this paper, we propose a new voltage binning technique to improve yield. Voltage binning technique tries to assign different supply voltages to different chips in order to improve the yield. A novel valid voltage segment concept is proposed, which is determined by the timing and power constraints of chips. Then we develop a formulation to predict the maximum number of bins required under the uniform binning scheme from the distribution of length of valid supply voltage segment. With the new concept, an optimal binning scheme can be modeled as a set-cover problem. A greedy algorithm is developed to solve the set-cover problem in an incremental way. The new method is also extendable to deal with a range of working supply voltages for dynamic voltage scaling under different operation modes (like lower power and high performance modes). Experimental results on some benchmarks in 45nm technology show that the proposed method can correctly predict the upper bound on the number of bins required. The optimal binning scheme can lead to significant saving for the number of bins compared to the uniform one to achieve the same yield with very small CPU cost.

1. INTRODUCTION

Process-induced variability has huge impacts on the circuit performance and yield in the nanometer VLSI technologies [6]. Indeed, the characteristics of devices and interconnects are prone to increasing process variability as device geometries getting close to the size of atoms. The yield loss from process fluctuations is expected to increase as the transistor size scaling down. As a result, improving yields considering the process variations is critical to mitigate the huge impacts from process uncertainties.

Supply voltage adjustment can be used as a technique to reduce yield loss, which is based on the fact that both chip performance and power consumption depend on supply voltage. By increasing supply voltage, chip performance improves. Both dynamic power and leakage power, however, will become worse at the same time [10]. In contrast, lower supply voltage will reduce the power consumption but make the chip slower. In other words, faster chips usually have higher power consumption and slower chips often come with lower power consumption. Therefore, it is possible to reduce yield loss by adjusting supply voltage to make some failing chips satisfy application constraints.

For yield enhancement, there are also different schemes for supply voltage adjustment. In [10], the authors proposed an adaptive supply voltage method for reducing impacts of parameter variations by assigning individual supply voltage to each manufactured chip. This methodology can be very effective but it requires significant effort in chip design and testing at many different supply voltages. Recently, a new voltage binning technique has been proposed by the patent [7] for yield optimization as an alternative technique of adaptive supply voltage. All manufactured chips are divided into several bins, and a certain value of supply voltage is assigned to each bin to make sure all chips in this bin can work under the corresponding supply voltage. At the cost of small yield loss, this technique is much more practical than the adaptive voltage supply. But only a general idea is given in [7], without details of selecting optimal supply voltage levels. Another recent work [13] provides a statistical technique of yield computation for different voltage binning schemes. From results of statistical timing and variational power analysis, the authors developed a combination of analytical and numerical techniques to compute joint probability density functions (PDFs) of chip yield as a function of inter-die variation in effective gate length L , and solve the problem of computing optimal supply voltages for a given binning scheme.

However, the method in [13] only works under several assumptions and approximations that will cause accuracy loss in both yield analysis and optimal voltage binning scheme. The statistical model for both timing and power analysis used in [13] are simplified by integrating all process variations other than inter-die variation in L to one random variable following Gaussian distribution. Indeed, the intra-die variations has a huge impact on performance and power consumption [1,9]. And other process variations (gate oxide thickness, threshold voltage, etc) have different distributions and should not be simplified to only one Gaussian distribution. Furthermore, this technique cannot predict the number of voltage bins needed under certain yield requirement before solving the voltage binning problem.

In general, voltage binning for yield improvement becomes an emerging technique but with many unsolved issues. In this paper we propose a new voltage binning scheme to optimize yield. The new method first computes the set of working supply voltage segments under timing and power constraints from either the measurement of real chips or Monte Carlo based SPICE simulations on a chip with process variations. Then on top of the distribution of voltage segment lengths, we propose a formulate to predict the upper bound of bin number needed under uniform binning scheme for the yield requirement. Furthermore, we frame the voltage

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binning scheme as a set-cover problem in graph theory and solve it by a greedy algorithm in an incremental way. The new method is not limited by the number or types of process variabilities involved as it should be based on actual measured results. Furthermore, the new algorithm can be easily extended to deal with a range of working supply voltages for dynamic voltage scaling under different operations modes (like lower power and high performance modes).

Experimental results on a number of benchmarks under 45nm technology show that the proposed method can correctly predict the upper bound on the number of bins required. The optimal binning scheme can lead to significant saving for the number of bins compared to the uniform one to achieve the same yield with very small CPU cost.

2. PROBLEM FORMULATION

2.1 Yield estimation

A "good" chip needs to satisfy two requirements:
1) timing slack is positive $S > 0$ under working frequency.
2) power does not exceed the limit $P < P_{lim}$.

For a single voltage supply, the definition of parametric chip yield is the percentage of manufactured chips satisfying these constraints. Specifically, we compute yield for a given voltage level by direct integration in the space of process parameters:

$$Y = \int \cdots \int_{S>0, P<P_{lim}} f(\Delta\vec{X}_1, \ldots, \Delta\vec{X}_n) d\Delta\vec{X}_1 \ldots d\Delta\vec{X}_n \qquad (1)$$

where $f(\Delta\vec{X}_1, \Delta\vec{X}_2, \ldots, \Delta\vec{X}_n)$ is the joint PDF of $\Delta\vec{X}_1$ to $\Delta\vec{X}_n$, which represents the process variations. Also there exists spatial correlation in the intra-die part of variation. Existing approach in [13] ignores the intra-die variation in process parameters, which means only one random variable for inter-die variation is considered. And all other variations except inter-die variation in L_{eff} are integrated into one Gaussian random variable. In this way, the multi-dimensional integral in (1) can be modeled numerically as a 2 or 3 dimensional integral. However, the spatial correlation can have significant impacts on both statistical timing and statistical power of a circuit [2,9], thus impacts on yield analysis also.

2.2 Voltage binning problem

We first define voltage binning scheme as in [13].

Definition 1. *A voltage binning scheme is a set of supply voltage levels $\vec{V} = \{V_1, V_2, \ldots, V_k\}$, a set of corresponding bins $\vec{U} = \{U_1, U_2, \ldots, U_k\}$, which is also a partitioning of all chips, and a binning algorithm B, which distributes manufactured chips among the bins.*

The binning algorithm B assigns chips to bins so that any chip in bin U_i meets both the performance and power constraints at supply voltage level V_i corresponding to U_i. The yield loss is constituted by chips which fail to be assigned to any bin in $\vec{U}$.

The definition of a voltage binning scheme depends on two factors: the bin voltage levels $\vec{V}$ and the binning algorithm A. Different binning algorithm will result in different yield even given the same bin voltage levels $\vec{V}$. However, in the optimization process, the focus is the binning algorithms which can produce the maximum possible yield. That is to say, in an optimal binning algorithm, there exists at least one voltage bin for any "good" chip (the chips satisfies performance and power constraints). In this way, the yield loss under bin voltage levels $\vec{V}$ will reach the maximum value.

Therefore, the problem of computing optimal voltage binning scheme can be formulated as follows:

$$\max_{\vec{V}} Y; \quad s.t. \qquad V_{min} \leq V_i \in \vec{V} \leq V_{max} \qquad (2)$$

where Y is the total yield under the optimal voltage binning scheme with supply voltage levels $\vec{V} = \{V_1, V_2, \ldots, V_k\}$.

We would like to mention one special type of voltage binning in which we have an infinite number of voltage bins with all possible voltage levels. This binning scheme allows the supply voltage to be individually tailored for each chip to meet timing and power constraints. It is obvious that the yield in this case is the maximum possible yield, named as Y_{max}, which should be an upper bound of yield for any other voltage binning scheme. As a result, for optimal solution, k_{opt} should be the minimum number of bins that make $Y_{k,opt} = Y_{max}$.

3. PROPOSED VOLTAGE BINNING METHOD

Algorithm: NEW VOLTAGE BINNING ALGORITHM

Input: Timing and power constraints, measured data of timing and power from N manufactured chips.
Output: Optimal voltage binning scheme and the corresponding number of bins k_{opt}.

1. Map measured data to a set of V_{dd} segments $\mathcal{S} = \{S_j\}$, in which $S_j = [V_{low,j}, V_{high,j}]$ represents the V_{dd} range at which the jth chip satisfies timing and power constraints.

2. Keep only the valid V_{dd} segments $\mathcal{S}_{val}$ ($V_{low} \leq V_{high}$).

3. Calculate voltage levels and corresponding bins for optimal binning scheme:
   $\mathcal{S}_{left} = \mathcal{S}_{val}$; $i = 1$
   while $\mathcal{S}_{left}$ is not empty
     $\mathcal{S}_{tmp} = \mathcal{S}_{left}$
     GREEDY-SET-COVER($\mathcal{S}_{tmp}$) $\rightarrow \mathcal{S}_{left}, V_i$
     U_i = chips covered by V_i; i ++
   $k_{opt} = i - 1$

Figure 1: The algorithm sketch of the proposed new voltage binning method.

In this section, we present a new voltage binning scheme, which not only gives the good solution for a given set of voltage levels, but also computes the minimum number of bins required. Fig. 1 presents the overall flow of the proposed method and highlights the major computing steps. Basically, Step 1 and 2 compute the valid voltage segment for each chip. Step 3 determinates the voltage levels and the chip assignments to the resulting bins. This is done by a greedy-based set covering method. In Fig. 1, $\mathcal{S}_{left}$ denotes the set of uncovered voltage segments left in the complete set of valid voltage segments $\mathcal{S}_{val}$. V_i is the ith supply voltage level, and chips assigned to U_i can meet both the power and timing constraints at supply voltage V_i.

The algorithm in Step 3 tries to find the voltage level one at a time such that it can cover as many chips as possible in a greedy fashion (a chip is covered if its valid V_{dd} segment contains the given voltage level). The algorithm stops when all the chips are covered, and the number of levels seen so far (k_{opt}) will be the minimum number of bins that can reach the maximum possible yield Y_{max}. In the new algorithm, we can also provide a formulation to predict the minimum number of bins required under the uniform binning scheme from the distribution of length of valid V_{dd} segment, which can serve as a guideline for the number of bins required.

3.1 Voltage binning considering valid segment

For a chip, the working supply voltage range (segment) $[V_{low}, V_{high}]$ actually can be considered as a knob to do the trade-off between the power and timing of the circuit. As we know, supply voltage affects power consumption and timing performance in opposite ways. Reducing supply voltage will decrease the dynamic power and leakage power, which is often considered the most effective technique for low power design. On the other hand, propagation delay will increase as supple voltage decreases [11]. Fig. 2 shows the mean delay and power consumption as functions of supply voltage, which show such trends clearly. As a result, given the power

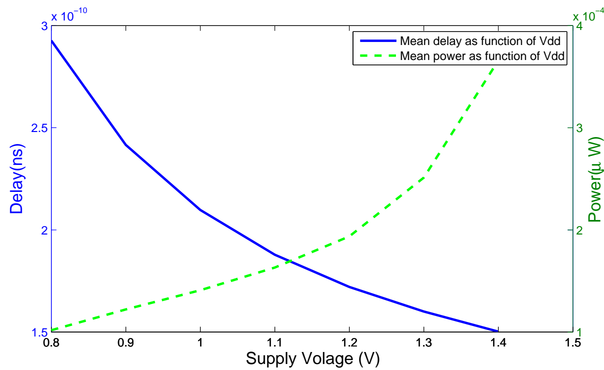

Figure 2: The delay and power change with supply voltage for C432.

consumption bound and the timing constraint for a chip, V_{low} is mainly decided by timing and V_{high} is mainly determined by power constraint. Since process variation leads to different timing performances and power consumptions, the valid V_{dd} segment $[V_{low}, V_{high}]$ will be different for each chip. As a result, the measured timing and total power data from a chip can be mapped onto corresponding working V_{dd} segments, which is the Step 1 in Fig. 1. For some chips, we may have $V_{low} > V_{high}$ (invalid segment), which means that these chips will fail on any supply voltage. So we call them "bad" chips.

Suppose there are N sampling chips from testing, and n_{bad} are bad chips. Obviously, the maximum of possible yield via voltage binning scheme only will be

$$Y_{max} = (N - n_{bad})/N, \quad (3)$$

We then define the set of valid segments $\mathcal{S}_{val} = [V_{low}, V_{high}]$ by removing the bad chips from the sampling set and only keeping the valid segments (Step 2 in Fig 1). Then the voltage binning scheme problem in (2) can be framed into a set-cover problem. Take Fig. 3 for instance, there are $n_{val} = 13$ horizontal segments between V_{min} and V_{max} (each corresponds a valid V_{dd} segment), and the problem becomes using minimum number of vertical lines to cover all the horizontal segments. In this case, three voltage levels can cover all the V_{dd} segments of these 6 chips. We also notice that one chip can be covered by more than one voltage level. In this case, it can be assigned to any voltage level containing it. The problem is well known in graph theory with known efficient solutions. This valid voltage segment model has many ben-

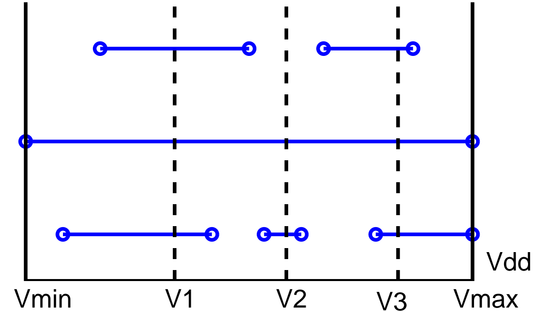

Figure 3: Valid voltage segment graph and the voltage binning solution.

efits compared with other yield analysis model for voltage binning:

1. Distribution of length of valid supply voltage segment can provide information about the minimum number for uniform binning under certain yield requirement (e.g. to achieve 99% for Y_{max}, more details in 3.2.)
2. The model can also be used when the allowed supply voltage level for one voltage bin is an interval or a group of discrete values for voltage scaling mechanism instead of a scalar (details in Section 3.3). To the best knowledge of the authors, this proposed method is the first one working for this case.

3.2 Bin number prediction under given yield requirement

The distribution of valid V_{dd} segment length (defined as $len = V_{high} - V_{low}$) can be a guide in yield optimization when there is a lower bound requirement for yield. And it works for both uniform binning and optimal binning. Notice that the optimal binning can always has an equal or better yield than the uniform binning. Actually the experiment result part shows that the number of bins needed for optimal voltage binning is much smaller than the prediction from the distribution of len. Fig. 4 shows the histogram of valid supply voltage length, len, for testing circuit C1908. From which we can see that it is hard to tell which type of random variable it belongs to. However, it is quite simple to get the numerical probability density function (PDF) and cumulative distribution function (CDF) from measured data of testing samples, as well as the mean value and standard deviation.

Suppose the yield requirement is Y_{req}, and the allowed supply voltages for testing is in $[V_{min}, V_{max}]$. For the uniform voltage binning scheme, there is k bins, and the set of supply voltage levels is $\vec{V} = \{V_1, V_2, \ldots, V_k\}$. Since the voltage binning scheme is uniform,

$$V_i - V_{i-1} = \Delta V \quad \text{const.} \quad (i = 2, 3, \ldots k). \quad (4)$$

For the uniform voltage binning scheme, we have the following observations:

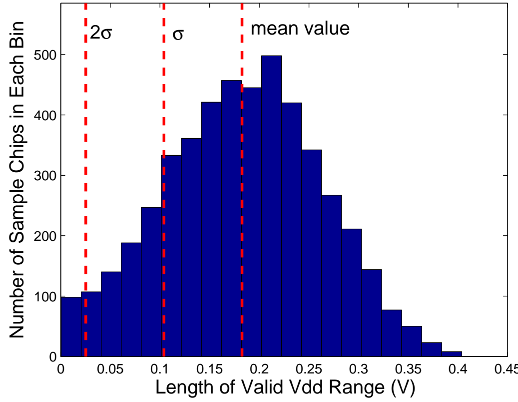

Figure 4: Histogram of the length of valid supply voltage segment len for C1908.

Observation 1. If there are k bins in $[V_{min}, V_{max}]$, then

$$\Delta V = (V_{max} - V_{min})/(k+1). \tag{5}$$

Observation 2. For a V_{dd} segment $[V_{low}, V_{high}]$ with a length $len = V_{high} - V_{low}$, if $len > \Delta V$, there must exist at least one V_{dd} level in the set of supply voltage levels $\vec{V} = \{V_1, V_2, \ldots, V_k\}$ that can cover $[V_{low}, V_{high}]$. Now we have the following results:

Proposition 1. *For the yield requirement Y_{req}, the upper bound for voltage binning numbers k_{up} can be determined by*

$$k_{up} = \frac{V_{max} - V_{min}}{F^{-1}(1 - Y_{req})} - 1, \tag{6}$$

where $F^{-1}(len)$ is the inverse function of cumulative distribution function (CDF) of len.

(6) basically says that the upper bound for the numbers of voltage bins in uniform scheme can be predicted from the yield requirement and the distribution of *len*.

Proof sketch for Proposition 1:
If the chip satisfies the yield requirement Y_{req},

$$1 - F(\Delta V) \le Y_{req} \quad (Observation 2). \tag{7}$$

For the upper bound for voltage binning numbers k_{up}, the corresponding ΔV_{min} can be calculated by

$$\Delta V_{min} = \frac{V_{max} - V_{min}}{k_{up} + 1} \quad (Observation 1). \tag{8}$$

From (7) and (8),

$$Y_{req} = 1 - F(\Delta V_{min}) = 1 - F\left(\frac{V_{max} - V_{min}}{k_{up} + 1}\right). \tag{9}$$

which is equivalent form of (6). Q.E.D.

Notice that the optimal binning always has a better or equal yield compared to uniform binning using same number of bins. Therefore, if the uniform voltage binning scheme with k bins already satisfies the yield requirement, k bins must be enough for the optimal voltage binning scheme. So the histogram for the length of valid V_{dd} segment can be used to estimate the upper bound for the number of bins needed for a certain yield requirement for both uniform and optimal voltage binning schemes. And this process can be done right after mapping measured power and timing data to working V_{dd} segments.

3.3 Yield analysis and optimization

The whole voltage binning algorithm for yield analysis and optimization is given in Fig. 1. After the yield analysis and optimization, supply voltage levels $\vec{V} = \{V_1, V_2, \ldots, V_{k,opt}\}$, the corresponding set of bins $\vec{U} = \{U_1, U_2, \ldots, U_{k,opt}\}$ can be calculated up to k_{opt}, where $Y_{k,opt} = Y_{max}$ already.

There are many algorithms for solving the set-cover problem in Step 3. By choosing optimal set-cover algorithm, the global optimal solution can be obtained. In this case, the decision version of set-covering problem will be NP-complete. In this paper we use a greedy approximation algorithm as shown in Fig. 5, which can easily be implemented to run in polynomial time and achieve a good enough approximation of optimal solution. Notice that the greedy approximation is not necessary and any algorithm for set-cover can be used in Step 3, which is not a limitation for our valid supply voltage segment model. The solution found by GREEDY-SET-COVER is at most a small constant times larger than optimal [3], which is found already satisfactory as shown in the experimental results. Besides, the greedy algorithm can guarantee that each voltage level will cover the most segments corresponding to uncovered testing chips, which means this algorithm is incremental. As a result, if only $k-1$ bins is needed, we can stop the computation at $k-1$ instead of k. And when the designer needs more voltage bins, the computation doesn't need to be start all over again. Actually the benefit of incremental voltage binning scheme is very useful for circuit design. Since when the number of bins increase from $k-1$ to k, the existing $k-1$ voltage levels will be the same.

Core algorithm: GREEDY-SET-COVER($\mathcal{S}$).

1. Select an supply voltage value V_g value which covers most voltage segments in $\mathcal{S}$
2. $\mathcal{C} \leftarrow \emptyset$
3. **for** i = 1 : size($\mathcal{S}$)
   if $V_g \in S_i$
   $\mathcal{C} \leftarrow \mathcal{C} + S_i$
4. **return** $\mathcal{C}$

Figure 5: The flow of greedy algorithm for covering most uncovered elements in $\mathcal{S}$.

We remark that the proposed method can be easily extended to deal with a group of discrete values $V_{g,1}, V_{g,2}, \ldots$ for dynamic voltage scaling under different operation modes instead of a single voltage. For example, if the ith supply voltage level V_i contains two discrete values, V_s and V_h, which are the supply voltages for saving-power mode and high-performance mode, respectively (anything in between also works for the selected chips). Set-cover algorithm in Fig. 5 now will use a range V_g (defined by users) to cover the voltage segments instead of a single voltage level. Such extension is very straightforward for the proposed method.

4. NUMERICAL RESULTS

In this section, the proposed voltage binning technique for yield analysis and optimization was verified on circuits in the ISCAS85 benchmark set with constraints on timing performance and power consumption. The circuits were synthesized with Nangate Open Cell Library. The technology parameters come from the 45nm FreePDK Base Kit and PTM models [8]. The proposed method has been imple-

mented in Matlab 7.8.0. All the experimental results are carried out in a Linux system with quad Intel Xeon CPUs with 2.99Ghz and 16GB memory.

4.1 Setting of process variation

For each type of circuit in the benchmark, 10000 Monte Carlo samples are generated from process variations. In this paper, effective gate length L and gate oxide thickness T_{ox} are considered as two main sources of process variations. According to [5], the physical variation in L and T_{ox} should be controlled within +/-12%. So the 3σ values of variations for L and T_{ox} were set to 12% of the nominal values, of which inter-die variations constitute 20% and intra-die variations, 80%. L is modeled as sum of spatial correlated sources of variations, and T_{ox} is modeled as an independent source of variation. The same framework can be easily extended to include other parameters of variations. Both L and T_{ox} are modeled as Gaussian parameters. For the correlated L, the spatial correlation was modeled based on the exponential models [12].

The power and timing information as a function of supply voltage for each testing chip is characterized by using SPICE simulation. Under $45nm$ technology, typical supply voltage range is $0.85V - 1.3625V$ [4]. Since that, V_{dd} is varied between 0.8 volt and 1.4 volt in this paper, which is enough for $45nm$ technology.

We remark that practically the power and timing information can be obtained from measurements. As a result, all the sources of variability of transistors and interconnects including inter-die and intra-die variations with spatial correlations will be considered automatically.

4.2 Prediction of bin numbers under yield requirement

As mentioned in 3.2, the proposed valid segment model can be used to predict the number of bins needed under yield requirement before voltage binning optimization. Table 1 shows the comparison between the predicted number and the actual number needed under yield requirement for the testing chips. In this table Y_{req} means the lower bound requirement for yield optimization (normalized by Y_{max}). Column 3 is the predicted number of bins; and columns 4 and 5 are the actual bin numbers found for the uniform and optimal voltage binning schemes, respectively. This table validates the upper bound formulation for the needed number of bins in 3.2. From this table, we can see that the predicted value is always the upper bound of actual number of bins needed, which can be applied as a guide for yield requirement in optimization. Table 1 also shows that the optimal voltage binning scheme can significantly reduce the number of bins compared with the uniform voltage binning schema under the same yield requirement. When yield requirement is 99% of the optimal yield, the optimal voltage binning scheme can reduce 52% bin count on average.

Table 1: Predicted and actual number of bins needed under yield requirement.

Circuit	Y_{req}	Predicted	Real for Uni.	Real for Opt.
C432	99%	25	23	4
	97%	10	9	3
	95%	7	6	3
C1908	99%	27	12	7
	97%	11	6	3
	95%	7	3	3
C2670	99%	8	4	3
	97%	5	3	2
	95%	3	2	1
C7552	99%	30	12	5
	97%	9	4	3
	95%	6	3	2

4.3 Comparison between uniform and optimal voltage binning schemes

Experiments for both uniform and the optimal voltage binning schemes with different number of bins are used to verify the proposed voltage binning technique. Table 2 shows the results, where Y_{max} is the maximum chip yield which can be achieved when V_{dd} is adjusted individually for each manufactured chip, VB stands for voltage binning schemes used and k_{opt} is the minimum number of bins to achieve Y_{max}. From Table 2, we can see that the yield of optimal VB always increases with the number of bins, with Y_{max} as the upper bound. And the voltage binning can significantly improve yield compared with simple supply voltage. Column 8 in Table 2 shows that the number of bins needed to achieve Y_{max} in optimal voltage binning schemes is only 1.88% of number of bins needed in the uniform scheme on average, which means that optimal voltage binning schemes is much more economic in order to reach the best possible yield.

Table 2: Yield under Uniform and Optimal voltage binning schemes (%).

Circuit	Y_{max}	VB	1 bin	2bins	5bins	10bins	k_{opt}
C432	96.66	Uni.	60.19	79.04	90.52	94.36	4514
		Opt.	80.08	88.68	96.42	96.66	10
C1908	98.06	Uni.	71.80	91.46	95.20	97.04	437
		Opt.	89.18	92.88	97.18	98.06	21
C2670	90.15	Uni.	81.12	87.13	89.74	89.95	1205
		Opt.	85.77	88.34	89.83	90.08	13
C7552	93.46	Uni.	73.94	86.38	91.40	92.34	1254
		Opt.	87.22	90.30	92.64	93.26	18

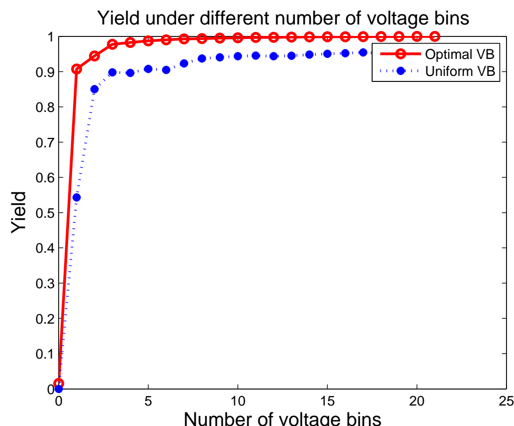

Figure 6: Yield under uniform and optimal voltage binning schemes for C1908.

Fig 6 compares the yields from uniform and optimal voltage binning schemes with the number of bins from 1 to

10 for C1908. This figure shows that the optimal binning scheme always provides higher yield than the uniform binning scheme. For optimal voltage binning scheme, the yield increasing speed is slower down as the bin number increases since we use greedy algorithm. For other testing circuits, similar phenomenon is observed from the yield results.

4.4 Sensitivity to frequency and power constraints

For very strict power or frequency constraints, voltage binning can provide more opportunities to improve yield. Figure 7 shows the changes in parametric yield for C1908 with and without voltage binning yield optimization due to the changes in frequency and power consumption requirements, where P_{norm} is normalized power constraint and f_{norm} is normalized frequency constraint. By analyzing this figure, we can see that parametric yield is sensitive to both performance and power constraints. As a result, yield can be substantially increased by binning supply voltage to a very small amount of levels in the optimal voltage binning scheme. For example, without voltage binning technique, the yield will fall down 0% when constraints become 20% stricter, while the voltage binning technique can keep the yield as high as 80% under the same situation.

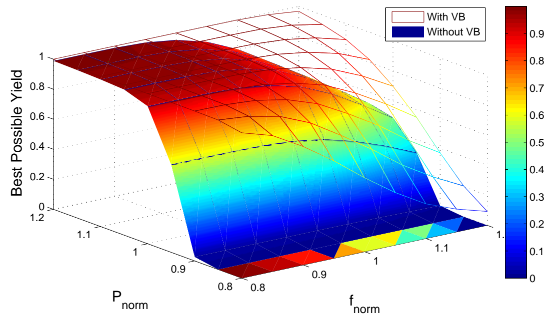

Figure 7: Maximum achievable yield as function of power and performance constraints for C1908.

4.5 CPU times

Table 3 compares the CPU times among different voltage binning schemes and different number of bins. Since the inputs of our algorithm in Fig. 1 are the measured data for real chips practically, the time cost of measuring data is not counted in the time cost of the voltage binning method. But in this paper, the timing and power data is generated from SPICE simulation. There are three steps in our proposed method as shown in Fig. 1. It is easy to see that the time complexity of Step 1 and 2 are both $O(N)$, where N is the number of MC sample points. From [3], Step 3 can run within $O(N^2 ln(N))$ time. Therefore, the speed of our voltage binning algorithm is not related to the size of circuits. Table 3 confirms that binning technique is insignificant even for the case of 10 bins, and the time cost is not increasing with the number of gates on chip.

5. CONCLUSION

We have proposed a new voltage binning technique to improve the yield of chips. First, we have proposed formulation to predict the maximum number of bins required under the uniform binning scheme from the distribution of valid V_{dd} segment length. We then developed an approximation of optimal binning scheme based on greedy-based set-cover solution to minimize the number of bins and keep the corresponding voltage levels incremental. The new method is also extendable to deal with a range of working supply voltages for dynamic voltage scaling operation. Experimental results on some benchmarks on 45nm technology show that the proposed method can correctly predict the upper bound on the number of bins required. The proposed optimal binning scheme can lead to significant saving for the number of bins compared to the uniform one to achieve the same yield with very small CPU cost.

Table 3: CPU time comparison(s).

Circuit	VB	1 bin	2bins	5bins	10bins
C432	Uni.	0.0486	0.0571	0.0866	0.1374
	Opt.	0.0747	0.0786	0.0823	0.0827
C1908	Uni.	0.0551	0.0749	0.1237	0.2037
	Opt.	0.0804	0.0840	0.0874	0.0901
C2670	Uni.	0.0347	0.0371	0.0425	0.0504
	Opt.	0.0686	0.0696	0.0711	0.0704
C7552	Uni.	0.0476	0.0565	0.0925	0.1493
	Opt.	0.0775	0.0791	0.0802	0.0812

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