Passive Hierarchical Model Order Reduction and Realization of RLCM Circuits

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ABSTRACT

This paper presents a novel compact passive modeling technique for high-performance RF passives and interconnects modeled as high-order RLCM circuits. The new method is based on a recently proposed general *s*-domain hierarchical modeling and analysis method. In this work, we first apply state-space based optimization technique to enforce passivity on the hierarchical model order reduced admittance matrix. To realize the passivity-enforced admittance, we propose a general multi-port network realization method based on relaxed one-port network synthesis technique based on Foster's canonical form. The resulting modeling algorithm leads to general *SPICE*-in and *SPICE*-out multi-port passive realization of any linear passive networks with easily controlled model accuracy and complexity. The experimental results on a number of PEEC modeled bus lines circuits demonstrate the effectiveness of the proposed algorithm.

I. INTRODUCTION

As more devices are integrated into a single chip, design verification becomes more difficult. The reduction of design complexity especially for those extracted high-order RLCM network is important for efficient VLSI design. Compact modeling of RC or RLC networks for interconnects has been an intensive research area in the past decade. The existing approach can be classified into two categories. The first is based on subspace projections [7, 10, 12, 13, 18]. Projection-based method was pioneered by Asymptotic Waveform Evaluation (AWE) algorithm [13] where explicit moment matching was used to compute dominant poles at low frequencies. Pade via Lanczos (PVL) [7], Arnoldi Transformation method [18] improved the numerical stability of AWE, congruence transformation method [10] and PRIMA [12] can further produce passive models. However the circuit realized from all these techniques is quite complicated. An efficient first few order moments matching based realization for interconnect RLC circuit is proposed in [9]. In general, no systematic approach is proposed to realize any linear passive networks.

Another quite different approach to circuit complexity reduction is by means of local node reduction and realization of reduced networks based on local node elimination and realization [2, 6, 15–17, 20]. The main idea is to reduce the number of nodes in the circuits and approximate the remaining elements of the reduced circuit matrix, in order-reduced rational forms or in the form of realized low order RLCM networks. The major advantage of these methods over projection-based methods is that the reduction can be done in a local manner and no overall solutions of the entire circuit are required, which makes these methods very amenable to attack large linear networks. This idea was first explored by selective node elimination for RC circuits [6, 16], where time constant analysis is used to select nodes for elimination.

Node reduction for the magnetic coupling interconnect (RLCM) circuits has been an active research area recently. Generalized Y-Δ transformation [15], RLCK circuit crunching [2], and branch merging [17] have been developed based on nodal analysis (NA), where inductance becomes susceptance in the admittance matrix. Since mutual inductance is coupled via branch currents, to perform nodal reduction, an equivalent 6-susceptance NA model is introduced in [15] to reduce two coupling current variables and template matching via geometrical programming is used to realize the model order reduced admittances. But accuracy depend heavily on the selection of templates and only 1-port realization was reported. Meanwhile, RLCK circuit crunching and branch merging methods are first-order approximation based on the node time constant analysis. The drawbacks for such first-order approximation are that: (1) errors are controlled in a local manner and will be accumulated. Hence it is difficult to control the global errors due to reduction; (2) not too many nodes can be reduced if the elimination condition is not satisfied.

In this paper, we proposed a new passive reduction and realization algorithm for any distributed high-order RLCM circuits. The new modeling technique is based on the general multiple-point *s*-domain hierarchical model reduction algorithm presented in [14, 20]. Compared with other reduction methods, this approach promises the compact modeling for both passive and active linear networks. The main contribution of this paper are: (1) we apply state-variable based convex programming method [4] to optimize the hierarchical model order reduced admittance matrix to enforce the passivity; (2) Foster's canonical form based *n*-port network realization technique is used to realize the passive model order reduced admittance in an error-free manner. The resulting modeling algorithm can deliver general *SPICE*-in and *SPICE*-out multi-port passive realization of any linear passive networks with easily controlled model accuracy and complexity.

The paper is organized as follows. Section II gives a background on the hierarchical modeling technique and the concepts of passivity and positive-realness. Section III will discuss state-space based passivity enforcement algorithm on the reduced admittance matrix. In section IV, we will describe the

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whole realization process, which includes a generalized n-port relaxed Foster's canonical form based network synthesis technique. The experimental results and conclusions are presented in section V and section VI, respectively.

II. Background

A. Passivity and positive-realness

Passivity is an important property of many physical systems. A passive network does not generate energy. If the reduced order model (ROM) lose its passivity, it may lead to unbounded responses in transient simulation, which means new energy has been generated in this network.

O. Brune [3] has proved that the admittance and impedance matrix of an electrical circuit consisting of an interconnection of a finite number of positive R, positive C, positive L, and transformers are passive if and only if their rational functions are positive real. A network with admittance matrix function $\mathbf{Y}(s)$ is said to be positive real iff

$$\begin{array}{ll}(1) & \mathbf{Y}(s) \text{ is analytic, for } Re(s) > 0\\ (2) & \overline{\mathbf{Y}(s)} = \mathbf{Y}(\bar{s}) \text{ , for } Re(s) > 0\\ (3) & \mathbf{Y}(s) + \mathbf{Y}(s)^H \geq 0 \text{ , for } Re(s) > 0\end{array}$$

Condition (1) means that there is no unstable poles (poles lie on right-half-plane (RHP) in s-domain). Condition (2) refers to system that has real response. And condition (3) is equivalent to that the real part of $\mathbf{Y}(s)$ is a positive semidefinite matrix at all frequencies. So it is only necessary condition that a positive-real function have no poles in the RHP. But condition (3) is difficult to check as it require the checking of frequency responses from DC to infinite.

Fortunately, there is a better way to check the positive realness. It can be proved that the following statements are equivalent:

(a) a transfer function matrix $\mathbf{Y}(s)$ is positive real.

(b) Let $(A\ B\ C\ D)$ be a minimal controllable state-space representation of $\mathbf{Y}(s)$. $\exists K$,

$$K = K^T, K \geq 0, \tag{1}$$

such that the Linear Matrix Inequality (LMI)

$$\left[\begin{array}{cc} A^TK + KA & KB - C^T \\ B^TK - C & -D - D^T \end{array}\right] \geq 0 \tag{2}$$

holds.

If we include the term proportional to s in the transfer function, which means we would like to know what would happen in infinite frequency, we can write the admittance matrix in terms of $(A\ B\ C\ D)$ as

$$\mathbf{Y}(s) = sY^{\infty} + D + C(sI - A)^{-1}B \tag{3}$$

where I denote an identity matrix with the same dimension as A. In order to keep the transfer function still positive real, the term Y^{∞} must satisfy

$$Y^{\infty} = (Y^{\infty})^T, Y^{\infty} \geq 0 \tag{4}$$

In summary, we transfer the problem of checking whether the admittance matrix $\mathbf{Y}(s)$ is positive real into the problem of checking whether its corresponding state space model in terms of $(A\ B\ C\ D)$ is positive semidefinite. It turns out that the latter is more easily to check and enforce than the former. Also it is not necessary to get the minimal state space realization when we change the admittance parameters matrix into its state space form as shown below.

B. Hierarchical multi-point model order reduction

The general s-domain hierarchical model order reduction method [20] is a general model order reduction technique that can be applied to any linear networks (passive or active). However, like AWE method, it suffers the numerical problems for computing high order terms due to polynomial divisions. The multi-point hierarchical method has been proposed to alleviate this problem [14], where multiple expansions along real or complex frequency axis are performed and poles obtained from different expansion poles are combined to get more accurate models over wide frequency ranges. We notice that similar ideas have been exploited before in projection based reduction approaches to improve the modeling accuracy [5,8]. The rational behind such a strategy is that dominant poles that are close to the expansion points can be more accurately captured than the poles that are far away from the expansion points in the moment matching based approximation framework. Therefore instead of expanding at one point, we can expand at multiple points to accurately capture all the dominant points in the given frequency range along real or complex axis.

III. Passive Enforcement

In this section, we present the state-space based passivity enforcement method which is similar to the method used in [4]. But we show how this method can be used in our hierarchical model order reduction framework to enforce passivity of the model order reduced admittances $\tilde{\mathbf{Y}}(s)$.

A. State-space model representation of $\tilde{\mathbf{Y}}(s)$

After the multiple-point hierarchical model reduction, an n-port order reduced admittance matrix is generated as shown in Eq.(5), where each $\tilde{\mathbf{Y}}_{p,q}$ is a rational function of s. The reduction process can capture the entire dominant complex poles, which means there is no poles in the RHP of the complex plane.

$$\tilde{\mathbf{Y}}(s) = \left[\begin{array}{ccc} \tilde{\mathbf{Y}}_{1,1} & \cdots & \tilde{\mathbf{Y}}_{1,n} \\ \vdots & \ddots & \vdots \\ \tilde{\mathbf{Y}}_{n,1} & \cdots & \tilde{\mathbf{Y}}_{n,n} \end{array}\right] \tag{5}$$

The first step we do is to transform the admittance matrix $\tilde{\mathbf{Y}}(s)$ into its state-space representation. We assume that all rational functions in the matrix share the common poles of the system. If there are private poles appearing on the leading diagonal element, we can separate them and their residues from the whole rational function after partial fraction decomposition and realize them separately.

Given a multivariable n-port network, each rational function $\tilde{\mathbf{Y}}_{p,q}$ is considered as a Single-Input and Single-Output (SISO) subsystem and mapped to its state-space representation in controllable canonical form, which correspond to

$(A_{q,q}\ B_{q,q}\ C_{p,q}\ D_{p,q})$ in the matrix of $(A\ B\ C\ D)$ respectively. Now we can write its state-space representation as Eq.(6)

$$A=\begin{bmatrix} A_{1,1} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & A_{n,n} \end{bmatrix} \quad B=\begin{bmatrix} B_{1,1} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & B_{n,n} \end{bmatrix}$$
$$C=\begin{bmatrix} C_{1,1} & \cdots & C_{1,n} \\ \vdots & \ddots & \vdots \\ C_{n,1} & \cdots & C_{n,n} \end{bmatrix} \quad D=\begin{bmatrix} D_{1,1} & \cdots & D_{1,n} \\ \vdots & \ddots & \vdots \\ D_{n,1} & \cdots & D_{n,n} \end{bmatrix} \tag{6}$$

Also this mapping process could be viewed as n sets Single-Input and Multiple-Output (SIMO) subsystems. If we choose the m-th port as input port, the m-th column admittance rational function can be mapped into $(A_{m,m}\ B_{m,m}\ C_{:,m}\ D_{:,m})$.

B. Passivity enforcement optimization

In this subsection, we briefly mention how passivity enforcement is done via a convex optimization process on the state-space representation of the admittance matrix.

Assume that we have obtained the admittance matrix of a model order reduced system $\tilde{\mathbf{Y}}(s)$ with a set of N sampling points. Let $\tilde{\mathbf{Y}}_{p,q}(s)$ denote the (p,q) entry of the transfer function $\tilde{\mathbf{Y}}(s)$. Let $\hat{\mathbf{Y}}_{p,q}(s_k)$ be the exact value of the entry (p,q) at the kth frequency point.

The optimization problem is to determine C, D, Y^∞ such that a cost function is minimized with constraints on the error $(\tilde{\mathbf{Y}}_{p,q}-\hat{\mathbf{Y}}_{p,q})$. Here the constraints are on the weighted least square error, taken over N frequencies

$$\sum_{k=1}^{N} w_{k,p,q}\|\tilde{\mathbf{Y}}_{p,q}(s_k)-\hat{\mathbf{Y}}_{p,q}(s_k)\|_2^2 < t_{p,q} \tag{7}$$

For simplicity, you can assume that $w_{p,q,k}=1$ for all values of k, p and q. In this paper we choose $w_{p,q,k}=1/\|\hat{\mathbf{Y}}_{p,q}(s_k)\|$ to normalize the relative error. Since N may be large, Eq.(7) will lead to a very large number of constraints. Thus a more compact form is desired.

For a matrix M, let M_p denote the pth row of M and M_q denote the qth column of M. We can write the transfer function for entry (p,q) as follows.

$$\tilde{\mathbf{Y}}_{p,q}(s_k)=sY^\infty_{p,q}+D_{p,q}+C_p(s_kI-A)^{-1}B_q \tag{8}$$

Let

$$\begin{aligned} J(s_k) &= w_{p,q,k}[B_q^T(s_kI-A^T)^{-1}\ e_q^T\ se_q^T] \\ L(s_k) &= w_{p,q,k}\hat{\mathbf{Y}}_{p,q}(s_k), \end{aligned} \tag{9}$$

and define

$$F_{p,q}=\begin{bmatrix} Real\{J(s)\} \\ Imag\{J(s)\} \end{bmatrix} \tag{10}$$

$$G_{p,q}=\begin{bmatrix} Real\{L(s)\} \\ Imag\{L(s)\} \end{bmatrix} \tag{11}$$

and

$$X=[\ C \quad D \quad Y^\infty\ ], \tag{12}$$

we now have

$$\sum_{k=1}^{N} w_{p,q,k}\|\tilde{\mathbf{Y}}_{p,q}(s_k)-\hat{\mathbf{Y}}_{p,q}(s_k)\|_2^2=\|F_{p,q}X_p^T-G_{p,q}\|. \tag{13}$$

We can perform QR decomposition to the matrix

$$F_{p,q}=Q_{p,q}R_{p,q} \tag{14}$$

where R is an upper triangular matrix and Q is an orthogonal matrix satisfying $Q^TQ=I$. We can write

$$\|F_{p,q}X_p^T-G_{p,q}\|=(F_{p,q}X_p^T-G_{p,q})^T(F_{p,q}X_p^T-G_{p,q}). \tag{15}$$

Let

$$E_{p,q}=(R_{p,q}X_p^T-Q_{p,q}^TG_{p,q}) \tag{16}$$

and

$$\delta_{p,q}^2=G_{p,q}^T(I-Q_{p,q}Q_{p,q}^T)G_{p,q}, \tag{17}$$

we can rewrite Eq.(15) as

$$\|F_{p,q}X_p^T-G_{p,q}\|=E_{p,q}^TE_{p,q}+\delta_{p,q}^2. \tag{18}$$

The least square constraints Eq.(13) becomes

$$E_{p,q}^TE_{p,q}+\delta_{p,q}^2\le t_{p,q}. \tag{19}$$

Now we can write the whole convex optimization problem as

$$\begin{aligned} \text{minimize:}\quad & t(K,C,D,Y^\infty) \\ \text{subject to:}\quad & \text{Eq. (1), (2), (4)} \\ & \forall 1\le p,q\le m, E_{p,q}^TE_{p,q}+\delta_{p,q}^2\le t_{p,q} \\ & \forall 1\le p,q\le m, t_{p,q}\le t, t\ge 0 \end{aligned} \tag{20}$$

where m is the port number of the circuit. Both the objective function and the constraints are convex functions of variables t, $t_{p,q}$, K, C, D, and Y^∞.

Sometimes we need to introduce additional constraints on C, D, and Y^∞. The most common ways are likely to fix D or Y^∞ to a special value, such as zero. The fixed value must ensure that the system meets the positive real condition.

We notice that passivity enforcement was done by the compensation-based approach proposed in [1]. But this method does not ensure the accurate matching because the compensated part may have significant impacts on the frequency range that we are interested.

IV. Multi-port circuit realization

Once the new C, D, Y^∞ are obtained by the convex programming, the new passivity-enforced $\mathbf{Y}(s)$ are constructed again by Eq.(3). We now discuss how to generate realized macromodels for both frequency and time domain simulation.

A. Relaxed one-port realization

We start with one-port network realization. For a one-port model with driving-point admittance function, we propose to use a generalized Foster's canonical form based realization to directly synthesize the admittance function.

To synthesize the one-port model from the driving-point admittance rational function $Y(s)$, we first rewrite it in the Foster's canonical form [21]:

$$Y(s)=sY_\infty+Y_0+\sum_{m=1}^{M}\frac{a_m}{s-p_m}+\sum_{n=1}^{N}\left(\frac{a_n}{s-p_n}+\frac{a_n^*}{s-p_n^*}\right) \tag{21}$$

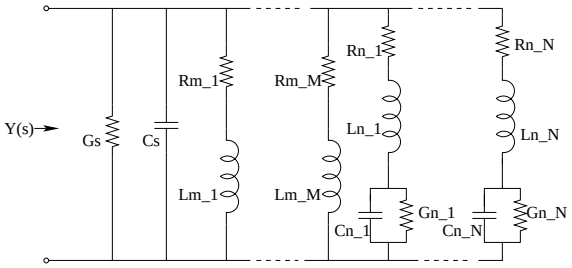

Fig. 1. One-port Foster admittance realization.

where we expand the rational function into partial fraction form with N conjugate-poles p_n and M real-poles p_m.

The admittance function in Foster's canonical-form can be then synthesized by an equivalent circuit in Fig. 1 with the following relations to determine R, L, C, G elements:

$$\begin{aligned}
&G_s = Y_0, \qquad C_s = Y_\infty;\\
&Rm_m = \frac{1}{a_m}, \qquad Lm_m = -\frac{p_m}{a_m};\\
&Ln_n = \frac{1}{2Re\{a_n\}}, \qquad Ln_nCn_n|p_n|^2 = Rn_nGn_n + 1,\\
&\frac{Gn_n}{Cn_n} = -\frac{Re\{a_n p_n^*\}}{Re\{a_n\}}, \qquad \frac{Rn_n}{Ln_n} = \frac{Re\{a_n p_n^*\}}{Re\{a_n\}} - 2Re\{p_n\}.
\end{aligned} \tag{22}$$

Some existing works like PRIME [11], requires every complex pole pair to be physically realizable (every RCL element is positive), which is over constrained and may lead to significant error if unrealizable pole pairs are discarded or their residues are changed. In our approach, we *relax* those constraints by allowing some negative RLC elements. But the passivity of the admittance function is still guaranteed by the passivity enforcement procedure since the realization is error-free and reversible and does not change the passivity of the realized system.

B. Multiple-port realization

For passive multiple-port model order reduced admittance matrix, we propose a general complete-graph structure (in case of full admittance matrix) to realize the admittance matrix based on the one-port realization. In the following, we first illustrate how 2-port network are realized and then we extend this concept for general n-port network realization.

Given a 2×2 passive model-order reduced network, its admittance matrix can be obtained via hierarchical model order reduction method.

$$Y_{2\times 2}(s) = \begin{bmatrix} y_{11}(s) & y_{12}(s) \\ y_{21}(s) & y_{22}(s) \end{bmatrix}, \tag{23}$$

it can be realized exactly by using the Π-structure template shown in Fig. 2, where each branch admittance will be realized by the one-port Foster's expansion method shown in Fig. 1. Based on this template, such a realization can be easily extended to multi-port case.

$$Y_{n\times n}(s) = \begin{bmatrix} y_{11}(s) & \cdots & y_{1n}(s) \\ \vdots & \ddots & \vdots \\ y_{n1}(s) & \cdots & y_{nn}(s) \end{bmatrix} \tag{24}$$

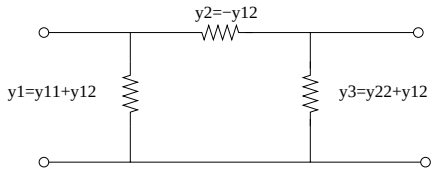

Fig. 2. A general two-port realization Π model.

Generally, for a reduced n-port network with a full $n\times n$ admittance matrix as shown in Eq.(24), the realized network will be a complete graph where each branch represents an admittance, which is realized by one-port realization method. For instance, Fig. 3 shows an realization of a synthesized 6-port network. The branch admittance of the mth port branch (the branch between the port and ground) is the sum of all the mth row admittances, and the admittance of the branch between the port and any other port is its negative value of the corresponding admittance.

Notice that our realization structure works for symmetrical admittance matrices, which are always the case for linear passive circuits with RLCM elements.

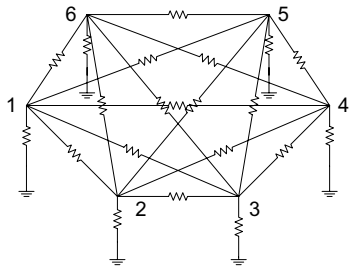

Fig. 3. A six-port realization based on Π-structure.

V. Experimental Results

The proposed algorithm has been implemented using C++ and MATLAB. CPU times are collected on a PC with P-IV 3.0Ghz CPU and 512MB RAM. We present the results on two examples.

The convex programming problem is solved using the some standard optimization packages. We use SeDuMi [19] and SeDuMi Interface to solve the convex programming problem in our passivity enforcement problem. SeDuMi is powerful software package add-on for MATLAB, which lets you solve optimization problems with linear, quadratic and semidifinite constraints.

The first example is the 2-bit bus with 20 segments. The original PEEC model contains 42 resistors, 63 capacitors, 40 self-inductors, and 760 mutual-inductors, where we consider inductive coupling between any two segments including those in the same line. For mutual inductance, a vector potential equivalent model (VPEC) is used [22], which is more hierarchical reduction friendly as not coupling inductor branch currents are involved and circuit partitions can be done easily.

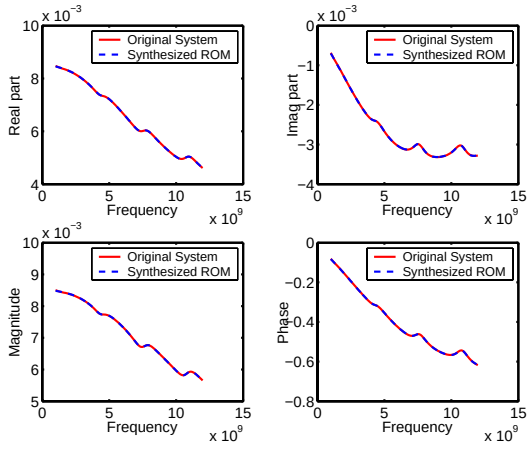

Fig. 4. Frequency Responses of Y_{11} of Bus2×20 Circuit.

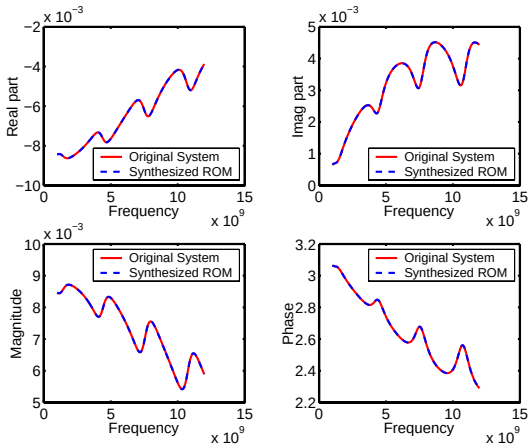

Fig. 5. Frequency Responses of Y_{12} of Bus2×20 Circuit.

We first perform the multi-point hierarchical model order reduction up to 12Ghz, which result in 20 dominant poles for admittances in the resulting 2×2 reduced matrix. Using the 2×2 template in Fig. 2, 10 stages admittance circuit shown in Fig. 1 are used for each branch in Fig. 2. The total RLC elements in the synthesized circuit is 126, which represent 83.8% reduction ratio. The resulting waveforms in frequency domain and comparison with the original waveforms are shown in Fig. 4 and Fig. 5 for $Y_{11}(s)$ and $Y_{12}(s)$ respectively. As you can see, the synthesized circuit matches the original circuit perfectly up to the 12Ghz in all aspects of the frequency responses.

We also compare the waveforms of the synthesized circuit with that of the original one in time domain. A pulse input is added at one of the bus circuits and we look at the responses at the other end of the bus circuits. The waveforms are shown in Fig. 6. The two waveforms match very well. But the synthesized model gives 48X speedup over the original circuit.

The second example is a 2-bit transmission line network. Also PEEC model circuit is first extracted and VPEC models are used for mutual inductors. The matching frequency is up to 31Ghz and we find 24 dominant poles in this range.

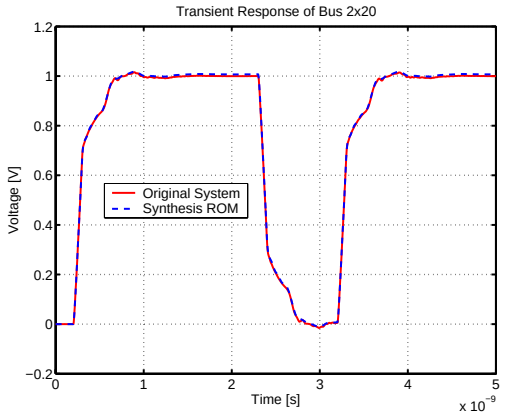

Fig. 6. Transient Responses of Bus2×20 Circuit.

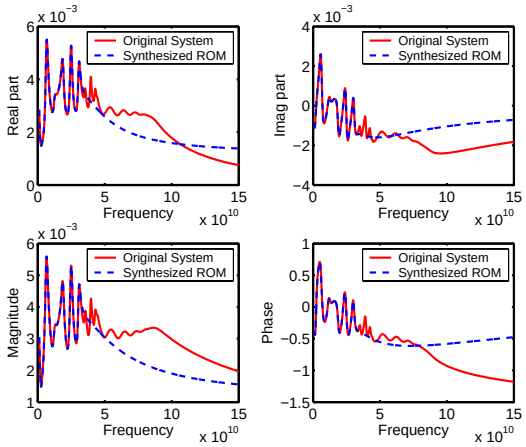

Fig. 7. Frequency Responses of Y_{11} of a 2-bit Transmission Line.

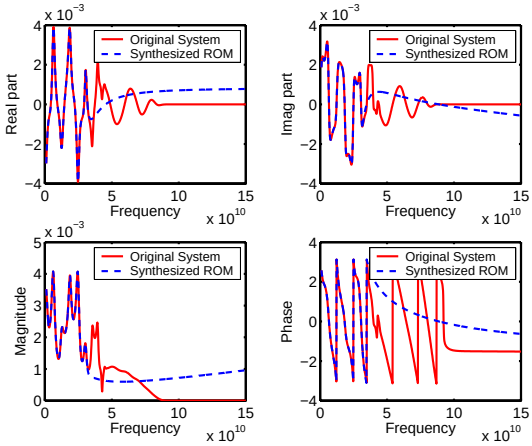

Fig. 8. Frequency Responses of Y_{12} of a 2-bit Transmission Line.

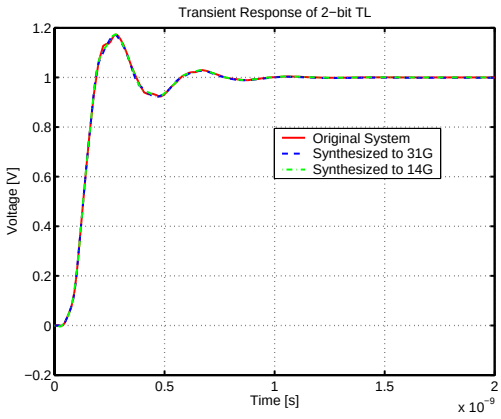

Fig. 9. Transient Responses of a 2-bit Transmission Line.

There are 150 RLC elements in the synthesized circuit compared with 364 devices in the original circuit, which represent 58.79% reduction rate. The frequency response for $Y_{11}(s)$ and $Y_{12}(s)$ are shown in Fig. 7 and Fig. 8 respectively. If we only match to 14G, 12 poles are required and we can achieve 78.5% reduction rate instead. The time domain step responses from the original one, the 14Ghz synthesized circuit and the 31Ghz synthesized circuit are shown in Fig. 9. The difference among these three circuits are fairly small.

VI. Conclusion

In this paper, we have presented a novel passive RLCM circuit modeling and realization technique for high-performance RF passives and interconnects compact modeling. The proposed method combines the general multi-port *s*-domain hierarchical modeling with state-space based optimization technique to realize passive multi-port RLC compact circuits. To realize the passivity-enforced admittance, we have proposed a general multi-port network realization method based on relaxed one-port network synthesis technique and Foster's canonical form network realization method. The resulting model order reduction flow takes the RLCM *SPICE* netlist in and produces the RLC *SPICE* netlist out, which makes the generated models very portable and flexible to be incorporated with other simulation tools. The experimental results on a number of PEEC modeled bus lines circuits demonstrate the effectiveness of the proposed algorithm.

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