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Invited Paper

Interconnect Electromigration Modeling and Analysis for Nanometer ICs: From Physics to Full-Chip

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Abstract: In this article, we will present recent advances in VLSI reliability effects with a focus on electromigration (EM) failure/aging effect on interconnects, which is one of the most important reliability concerns for VLSI systems especially at the nanometer regime. *One of the most important advances for EM analysis in recent years is the recognition that EM failure analysis can't depend on single wire segment anymore, as done in the traditional Black and Blech's based methods. New generation of EM modeling and design must consider all the wire segments in an interconnect as the hydrostatic stress in those wire segments affect each other.* Such recognition bring both challenges and opportunities. We will start with physics-level stress-oriented characterization of EM failure effects and recently proposed three-phase EM models. Then we present a new EM immortality check at the circuit level considering multi-segment interconnects and void saturation volumes. After this, we will present how to accelerate EM aging effects for fast EM validation at the circuit level under normal working conditions using advanced structure-based techniques. Finally, we will present new EM sign-off analysis tool, called *EMspice*, at the full-chip power grid level considering the interplays between resistance changes from post-voiding processes and current density changes from power grids over the aging process. A number of other relevant works will be reviewed and compared as well.

Keywords: interconnect, reliability, electromigration, power grid networks

1. Introduction

Electromigration (EM) induced aging and failure effects remain a top reliability concern for modern VLSI chips in the nanometer regime. It is expected that the future chips would show signs of reliability-induced aging much faster than previous generations. The International Technology Roadmap for Semiconductor (ITRS 2015) [1] shows that if the current densities keep increasing due to the technology scaling, designers will run into serious EM reliability issues as shown in **Fig. 1**.

To mitigate such *EM crisis*, in addition to the innovation at material and fabrication levels, more accurate modeling and EM-aware cross-layer design and optimization at circuit and system levels can also come to the rescue [2]. However, it is well accepted that existing Black and Blech-based EM models are subject to growing criticism due to over conservativeness and they only work for a single wire segment [3], [4]. Therefore, it is important to develop more accurate and less conservative EM sign-off and validation techniques [5].

To mitigate the existing problem in EM models, a number of physics-based EM models and assessment techniques have been proposed recently [2], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22]. These EM models are primarily based on the hydrostatic stress diffusion kinetics in the confined metal wires and therefore have a more accurate time to failure estimation for general multi-segment interconnect wires over a wide range of stress conditions.

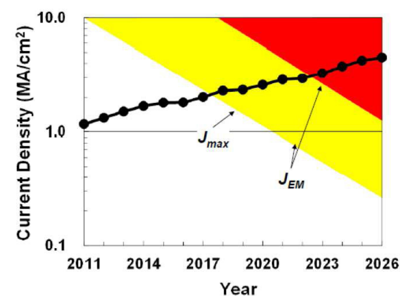

Fig. 1 Evolution of current densities: J_{max}, the maximum equivalent DC current density and J_{EM}, the current density for targeted lifetime [1].

One of the most important observations and advances from those EM modeling investigations is that EM failure analysis can't depend on single wire segments any more, as done in the traditional Black and Blech's based methods [3], [4]. New generation of EM modeling and design must consider all the wire segments in interconnect tree in a same layer of metallization as the hydrostatic stress in those wire segments affect each other. **Figure 2** illustrates a multi-segment interconnect tree representing continuously connected, highly conductive metal lines within one layer of metallization, terminated by diffusion barriers and vias. The EM modeling and failure assessment

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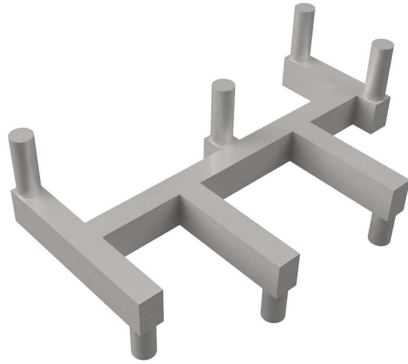

Fig. 2 A multi-segment interconnect tree of one layer metallization.

for multi-segment interconnect wires bring both challenges and opportunities. On one hand, the computing costs for EM assessment and analysis becomes more expensive as one needs to solve the resulting partial differential equation (PDE) (called Korhonen's equation) of hydrostatic stress evolution in the confined multi-segment wires subject to blocking material boundary conditions [14], [15], [17], [20], [22]. On the other hand, designers can exploit the geometrical, structure and topological impacts on the hydrostatic stress of different wires to engineer a expected EM failure processes for different applications such as EM-aware physical design and optimization [23], EM aging acceleration for fast EM validation [21], EM-based aging sensor designs [24], [25] and EM-aging based hardware Trojan design and prevention techniques [26].

In this review article, we will summarize some of recent major advances for physics-based EM modeling and assessment works in the past few years. We want to point out recent excellent survey work for similar topics in Refs. [2] and [5]. As a result, instead of trying to be comprehensive, which requires a new book treatment of this topic, we would like to highlight a few important research efforts since those survey works have been published. We note that the lack of coverage of some related works does not diminish their significant contributions.

Specifically, in Section 2 we review the basic EM physics and stress-based EM modeling. Then we show the latest three-phase compact EM models for both single wire segment and multi-segment wires, which form the foundation for advanced EM models. Section 3 reviews the new voltage-based EM immortality check for multi-segment wires for void nucleation phase and Section 4 reviews the new EM immortality check for incubation phase with a fast saturation void volume estimation method. Section 5 covers a recently proposed EM acceleration technique based on multi-segment structures. Section 6 describes a new coupled EM and IR drop analysis tool, *EMspice*, for full-chip power grid level EM sign-off analysis. Source codes and documents of *EMspice* can be downloaded at Ref. [27]. Section 7 summarizes other recent EM modeling and analysis works proposed recently. Finally, Section 8 concludes this article.

2. EM Physics and Three-phase EM Modeling

2.1 EM Physics and Stress-based EM Modeling

EM is a physical phenomenon of the migration of mental atoms

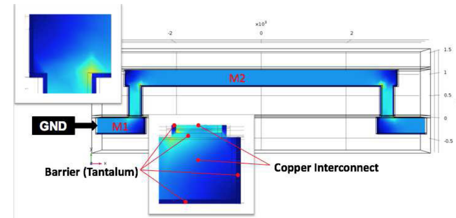

Fig. 3 Up-stream structure with electron flux flow from M1 to upper M2 through cathode node.

along the direction of the applied electrical field. Atoms (ether lattice atoms or defects/impurities) migrate along the trajectory of conducting electrons. During the migration process, hydrostatic stress is generated inside the embedded metal wire due to momentum exchange between lattice atoms. Overtime, void and hillock formation is caused by conducting electrons at the opposite ends of the wire. Indeed, when metal wire is passivated into a rigid confinement, which is the case for copper dual damascene structure, the wire volume changes (induced by the atom depletion and accumulation due to migration), and creates tension at the cathode end and compression at the anode end of the line [28], [29], [30]. EM can degrade both global interconnects such as power grid networks and local signal wires when the current densities are sufficiently high (about $1\,\mathrm{MA/cm^2}$). However, the power grid networks are more susceptible to EM effects due to the conduction of unidirectional currents.

Figure 3 shows the typical copper dual damascene interconnect structure, where the electron flows from the GND node (M1) to the testing metal wire M2. This is called upstream structure. In this structure, metal 2 (M2) is passivated into the Ta barrier layer. The top of the metal is covered by the capping layer using material such as SiN. As time goes on, the lasting unidirectional electrical load will increase hydrostatic stress, as well as the stress gradient which acts as a counter-force for atomic migration along the metal line. Generally when a line is long, this stress can reach a critical level, resulting in a void nucleation at the cathode and/or hillock formation at the anode end of line.

Mathematically, transient hydrostatic stress evolution due to EM effects in confined metal $\sigma(x,t)$ can described by Korhonen's equation [31]. Specifically, if we consider a simple line wire of length l with the blocking boundary conditions at the two blocked ends located at $x = 0$ and L and constant initial condition:

$$\begin{aligned}
&\frac{\partial\sigma(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial\sigma(x,t)}{\partial x} + G\right)\right],\ 0 \le x \le L, t > 0\\
&BC: \frac{\partial\sigma(0,t)}{\partial x} = -G, \qquad t > 0\\
&BC: \frac{\partial\sigma(L,t)}{\partial x} = -G, \qquad t > 0\\
&IC: \sigma(x,0) = \sigma_T
\end{aligned} \tag{1}$$

where, $\kappa = D_a B\Omega/kT$, and $D_a = D_0 exp(-\frac{E_D - \Omega^*\sigma_T}{k_B T})$ is the effective atomic diffusivity where E_D is the activation energy of the atom diffusion, T is the absolute temperature, k is the Boltzmann constant, B is the effective bulk elasticity modulus and $G = \frac{eZ\rho j}{\Omega}$, where e is the electron charge, eZ is the effective charge of the migrating atoms, Ω is atomic volume, ρ is the wire electrical resistivity, and j is the current density. σ_T is the thermal stress

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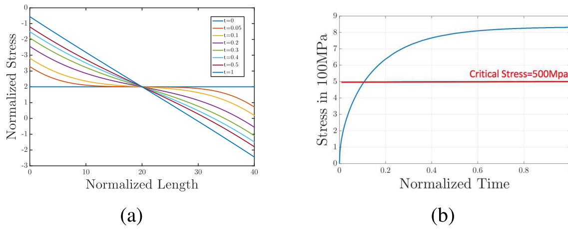


(a) (b)

Fig. 4 (a) EM-stress distribution change over time in a simple metal wire. (b) EM-stress evaluation versus time.

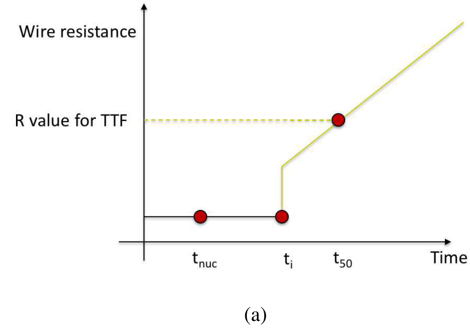
developed in the metal line during cooling from the zero stress temperature T_{ZS} down to the temperature of use condition.

Figure 4 (a) shows stress development over time in a metal line with Korhonen's equation. Over time, tensile (positive) stress will develop at the cathode (left) node and compressive (negative) stress will develop at the anode (right) node. The stress changes polarity in the middle of the wire. The built-up stress (its gradient) will serve as the counter force for atomic flux. Figure 4 (b) shows stress evolution on the cathode, which reaches a steady-state over time. If the highest stress at the cathode node exceeds the critical stress, voids will be created. The time to reach the critical stress is called nucleation time(t_{nuc}). After the void is nucleated, it will begin to grow, consequently raising the wire resistance.

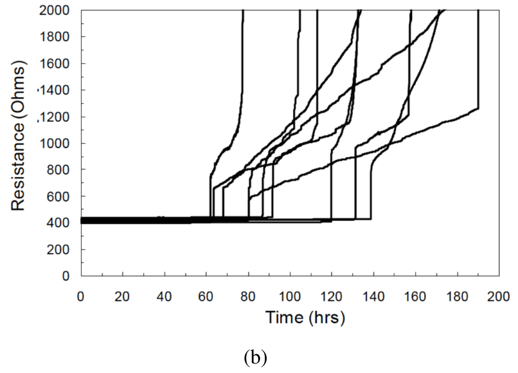
2.2 The Three-phase Physics-based Compact EM Model for Multi-segment Wires

As mentioned above, the EM failure process in general can be viewed as two phases: the nucleation phase, in which void is generated after the critical stress is reached, and the growth phase, in which void starts to grow. Existing compact EM models are also versed in terms of the two phases, where each phase is described by time-to-failure as a function of current density and other parameters [9], [32]. However, such a simple EM model ignores the fact that when the void is nucleated or formed, it will not change the wire resistance immediately. It is observed experimentally that there exists a so-called *critical void size* [33], [34], which is typically the via-diameter or cross section area of the interconnect wire. Since the conductivity of Cu is much higher than the barrier layers, resistance of the wire does not change until the void grows to a point where its volume equals or becomes larger than the cross-section of the via or wire. Only then will all the current start to flow over the thin barrier layer, which will lead to a very high current density and consequent joule heating. The joule heating in turn will lead to a small resistance jump, indicating the end of this phase. **Figure 5** (b) shows the experimentally measured resistance change over time. Here, the small resistance jumps are clearly visible. Also, sometimes the barrier layers are not very stable, due to manufacturing process variations, causing the barrier layer to quickly burn out resulting in an open circuit as is shown in Fig. 5 (b) [34].

Based on these observations, a three phase EM model has been proposed for a single segment wire [2]. In the new model, we have three phases as shown in Fig. 5 (a): (1) the *nucleation phase* from $t = 0$ to t_{nuc}; (2) the *incubation phase* from t_{nuc} to the t_i; and (3) the *growth phase* starting from t_i to t_{50}, t_{50} together indicate



(a)



(b)

Fig. 5 (a) The proposed 3-phase EM model and the resulting resistance change over time, courtesy of Ref. [2]. (b) Measured resistance change, courtesy of Ref. [34].

the time-to-failure in statistical terms (50% of the samples fail). In this paper, we extended this 3-phase EM model to consider multi-segment wires.

In the **nucleation phase**, a void is not formed until time t_{nuc}, hence the resistance does not increase. Here, the stress can be modeled by Korhonen's equation in Eq. (1) and the nucleation time can be estimated by solving the Korhonen's equation based on finite element or finite difference methods [35].

In the **incubation phase**, which is defined by the time period from t_{nuc} to the t_i, the void is nucleated, but its size is not significant. Hence the resistance will remain almost the same. The incubation time($t_i - t_{nuc}$) can be estimated as

$$t_i - t_{nuc} = \frac{\Delta L_{crit}}{v_d} \tag{2}$$

Here ΔL_{crit} is the length of critical void size and v_d is the void's growth rate. For a single segment wire, v_d is related to atomic flux (J) as $v = \Omega J$ [36], where Ω is atomic volume. Atomic flux J is the number of atoms crossing a unit area per unit time. Thus, the atoms crossing per unit length can be expressed as JW. $J = \frac{D_a f}{\Omega k T}$, where f is electron wind force per atom: $f = eZ\rho j$.

For a multi-segment tree, all segments connected with the void can contribute to the void growth. Electron wind at each segment can accelerate or slow down the void growth based on their directions. So total atom flux can also be expressed as a combination of all the fluxs on the segments. For multi-segment wires, the effective atomic flux per unit length $v_d W_m$ is the void growth rate on the main segment which can be expressed as

$$v_d = \Omega J_m^* = \Omega \frac{1}{W_m} \sum_i J_i W_i = \frac{D_a e Z \rho}{kT W_m} \sum_i j_i W_i \tag{3}$$

Here j_i and W_i are the current density and width of the ith seg-

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ment. W_m is the width of the main segment where the void is formed and J_m is the total flux impact on the main segment. Here, we use $J_m^* = \frac{1}{W_m}\sum_i J_i W_i$ to compute the effective atomic flux J_m on the main segment. Note if we only have one segment, then $v_d = \frac{D_a eZ\rho j}{kT}$ as shown in Ref. [33].

Finally, in the **growth phase**, defined by time period from t_i to t_{50}, the void reaches its critical size and blocks the cross section above the via, forcing the current to flow through the liner or barrier layers. Since this liner is very thin, and its resistivity is much larger than copper, the current density and resistance on the linear will be very high. At this point, resistance of the wire will continue to increase over time after a small resistance jump due to joule heating [37]. Hence, given incubation time t_i and v_d in Eq. (3), the time and the resistance change can be expressed as Ref. [6]:

$$t - t_i = \frac{\Delta R(t)}{v_d[\frac{\rho_{Ta}}{h_{Ta}(2H+W_m)} - \frac{\rho_{Cu}}{HWm}]} \quad (4)$$

where ρ_{Ta} and ρ_{Cu} are the resistivities of the (barrier) liner material (Ta for instance) and copper respectively, W_m is the line width of the segment where void is formed (main segment), H is the copper thickness, and h_{Ta} is the liner layer thickness.

One important aspect in both incubation and growth phases is that the void volume will saturate in steady state. If saturation happens before critical void size is reached, the wire can still be rendered as immortal. As a result, determining the void's saturation volume is critical. While there are methods of determining the saturation volume, they are limited to 2-segment wires, which is not practical for real interconnect structures. In the following section, we propose a new method of computing the void saturation volume for general multi-segment interconnects.

3. EM Immortality Check for Nucleation Phase

EM immortality check is an important part of EM validation and sign off step in the design flow. In this section, we review recently proposed voltage-based EM immortality check for multi-segment interconnects for nucleation phase [11], [16].

The traditional method mainly focuses current density on each individual wire segments. Specifically, if the critical stress that the wire can withstand is σ_{crit} and σ_{init} is the initial stress, we can define the critical product for EM failure as

$$(jL)_{crit} = \frac{\Omega(\sigma_{crit} - \sigma_{init})}{eZ\rho} \quad (5)$$

which is called the *Blech limit* or *Blech product* [4]. Ω is the atomic lattice volume, e is the electron charge, eZ is the effective charge of the migrating atoms, ρ is the wire electrical resistivity, and j is current density.

A wire is immortal for EM if it satisfies $jL < (jL)_{crit}$. As a result, the Blech product can help identify all the immortal wires efficiently.

However, recently study shows that we have to consider all the wire segments in a interconnect tree together [5]. Sun et al. recently proposed voltage-based immortality check for multi-segment interconnect [16]. Specifically, for a given arbitrary interconnect tree with N nodes, assuming the voltage in node i is V_i and the ground node is g and $V_g = 0$, then the stress at the node i can be computed as

$$\sigma_i = \frac{eZ}{\Omega}(V_E - V_i) \quad (6)$$

where A is the total area of the wire segments and V_E is defined as the *EM Voltage*,

$$V_E = \frac{1}{2A}\sum_{k\neq g}^{N} a_k V_k \quad (7)$$

where a_k is the total area of the branches connected to the node. Given the *Critical EM Voltage, $V_{Crit,EM}$*, defined as

$$V_{crit,EM} = \frac{\Omega}{eZ}(\sigma_{crit} - \sigma_{init}) \quad (8)$$

then EM immortality check for node i becomes

$$V_{crit,EM} > V_E - V_i \quad (9)$$

Since we only need to look at the node with lowest voltage, the ground node or cathode node of the whole tree, as a result, Eq. (9) can be simplified to $V_{crit,EM} > V_E$. If this EM check fails, then transient EM analysis will be carried out to find the void location and the nucleation time.

However, this voltage based method did not consider the Joule heating from the interconnects. Recently, Abbasinasab et al. considered the Joule heating effects and provided a voltage based model to perform EM reliability check [18]. In this method, the node voltage has need to be adjusted by the temperature of the wire segment. Specifically, for an interconnect tree, we define

$$V_i^T = V_i - \frac{Q}{Ze}\ln(T_i) \quad (10)$$

$$6V_E^T = \frac{1}{A}\sum_{i\in B}\left(V_{0i} - \frac{Q}{Ze}\ln(T_{0i})\right)A_i \quad (11)$$

where Q is the specific heat of transport, V_{0i} is the average voltage of two end nodes and T_{0i} is the geometrical average of temperature of the same two end nodes in the ith segment respectively, A_i is the area of the ith line, A is the total area of all lines, V_i and T_i are the voltage and temperature at node i, respectively, V_E^T is the EM voltage for the whole tree, and V_i^T is effective voltage considering temperature at node i. B is the set of all the branches or segments in the interconnect tree.

Given the same critical voltage definition in Eq. (8), then the EM immortality check becomes

$$V_{crit,EM} > V_E^T - V_i^T \quad (12)$$

However, the temperature of each segment from Joule heating is computed separately, which leads to some accuracy loss.

4. EM Immortality Check for Incubation Phase

For multi-segment interconnects, recent study shows that a wire can still be immortal even if has void nucleation. The reason is that void volume may not reach the critical volume (to manifest the resistance changes) before it reaches the steady state (so-called saturation volume). As a result, estimating the saturation

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volume of a void for multi-segment wire becomes important for post-voiding EM immortality check.

Recently a saturation volume based EM immortality check method has been proposed [19], which can further relax the constraint and filter out more immortal trees in order to reduce the more expensive EM transient simulation.

4.1 The Fast Saturation Volume Estimation in Incubation Phase

In the model, the saturation void volume for general multi-segment wires can be represented as following:

$$\mathcal{V}_{sat,total} = \sum_i \mathcal{V}_{sat,i} = h \times \sum_i \left(-2\sigma_{c,i} + \frac{V_i eZ}{\Omega}\right) \times \frac{L_i W_i}{2B} = h \times \sum_i \left(-2\sigma_{c,i} + \frac{j_i L_i \rho eZ}{\Omega}\right) \times \frac{L_i W_i}{2B} \tag{13}$$

where $\mathcal{V}_{sat,total}$ is the total saturation volume of a multi-segment wire, V_i, j_i, L_i, W_i are the voltage difference between anode and cathode, current density, length, and width of ith segment respectively. h is the thickness of the wire, which is the same for all the wire segments. $\sigma_{c,i}$ is the steady state stress on the cathode of segment i, which becomes 0 where the void is nucleated. We note that except for the segment with the void, steady-state stress on the cathode node of other segments are actually equal to the anode of the segment connected to them.

EM failure will not happen if cathode node can pass the immortality check since it has the lowest voltage among all the nodes on a tree. Following equation is the condition of immortality of the tree:

$$V_{crit,EM} > V_E - V_{cat} \tag{14}$$

where V_{cat} is the voltage at the cathode.

In order to illustrate this method, we use some examples. **Figure 6** is a T-intersection wire. In this case a void will be formed at node 0, stress at other nodes can be calculated as:

$$\begin{aligned} \sigma_1 &= -\frac{V_1 eZ}{\Omega} = -\frac{j_1 L_1 \rho eZ}{\Omega} \\ \sigma_2 &= \sigma_1 - \frac{(V_2 - V_1)eZ}{\Omega} = -\frac{(j_1 L_1 + j_2 L_2)\rho eZ}{\Omega} \\ \sigma_3 &= \sigma_1 - \frac{(V_3 - V_1)eZ}{\Omega} = -\frac{(j_1 L_1 + j_3 L_3)\rho eZ}{\Omega} \end{aligned} \tag{15}$$

Figure 7 shows stress at steady-state during the growth phase.

Here, the saturation void volume can be calculated as

$$\begin{aligned} \mathcal{V}_{sat,3seg} &= h \times \frac{-\sigma_1 L_1 W_1 + (-\sigma_1 - \sigma_2) L_2 W_2}{2B\Omega} + \frac{(-\sigma_1 - \sigma_3) L_3 W_3}{2B} \\ &= h \times \left(\frac{j_1 L_1^2 W_1 \rho eZ}{2B\Omega} + \frac{(2j_1 L_1 + j_2 L_2) L_2 W_2 \rho eZ}{2B\Omega} + \frac{(2j_1 L_1 + j_3 L_3) L_3 W_3 \rho eZ}{2B\Omega}\right) \end{aligned} \tag{16}$$

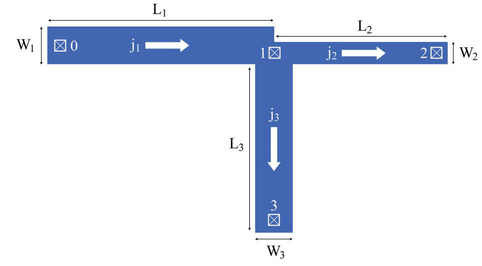

Fig. 6 A T-shaped wire (Arrows indicate electron flow) [19].

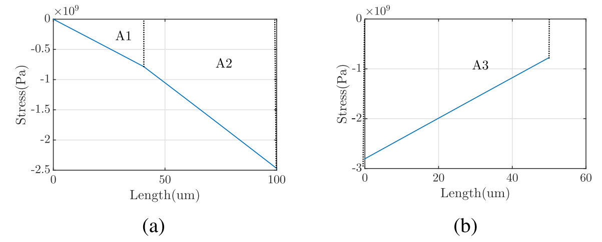

Fig. 7 (a) Stress on horizontal segment 0-2, (b) Stress on vertical segment 1-3 [19].

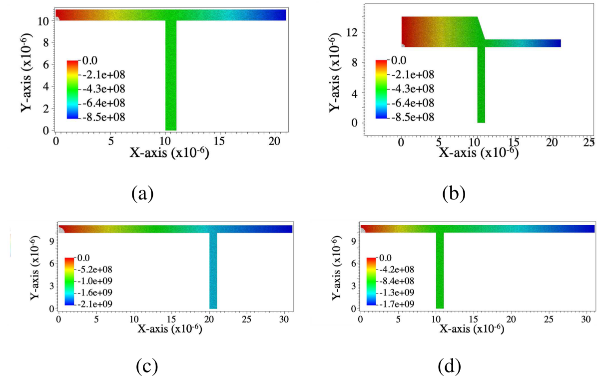

Fig. 8 (a) Case 1, (b) Case 2, (c) Case 3, (d) Case 4 [19].

Table 1 Comparison of void area of two methods (wire thickness = 0.1 um) [19].

	Case 1	Case 2	Case 3	Case 4
L_1 (um)	10	10	20	10
L_2 (um)	10	10	10	20
L_3 (um)	10	10	10	10
W_1 (um)	1	4	1	1
W_2 (um)	1	1	1	1
W_3 (um)	1	1	1	1
j_1 (A/m^2)	10^{10}	10^{10}	20^{10}	20^{10}
j_2 (A/m^2)	10^{10}	10^{10}	10^{10}	10^{10}
j_3 (A/m^2)	0	0	0	0
$\mathcal{V}_{FEM}$ (um^3)	0.0125	0.0185	0.0510	0.0368
$\mathcal{V}_w$ (um^3)	0.0121	0.0183	0.0495	0.0356

In order to validate the model, we compare the saturation volume estimate by proposed method and a physics-based 3D FEM analysis tool [17], [38] on a T-shaped three segment wire. Four test cases with their estimated void volumes generated by the FEM tool is shown in **Fig. 8**. The results of aforementioned test cases are shown in **Table 1**.

Where $\mathcal{V}_{FEM}$ is the saturation volume calculated using an FEM analysis tool, $\mathcal{V}_w$ is the saturation volume calculated using the proposed method considering the void volume effect. We can see among the four test cases in Table 1, the maximum difference is only 3.2% between $\mathcal{V}_{FEM}$ and $\mathcal{V}_w$.

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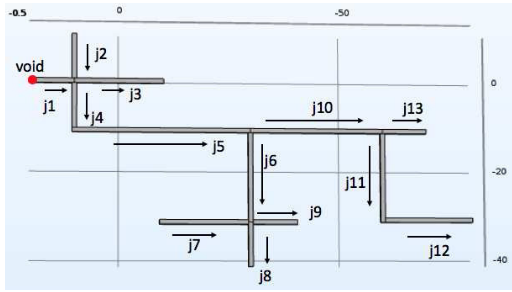


Fig. 9 A complicated multi-segment structure [19].

Table 2 Parameters used for the 13-segment interconnect wire [19].

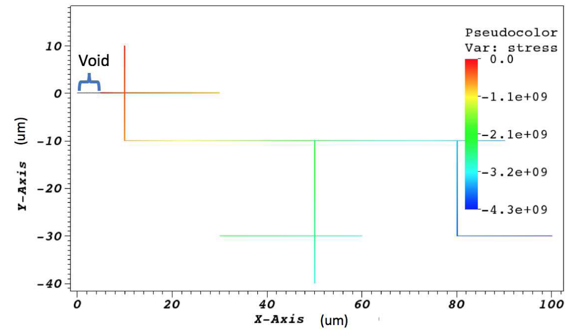
Brch#	CD (A/m^2)	Lth (um)	Brch#	J (A/m^2)	Lth (um)
1	10×10^9	10	8	15×10^9	10
2	5×10^9	10	9	5×10^9	10
3	5×10^9	20	10	10×10^9	30
4	5×10^9	10	11	5×10^9	20
5	10×10^9	40	12	5×10^9	20
6	5×10^9	20	13	5×10^9	10
7	5×10^9	20	–	–	–

In order to further validate the universality on general multi-segment wire and accuracy of the method, we compare our estimation with the FEM simulation from physics-based 3D FEM analysis tool [17], [38] on a more complicated wire structure with 13 segments as shown in **Fig. 9**. Here, the width of all the wires is 0.2 um and thickness is 0.1 um. The current densities and lengths of all the segment are given in **Table 2**, where *Brch* is branch index, *J* is current density, *Lth* is the length of the wire. Critical void volume is 0.004 um^2. As shown in the **Fig. 10**, the void is formed on *segment*1.

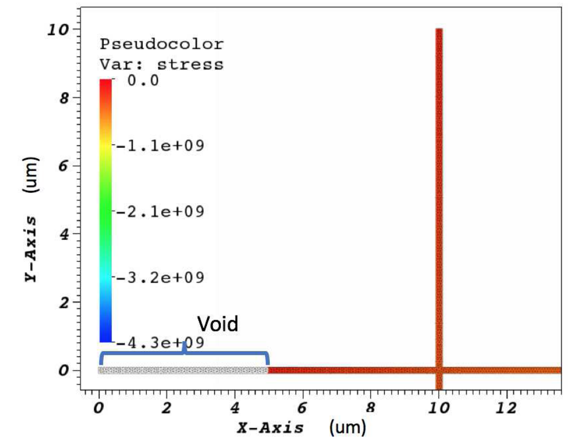
The saturation void volume estimated by the proposed method is 0.1025 um^3 while the saturation void volume calculated by FEM analysis tool is 0.1021 um^3. As we can see, the results are almost identical (about 0.39% difference). We remark that the errors for this complicated wire structure is much smaller than the previous T-shaped wire. The reason is that the saturation volumes for the T-shaped wire is small while the 13-segment wire has much larger void volume compared to the length of the wires. As a result, we obtained much smaller relative errors for the latter case.

4.2 The New EM Immortality Check Flow Considering Both Nucleation and Incubation Phases

The immortality check flow is shown in **Fig. 11**, which consists of two filtering algorithms. First, a tree in the power grid is checked by a voltage based nucleation phase filtering [11], [16] to see if voids can be nucleated. If no void can be nucleated, the wire is immortal. If voids will be nucleated, the tree is then passed to incubation phase immortality filter which is based on the aforementioned saturation void volume model [19]. If the void volume cannot exceed critical void volume, the tree is still treated as immortal. Only the mortal interconnect trees will be further analyzed for resistance changes. This new EM immortality check has been implemented in the proposed EMspice tool, which couple the EM and IR drop analysis for full-chip power grid analysis as shown in Section 6 [22].



(a)



(b)

Fig. 10 (a) Complex multi-segment structure result from FEM analysis tool. (b) The zoomed view of the void area [19].

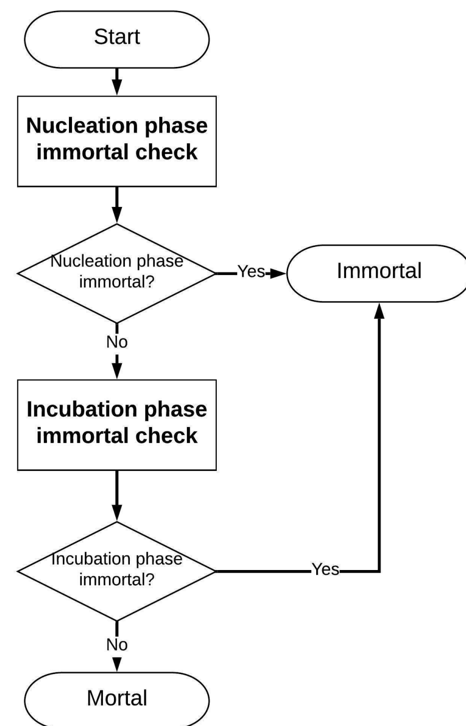


Fig. 11 The new EM immortality check flow considering both nucleation phase and growth phase immortality criteria [22].

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5. EM Aging Acceleration Techniques

Practical testing and detection of EM induced failures in dual damascene copper interconnects require stressing conditions that induce the chip to fail exclusively under EM in a very short period of time so that EM sign-off and validation can be carried out efficiently. Existing acceleration techniques, which rely on increasing temperature and current densities beyond the known limits, also accelerate other reliability effects making it very difficult, if not impossible, to test EM in isolation or in the normal working conditions. In this section, we present recently proposed structure-based EM wear-out acceleration techniques to address the aforementioned issue [21].

5.1 Configurable Reservoir based EM Failure Acceleration

Reservoir structures (passive interconnect segments) are typically added to the cathode terminal of active interconnect wires that are vulnerable to EM wear-out. These structures decrease the rate of hydrostatic stress evolution on the active wires, consequently prolonging nucleation time.

To demonstrate the impact of reservoir segments, let us consider an active interconnect segment (main-branch), with no reservoir structure, shown in **Fig. 12**. With the previously discussed three-phase EM model, transient stress across this wire segment can be computed. **Figure 15** (a) shows the hydrostatic stress evolution over time at the cathode terminal of the given wire. Only the cathode node is shown since, in most cases, void is nucleated here as the cathode end of the wire experiences the maximum tensile stress. The results for this structure show void nucleation, t_{nuc}, at 1.68×10^3 hrs. Post nucleation, the incubation and growth times are: $t_i - t_{nuc} = 1.68 \times 10^4$ hrs, and $t_{50} - t_i = 1.56 \times 10^4$ hrs. Therefore the effective time-to-failure (TTF), marked by the end of the growth phase (t_{50}) is 3.41×10^4 hrs for the interconnect wire shown in Fig. 12.

Let us now consider the effect of adding a passive reservoir segment to the cathode terminal of this wire. For now, let us arbitrarily set the reservoir to be half the length and twice the width of the active wire ($W_R = 0.1$ um and $L_R = 50$ um) as shown in **Fig. 13**. Transient stress analysis at the cathode of this new structure shows nucleation delayed to $t_{nuc} = 1.29 \times 10^4$ hrs as shown in Fig. 15 (b). Incubation and growth times stay the same since these depend on total atom flux at the cathode and at this point, only the main-branch is carrying current and therefore contributing to the effective flux. Nonetheless, delaying nucleation time prolongs the wire's lifetime to $t_{50} = 3.28 \times 10^4$ hrs. This is the typical application for reservoir segments.

Interestingly, if we design the structure shown in Fig. 13 such that current in the reservoir segment can be activated during runtime, we can exploit a very unique property. Let us consider the structure shown in **Fig. 14**, which is identical to the structure in Fig. 13 but with current flow enabled in the reservoir segment. Let us arbitrarily set the current density in the reservoir segment (Disabled Reservoir) to be the same as the main-branch, but in the opposite direction. We call this a disabled reservoir since this configuration effectively disables the benefits of the reservoir segment, shifting nucleation time back to what was originally observed from the structure in Fig. 12. This acceleration in nucleation time is shown in Fig. 15 (c). Moreover, the additional atom flux generated by the electron flow in the reservoir segment also accelerates the incubation and growth times: $t_i - t_{nuc} = 1.41 \times 10^3$ hrs and $t_{50} - t_i = 5.19 \times 10^3$ hrs. The effective TTF now becomes $t_{50} = 8.28 \times 10^3$ hrs. This is a significant reduction in lifetime achieved, at nominal current density and temperature, by merely switching on current flow in the reservoir segment. This critical observation is the basis for our reservoir-enhanced EM acceleration technique.

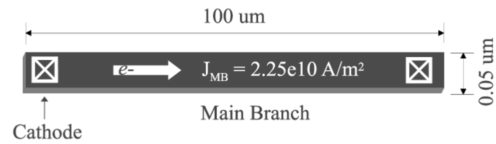

Fig. 12 Active interconnect wire segment [21].

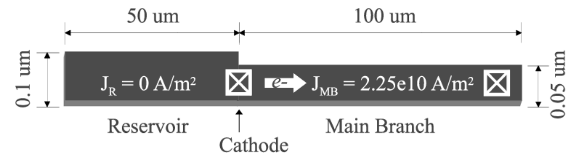

Fig. 13 Reservoir at the cathode of an active interconnect wire [21].

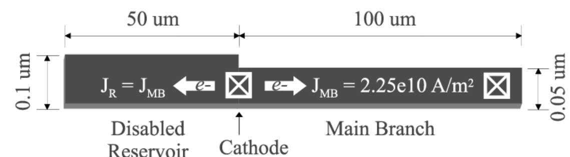

Fig. 14 Disabled reservoir at the cathode of an active interconnect wire [21].

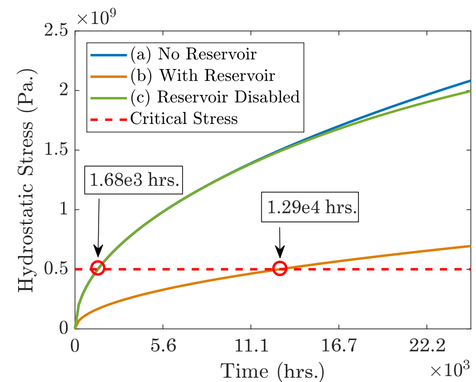

Fig. 15 Impact of reservoir on nucleation time [21].

Based on this analysis, a configurable two-segment interconnect structure shown in **Fig. 16** was proposed in Refs. [21], [39]. The structure consists of a two segment wire (one reservoir and one main-branch), one MOSFET device (switch to disable the reservoir) and two resistors R_1 and R_2 to configure the currents in the two wire segments. The bottom half of Fig. 16 shows the 3D view of this design. During normal use, the reservoir will remain passive (zero current density). Once acceleration ($Acc.Signal$) is activated, the current density in the reservoir will become nonzero, thus disabling the reservoir and accelerating EM wear-out.

Furthermore, we can design a configurable three-segment in-

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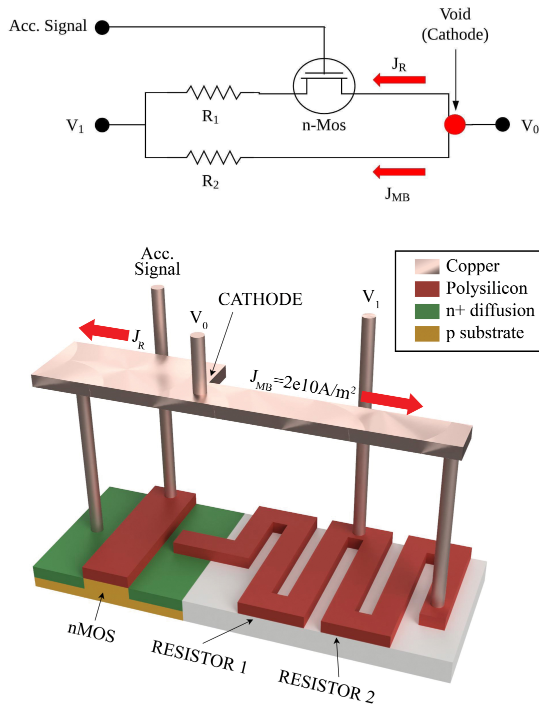


Fig. 16 The configurable reservoir-based EM wear-out acceleration circuit [21].

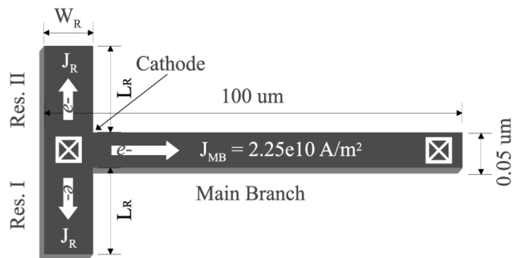
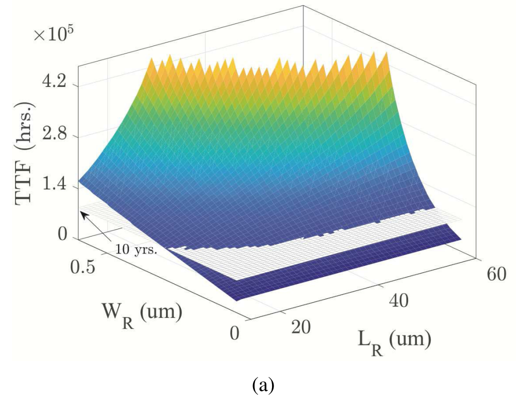


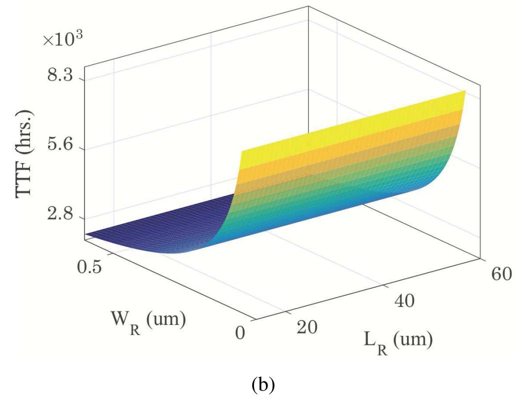
Fig. 17 Proposed EM acceleration structure with two reservoir segments [21].

terconnect structure shown in **Fig. 17**. The structure consists of a two reservoir segments (Res I and II), and one main-branch. The proposed structure will be designed to operate under two modes: normal use and acceleration. The configurable nature of the proposed structure allows for optimization between geometry, and current density, to achieve the desired lifetimes under normal use and acceleration modes. Under normal use (no current in reservoir), it is typical to ensure that the structure will have a lifetime of at least 10 years (or as needed for the given application). Under acceleration (current enabled in reservoir), we want the structure to fail quickly (typically within days or hours). Hence, the goal is to find a configuration (W_R, L_R) that will meet these requirements.

Traditionally, current density of the main branch, J_{MB}, is significantly increased to achieve EM acceleration. However, this method also accelerates other reliability effects and, above a certain threshold, leads to joule-heating causing additional problems. Hence, we will fix J_{MB} to be the same under both normal use and acceleration modes. For acceleration mode we will simply activate current in the reservoir such that $J_R = 0$ becomes $J_R = J_{MB}$.



(a)



(b)

Fig. 18 TTF_{LF} (a) Normal use, (b) Acceleration mode [21].

Indeed, J_R can be set higher than J_{MB} as long as it abides by the design rules (i.e., Synopsys 32nm PDK [40]).

As shown in **Fig. 18**, the proposed structure gives the circuit designer a great deal of flexibility in achieving the desired TTF for the application at hand. For instance the configuration W_R = 0.3 um and L_R = 18 um results in t_{nuc} = 8.31 × 10^4 hrs, $t_i - t_{nuc}$ = 4.17 × 10^3 hrs, and $t_{50} - t_i$ = 1.56 × 10^4 hrs (TTF ≈ 11.7 years) under normal use, and t_{nuc} = 1,440 hrs, $t_i - t_{nuc}$ = 325 hrs, $t_{50} - t_i$ = 1,197 hrs (TTF ≈ 123.5 days) under acceleration mode. TTF can be reduced a little further with larger reservoirs, for instance the configuration W_R = 1 um and L_R = 18 um results in t_{nuc} = 1,427 hrs, $t_i - t_{nuc}$ = 103 hrs, $t_{50} - t_i$ = 381 hrs (TTF ≈ 79.6 days). However, bear in mind, this was achieved at a working temperature of 353K (~80°C), this structure under burn-in conditions will yield a failure time that is much lower.

5.2 Configurable Sink based EM Failure Acceleration

Atomic sinks can be passive or active interconnect structures that, when added to the anode terminal of an active interconnect wire, can significantly increase the steady state tensile stress at the cathode. Additionally, adding a sink segment can reduce the compressive stress at the anode node, hence reducing the chance of hillock formations or extrusions.

Let us consider the structure shown in **Fig. 19** (a) where L_{MB} = 5 um, W_{MB} = W_S = 0.05 um, L_S = 95 um and J_{MB} = J_S = 2.25 × 10^{10} A/m^2. This structure is indeed identical to the single main-branch that was shown in Fig. 12, but this time split into two segments. We will now refer to the first segment as

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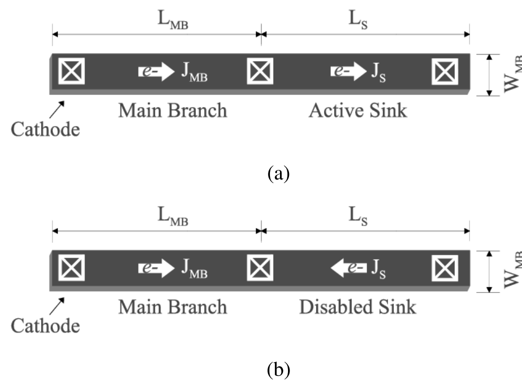

Fig. 19 Active interconnect wire with: (a) an active sink at the anode, (b) disabled sink at the anode [21].

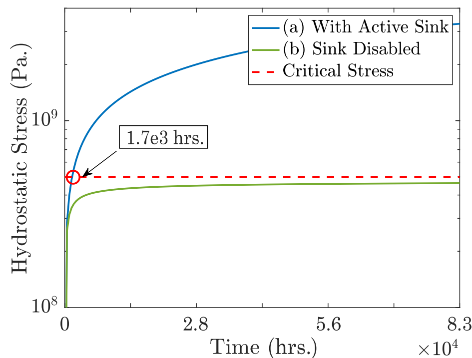

Fig. 20 Hydrostatic stress progression at the cathode with: (a) an active sink at the anode, (b) a disabled sink at the anode [21].

the main-branch and the second segment as the active sink. As expected, hydrostatic stress evolution over time at the cathode terminal (**Fig. 20** (a)) of the structure in Fig. 19 (a) is identical to what was previously observed for the structure in Fig. 12.

However, if we can design this structure such that the direction of current in the sink segment can be reversed during runtime, then we can effectively disable the impact of the sink segment, hence significantly reducing the tensile stress at the cathode (Fig. 20 (b)). Note, sink structures behave very differently than reservoir structures. While reservoirs affect both steady-state and transient stress, sink structures only affect the steady-state. This is a critical distinction that should be noted.

Sadiqbatcha et al. proposed two methods to trigger the wire to fail [41]. In the first method, an active wire segment is converted to a passive sink, where as in the second method, a passive sink is converted to an active sink. This approach was revised in Ref. [21], effectively combining the two methods, turning an active wire segment into an active sink directly. This technique allows us to easily control the mortality of the interconnect structure during runtime simply by controlling the direction of current flow in the sink segment.

To take advantage of this behavior, we have to carefully design the structure such that the tensile stress at the cathode saturates above critical stress for acceleration (active sink), and below critical stress for normal use (disabled sink). When steady-state stress is below critical stress, the structure is immortal under EM (will never fail). Hence, unlike the reservoir based method, the sink based method requires careful tuning of three variables (main-branch length, sink length, and current density) to achieve the desired TTF under normal-use and acceleration modes.

Table 3 TTF acceleration with various sink and main-branch configurations [21].

L_{MB} (um)	L_S (um)	J (A/m^2)	TTF (hr)
100	60	2.90×10^9	2.36×10^5
50	30	4.10×10^9	1.1×10^5
30	20	6.80×10^9	4.47×10^4
20	15	1.20×10^{10}	1.84×10^4
15	10	1.60×10^{10}	1.13×10^4
10	7	3.10×10^{10}	4.53×10^3
8	6	3.80×10^{10}	3.36×10^3
7	4	5.30×10^{10}	2.25×10^3

The TTF results for various configurations are shown in **Table 3**. Note, all these configurations are carefully designed so that the structure is immortal under normal use; the results presented in the table are from when the structure is operated under acceleration mode.

6. EMspice: Full-chip Power Grid EM Check by Coupled Electronic and Stress Simulation

In this section, we present the full-chip power grid EM check using coupled electronic and stress tool, *EMspice* [22]. *EMspice* was implemented in Python and C++ is open sourced and can be downloaded at Ref. [27].

The motivation for this work is that EM-induced resistance change will alter the current densities of on-chip power grid networks, which then can further affect the stress evolution of interconnect wires and thus resistance changes. As a result, one has to consider the interplay between the two physics: the electronic and hydrostatic stress in the interconnect wires. We also shows how it can be integrated with commercial EDA tools to achieve the EM sign-off analysis.

EMspice takes power grid netlists from Synopsys ICC flow, and outputs the failed EM wires, their resistance changes and resulting IR drops of the power grids over the given aging time. The EM sign-off and check flow proposed in *EMspice* is shown in **Fig. 21**. The whole EM check flow mainly consists of four major steps: *(1) power grid generation step* from the EDA tool (Synopsys ICC), *(2) EM immortality filtering step*, *(3) coupled FDTD EM solver and linear network IR drop solver*, and *(4) EM check framework GUI*. In the first step, the power grid information is constructed from Synopsys IC Compiler (ICC) during the physical synthesis process for a specific design. In the section step, the power gird and corresponding branch current are first passed to the EM immortality filter to remove all the immortal wires. The third step is to solve the stress and IR drop of interconnect wires in a coupled way. The coupled solver consists of the finite difference time domain (FDTD) solver for EM stress analysis [15] and linear network DC IR drop solver. In the last step, all information will then be passed to the EM check framework graphical user interface (GUI) for interactive user analysis.

The immortality check flow is shown in Fig. 11 in Section 4.2, which consists of EM immortality checks for both nucleation and incubation phases as discussed in Section 3 and Section 4. As a result, only the true mortal wires whose resistance will change are simulated in the coupled EM-IR simulation.

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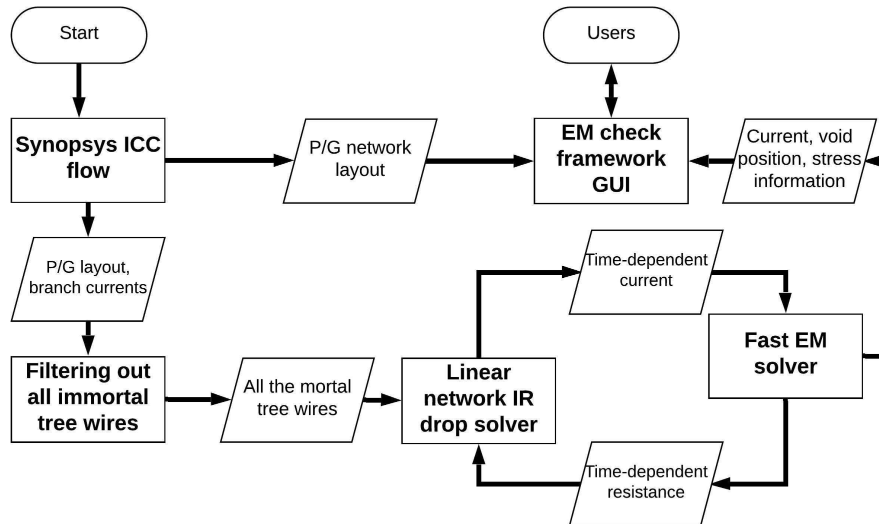

Fig. 21 Simulation Framework for *EMSpice* simulator [22].

For the third step, the coupled FDTD EM solver and linear network IR drop analysis can be described as

$$\begin{aligned} &\mathbf{C}\dot{\sigma}(t) = \mathbf{A}\sigma(t) + \mathbf{P}I(t), \\ &\mathcal{V}_v(t) = \int_{\Omega_L} \frac{\sigma(t)}{B} d\mathcal{V}, \\ &\mathbf{M}(t) \times u(t) = \mathbf{P}I(t), \\ &\sigma(0) = [\sigma_1(0), \sigma_2(0), ..., \sigma_n(0)] \text{ , } at\ t = 0 \end{aligned} \quad (17)$$

where $\mathbf{M}(t)$ is the admittance matrix for the power grid network, which is time-varying due to the fact that wire resistance will change with EM failure effects over time. $\mathbf{P}$ is the $b \times p$ input matrix, where p is the number of inputs or the size of driving current density sources $I(t)$. $u(t)$ represent the nodal voltages in the network and $I(t)$ are the current sources from the function blocks of the chips. $\mathbf{C}, \mathbf{A}$ are $n \times n$ matrices. And n is the number of nodes. Note that $\sigma(0)$ is the initial stress at time 0. For each new simulation step, the stress from previous simulation will be used as the initial condition.

The three equations are coupled and solved together as shown in **Fig. 22**. Linear network IR drop solver passes time-dependent current density information and P/G layout information to the FDTD EM solver. Once the voids are formed and IR drops in the power grid will change, the current at each time step will be different. The FDTD EM solver will provide the IR drop solver with new resistance information for wires with voids. As we can see, these two simulations are coupled together, and wire current and resistance depend on each other for each mortal wire. Note that $\mathbf{C}, \mathbf{A}$ matrices, which depend on wire structures, are time-independent in the coupled equation.

There example is to show the accuracy and effectiveness of EM check flow. **Figure 23** is the simulation result of a power grid of the Cortex-M0 DesignStart processor, named(*Cortex*). This is a 32-bit processor that implements the ARMv6-M architecture [42]. This processor is synthesized using Synopsys Design Compiler, and is placed and routed with Synopsys 32/28 nm Generic Library [43]. The power grid of *Cortex* has two layers,

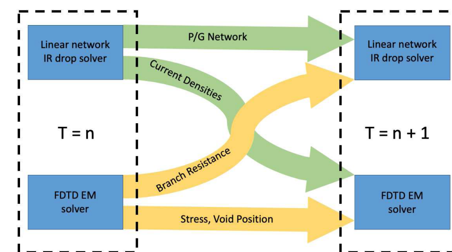

Fig. 22 Block diagram of coupled FDTD and IR drop power grid simulator [22].

Table 4 Void size comparison between *EMSpice* (FDTD) and COMSOL on a wire from *Cortex* [22].

Time after void formed	1 year	3 year	7 year
Void size from *EMSpice* (um^3)	3.63	7.38	12.04
Void size from COMSOL (um^3)	3.69	7.53	12.16
Error	1.65%	1.99%	0.98%

Table 5 Comparison of failed tree number of three methods on the power grid of *Cortex* [22].

Simulation time		8 years	12 years	20 years
Black's method	Failed tree number	24	24	24
	Failed tree percentage	35.3%	35.3 %	35.3%
Huang's method	Failed tree number	11	13	16
	Failed tree percentage	16.2%	19.1 %	23.5%
EMSpice simulator	Failed tree number	0	2	9
	Failed tree percentage	0%	2.9 %	13.2%

and there are 68 trees in total. The simulation takes about 67.14 second to finish. As can be seen from Fig. 23, after a long period of time, voids are formed in the power grid. Detailed formulation steps of voids at different time are shown in **Fig. 24**. Nucleation phase, incubation phase and growth phase of the void is shown in these three figures.

In order to show the accuracy of that method, we compare *EMSpice* against two methods: the traditional Black's method in which the time to failure is calculated for each segment based on Black's equation [3] with the same parameters used; we also employ Huang's method [9] as another baseline.

In the Black's method, tree failure only depends on the cur-

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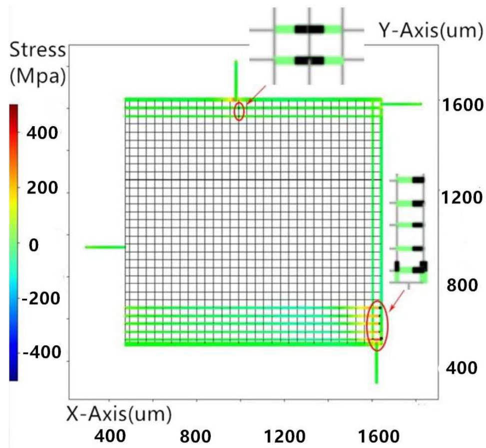

Fig. 23 20th year for *Cortex* design (X and Y in *um* and stress in *Mpa*) [22].

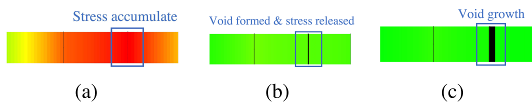

Fig. 24 (a) Zoomed stress distribution and void formation at 8th year, (b) 12th year, (c) 20th year of *Cortex* design [22].

Table 6 Lifetime comparison of the three full-chip EM analysis methods on the power grid of *Cortex* [22].

Trees name	Time to Failure (years)		
	Black's method	Huang's method	*EMSpice* simulator
Tree 1	8.33	immortal	immortal
Tree 2	4.45	9.17	immortal
Tree 3	3.08	6.16	16.67
Tree 4	2.17	4.50	14.58
Tree 5	1.67	3.67	10.41

rent densities on that tree. It cannot consider time-varying current change in the power grid. Compared with other methods, Black's method leads to the most conservative results. Around 35% of the trees in the power grid of *Cortex* are estimated to be failed by this method. Huang's method considers both nucleation phase and growth phase. But this method is still less accurate as compact models are used for both nucleation and growth phases. It marks 23.5% trees in the power grid of *Cortex* as the failed trees in the 20th year. *EMSpice* simulator shows only 13.2% failed tree wires in the power grid of *Cortex* in the 20th year. As we can see, at the 20th year, the number of failed trees by *EMSpice* simulator is 63.5% less than Black's method and 43.8% less than Huang's method in the *Cortex* case. *EMSpice* method can significantly reduce over-conservations from the existing two methods, which can lead to more aggressive design with less guard bands, which in turn leads to better performance under the same design costs.

Furthermore, we also look at the lifetime of some immortal and failed trees. Their lifetime given by the three methods are shown in **Table 6**. As we can see, *EMSpice* still gives the long lifetime estimation among the three methods for the five tree wires. The difference can be quite significant (up to 6.71X longer). Further, we observe that the immortal tree wire marked in the *EMSpice* method can be considered as mortal tree wires in both the Black's method and Huang's method. The reason is that the *EMSpice* method considers the unique incubation phase immortality case and it can identify the nucleated wires as immortal as long as their void sizes are small enough.

7. Some Other Relevant EM Models and Analysis Methods

In addition to the discussed physics-based EM models and assessment techniques in the previous sections, there are some other related work and research efforts proposed recently. Some of these have been summarized in Refs. [2] and [5]. Again, we stress that the lack of coverage of some related work does not diminish their significant contributions. In this section, we briefly mention some of these research works.

Huang et al. proposed a physics-based compact EM model for single and multi-segment wires [6], [7], [9]. This work is based on the analytic solutions of a single wire of Korhonen's equation and simplified projection into multi-segment to find the nucleation time. Chen et al. proposed analytic solutions for a number of simple wire structures like straight line, T-shaped and cross-shaped lines [8], [44]. But this method can't be applied to general multi-segment wires. Dynamic EM models considering time-varying current density and temperature changes have been proposed in Refs. [12], [13], [45]. The proposed method also can model the EM recovery effects for the first time [13]. The recovery effects can be exploited at the system level to improve the EM lifetime [46], [47], [48].

EM failure shows strong stochastic behaviors and EM impacts on the power grid and signal interconnects inside standard cells considering practical workloads, wire structure and AC currents also need detailed studies and investigations [49], [50]. Several important works were proposed recently to address those problems.

EM analysis considering both signal and power ground interconnect wires inside standard cells was studied in Refs. [51], [52]. The Joule heating effects were considered based on the root mean square (RMS) current estimation of AC currents. A equivalent EM DC current formula was proposed to consider AC current effects and signal interconnect topologies inside a cell. It was also shown that the lifetimes of the output pins in different locations can be different, which can be exploited for life time optimization for standard cells. But this work still uses the traditional Black's model.

The more detailed AC EM analysis for signal interconnect was further proposed in Ref. [53]. The effective current densities with recovery effects were considered for both ends of a wire segment under AC currents. The EM impacts on the circuit performances were assessed by a Monte Carlo based analysis based on the proposed AC EM assessment method. The result also showed that EM induced degradation can be comparable to (even larger than) major device aging mechanisms such as BTI (bias temperature instability) and HCI (hot carrier injection) in the advanced technology nodes (sub 10nm).

Work in Ref. [10] studied the solutions of the Korhonen's equation for a single wire with a finite length and with a semi-finite length. The authors showed that the solution of the finite length wire is upper bounded by that of the semi-finite wire. As a result, a hierarchical EM mortality check algorithm was proposed to find out EM-susceptible wires efficiently by using three criteria sequentially in an accuracy increasing order. The authors also

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pointed out that the existing method using one item in the solution of Korhonen's equation proposed in Ref. [6] may not be accurate for very long wires.

Further more, the EM statistical analysis of the meshed clock networks using the Monte Carlo method considering the redundant structure was studied in Ref. [54]. In addition, a framework for logic IP internal EM verification was proposed in Refs. [55], [56]. The authors tried to solve the various work load issues for designing EM safe cells or IPs for specific lifetime targets. The lifetime surface response modeling was developed by parametrized work load currents and temperature so that different lifetime goals can be targeted at design time.

Cook et al. proposed a finite difference method (FDM) based approach for solving the Korhonen's equation [35]. To speed up the transient EM analysis, fast frequency time domain technique based on Krylov subspace based model order reduction technique, called *FastEM*, has been proposed [15]. It can lead to at least two orders of magnitude speedup over plain FDM method. At the same time, a similar finite difference method for solving Korhonen's equation for power grid EM analysis was proposed in Ref. [57]. Effective filtering and predictor-based schemes were used to speed up the analysis. The proposed EM solver also considered the statistical impacts of the EM failures using the Monte Carlo method. Later on, a compact modeling of resulting discretized dynamic Korhonen's equations by reduced order modeling was further proposed to speedup the analysis [58], [59].

Recently Zhao et al. proposed a finite element method (FEM) based analysis technique for post-voiding stress analysis in 2D wire structures [17]. This approach introduces a phase field variable to explicitly model the void boundary change. The new method explicitly considers the stress distribution's impacts on the void volumes due to atomic conservation in confined wires. This work is further extended to the 3D multi-physics based FEM analysis for multi-segment interconnects in which stress, thermal and electrical field are considered and solved in a coupled way to fully capture the dynamics of void shape growth, wire resistance and temperature changes [38].

FDM and FEM analysis is very accurate, but they still cannot scale to solve very large interconnect wires. To mitigate this problems, a number of analytic and semi-analytic solutions have been studied recently. An analytic approach to solving Korhonen's equation based on an eigenfunction method was proposed in Ref. [46]. This method can give the exact solution for the stress evolution for the finite locations over time for straight multi-segment wires and work for both nucleation and growth phases. Wang et al. further proposed a more general semi-analytic solution for general multi-segment interconnect wires using separation of variables (SOV) method [48]. However, this method can still be too slow as it needs to find the eigenvalues numerically for general interconnect wires. Recently, Chen et al. proposed a more general semi-analytic solution to the Korhonen's equation for multi-segment interconnects based accelerated separation of variable (ASOV) [20]. This method proposed analytic solution to the eigenvalues for a few widely used multi-segment wire structures such as straight line and stared wire structures. Further more, it proposed more efficient numerical approaches for eigenvalue calculations than the method in Ref. [48].

A probabilistic EM analysis framework for power grids was further proposed in Refs. [60], [61]. This work considered the inherent variations from the metal micro-structures and activation energy on the wire resistances of copper dual-damascene interconnects based on a physics-based EM model of semi-infinite wires. It also was demonstrated that the power grids have inherent resilience to EM failures. Another stochastic EM analysis for power grids was also proposed using the Hermite polynomial chaos based stochastic analysis considering leakage current variations and inherent EM uncertainties [62]. A *k*th failure statistical method was used to consider the EM resilience of the P/G networks. But this method is still based on the traditional Black's model. Another work considering interplay of the thermo-mechanical stress and EM stress on the array of vias for copper wires was proposed in Ref. [63]. The work showed that a via in a via array has different lifetime due to layout dependency. Monte Carlo analysis was applied to estimate the time to failure distribution of the power grids with the via arrays.

A method for checking the EM immortality of multi-segment interconnect tree was proposed in Ref. [64]. This method can compute the steady state for each branch (their terminal nodes) so that EM immortality is checked for each branch. Recently, Abbasinasab *et al.* proposed to consider Joule heating effects of interconnects in EM analysis techniques and voltage-based EM immortality check [18], [65], [66]. Their work shows that thermal gradient impacts (called thermal migration) can be as significant as the EM effects and will get worse as technology scales. Their work can be viewed as an extension of the voltage-based EM immortality check method [11], [67] (discussed in details in Section 3) by considering the temperature gradient impacts due to Joule heating on the stress distributions of the wires.

8. Conclusion

In this article, we have presented the latest development and advances for modeling and analysis of electromigration for interconnect wires for nanometer VLSI systems.

References

[1] International Technology Roadmap for Semiconductors 2.0 (ITRS 2.0) (2015), http://www.itrs2.net/itrs-reports.html.

[2] Tan, S.X.-D., Amrouch, H., Kim, T., Sun, Z., Cook, C. and Henkel, J.: Recent advances in EM and BTI induced reliability modeling, analysis and optimization, Integration, *VLSI Journal*, Vol.60, pp.132–152 (2018).

[3] Black, J.R.: Electromigration-A Brief Survey and Some Recent Results, *IEEE Trans. Electron Devices*, Vol.16, No.4, pp.338–347 (1969).

[4] Blech, I.A.: Electromigration in thin aluminum films on titanium nitride, *Journal of Applied Physics*, Vol.47, No.4, pp.1203–1208 (1976).

[5] Tan, S.X.-D., Tahoori, M., Kim, T., Wang, S., Sun, Z. and Kiamehr, S.: VLSI Systems Long-Term Reliability – Modeling, Simulation and Optimization, Springer Publishing (2019).

[6] Huang, X., Yu, T., Sukharev, V. and Tan, S.X.-D.: Physics-based electromigration assessment for power grid networks, *Proc. Design Automation Conf.* (*DAC*), pp.1–6, IEEE (2014).

[7] Sukharev, V., Huang, X., Chen, H.-B. and Tan, S.X.-D.: IR-drop based electromigration assessment: parametric failure chip-scale analysis, *Proc. Int. Conf. Computer Aided Design* (*ICCAD*), pp.428–433, IEEE (2014).

[8] Chen, H., Tan, S.X.-D., Huang, X., Kim, T. and Sukharev, V.: Analytical modeling and characterization of electromigration effects for multibranch interconnect trees, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.35, No.11, pp.1811–1824 (2016).

© 2020 Information Processing Society of Japan

[9] Huang, X., Kteyan, A., Tan, S.X.-D. and Sukharev, V.: Physics-based electromigration models and full-chip assessment for power grid networks, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.35, No.11, pp.1848–1861, DOI: 10.1109/TCAD.2016.2524540 (2016).

[10] Mishra, V. and Sapatnekar, S.S.: Predicting Electromigration Mortality Under Temperature and Product Lifetime Specifications, *Proc. Design Automation Conf.* (*DAC*), pp.1–6 (2016).

[11] Sun, Z., Demircan, E., Shroff, M.D., Kim, T., Huang, X. and Tan, S.X.-D.: Voltage-Based Electromigration Immortality Check for General Multi-Branch Interconnects, *Proc. Int. Conf. Computer Aided Design* (*ICCAD*), pp.1–7 (2016).

[12] Huang, X., Sukharev, V., Kim, T. and Tan, S.X.-D.: Electromigration recovery modeling and analysis under time-depdendent current and temperature stressing, *Proc. Asia South Pacific Design Automation Conf.* (*ASPDAC*), pp.244–249, IEEE (2016).

[13] Huang, X., Sukharev, V. and Tan, S.X.-D.: Dynamic electromigration modeling for transient stress evolution and recovery under time-dependent current and temperature stressing, *Integration, VLSI Journal*, Vol.55, pp.307–315 (2016).

[14] Chatterjee, S., Sukharev, V. and Najm, F.N.: Power Grid Electromigration Checking using Physics-Based Models, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.37, No.7, pp.1317–1330 (2018).

[15] Cook, C., Sun, Z., Demircan, E., Shroff, M.D. and Tan, S.X.-D.: Fast electromigration stress evolution analysis for interconnect trees using krylov subspace method, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, Vol.26, No.5, pp.969–980 (2018).

[16] Sun, Z., Demircan, E., Shroff, M.D., Cook, C. and Tan, S.X.-D.: Fast Electromigration Immortality Analysis for Multisegment Copper Interconnect Wires, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.37, No.12, pp.3137–3150 (2018).

[17] Zhao, H. and Tan, S.X.-D.: Postvoiding fem analysis for electromigration failure characterization, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, Vol.26, No.11, pp.2483–2493 (2018).

[18] Abbasinasab, A. and Marek-Sadowska, M.: RAIN: A tool for reliability assessment of interconnect networks—Physics to software, *Proc. Design Automation Conf.* (*DAC*), pp.133:1–133:6, ACM (2018).

[19] Sun, Z., Sadiqbatcha, S., Zhao, H. and Tan, S.X.-D.: Saturation-Volume Estimation for Multisegment Copper Interconnect Wires, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, Vol.27, No.7, pp.1666–1674 (2019).

[20] Chen, L., Tan, S.X.-D., Sun, Z., Peng, S., Tang, M. and Mao, J.: Fast analytic electromigration analysis for general multisegment interconnect wires, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, pp.1–12, DOI: 10.1109/TVLSI.2019.2940197 (2019).

[21] Sadiqbatcha, S., Sun, Z. and Tan, S.X.: Accelerating electromigration aging: Fast failure detection for nanometer ICs, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.39, No.4, pp.885–894 (2020).

[22] Sun, Z., Yu, S., Zhou, H., Liu, Y. and Tan, S.X.: Emspice: Physics-based electromigration check using coupled electronic and stress simulation, *IEEE Trans. Device and Materials Reliability*, p.1 (2020).

[23] Zhou, H., Sun, Z., Sadiqbatcha, S., Chang, N. and Tan, S.X.-D.: EM-Aware and Lifetime-Constrained Optimization for Multisegment Power Grid Networks, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, Vol.27, No.4, pp.940–953 (2019).

[24] He, K., Huang, X., Tan, S.X.-D.: Em-based on-chip aging sensor for detection and prevention of counterfeit and recycled ics, *Proc. Int. Conf. Computer Aided Design* (*ICCAD*), pp.146–151 IEEE (2015).

[25] He, K., Huang, X. and Tan, S.X.-D.: Em-based on-chip aging sensor for detection of recycled ICs, *IEEE Design & Test*, Vol.33, No.5, pp.56–64 (2016).

[26] Cook, C., Sadiqbatcha, S., Sun, Z. and Tan, S.X.-D.: Reliability-based hardware trojan design using physics-based electromigration models, *Integration, VLSI Journal*, Vol.66, pp.9–15 (2019).

[27] EMspice – Coupled EM-IR Analysis Tool for Full-Chip Power Grid EM Check and Sign-off, available from ⟨https://github.com/sheldonucr/EMspice_python⟩.

[28] Lasance, C.J.M.: Thermally driven reliability issues in microelectronic systems: Status-quo and challenges, *Microelectronics Reliability*, Vol.43, No.12, pp.1969–1974 (2003).

[29] Sukharev, V.: Physically Based Simulation of Electromigration-Induced Degradation Mechanisms in Dual-Inlaid Copper Interconnects, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.24, No.9, pp.1326–1335 (2005).

[30] Sukharev, V., Zschech, E. and Nix, W.D.: A model for electromigration-induced degradation mechanisms in dual-inlaid copper interconnects: Effect of microstructure, *Journal of Applied Physics*, Vol.102, No.5, 053505 (2007).

[31] Korhonen, M.A., Børgesen, P., Tu, K.N. and Li, C.-Y.: Stress evolution due to electromigration in confined metal lines, *Journal of Applied Physics*, Vol.73, No.8, pp.3790–3799 (1993).

[32] Lloyd, J.R.: New models for interconnect failure in advanced IC technology, *15th International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA 2008*, pp.1–7 (2008).

[33] Hu, C.-K., Canaperi, D., Chen, S.T., Gignac, L.M., Herbst, B., Kaldor, S., Krishnan, M., Liniger, E., Rath, D.L., Restaino, D., Rosenberg, R., Rubino, J., Seo, S.-C., Simon, A., Smith, S. and Tseng, W.-T.: Effects of overlayers on electromigration reliability improvement for cu/low k interconnects, *2004 IEEE International Reliability Physics Symposium Proc. 42nd Annual*, pp.222–228, IEEE (2004).

[34] Zhang, L.: *Effects of scaling and grain structure on electromigration reliability of cu interconnects*, Ph.D. thesis, University of Texas at Austin (2010).

[35] Cook, C., Sun, Z., Kim, T. and Tan, S.X.-D.: Finite difference method for electromigration analysis of multi-branch interconnects, *Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), pp.1–4, IEEE (2016).

[36] Suo, Z.: *Reliability of Interconnect Structures, Vol.8 of Comprehensive Structural Integrity*, Elsevier, Amsterdam (2003).

[37] Roy, A. and Tan, C.M.: Very high current density package level electromigration test for copper interconnects, *Journal of Applied Physics*, Vol.103, No.9 (2008).

[38] Zhao, H. and Tan, S.X.-D.: Multi-physics-based FEM analysis for post-voiding analysis of electromigration failure effects, *Proc. Int. Conf. Computer Aided Design* (*ICCAD*), pp.1–8, IEEE (2018).

[39] Sun, Z., Sadiqbatcha, S., Zhao, H. and Tan, S.X.-D.: Accelerating Electromigration Aging for Fast Failure Detection for Nanometer ICs, *Proc. Asia South Pacific Design Automation Conf.* (*ASPDAC*), pp.623–630 (2018).

[40] Synopsys, Synopsys University Program and Resources, available from ⟨https://www.synopsys.com/community/university-program/teaching-resources.html⟩.

[41] Sadiqbatcha, S., Cook, C., Sun, Z. and Tan, S.X.-D.: Accelerating electromigration wear-out effects based on configurable sink-structured wires, *Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), pp.21–24, IEEE (2018).

[42] Limited, A.: Arm cortex-m0 designstart (2010), available from ⟨https://developer.arm.com/products/designstart/processor-ip⟩.

[43] Synopsys 32/28nm generic library for teaching ic design, available from ⟨http://www.synopsys.com⟩.

[44] Chen, H., Tan, S.X.-D., Sukharev, V., Huang, X. and Kim, T.: Interconnect reliability modeling and analysis for multi-branch interconnect trees, *Proc. Design Automation Conf.* (*DAC*), pp.1–6, IEEE (2015).

[45] Chen, H.-B., Tan, S.X.-D., Huang, X. and Sukharev, V.: New electromigration modeling and analysis considering time-varying temperature and current densities, *Proc. Asia South Pacific Design Automation Conf.* (*ASPDAC*), pp.352–357, IEEE (2015).

[46] Wang, X., Wang, H., He, J., Tan, S.X.-D., Cai, Y. and Yang, S.: Physics-based Electromigration Modeling and Assessment for Multi-Segment Interconnects in Power Grid Networks, *Proc. Design, Automation and Test In Europe Conf.* (*DATE*), pp.1727–1732 (2017).

[47] Kim, T., Sun, Z., Cook, C., Zhao, H., Li, R., Wong, D., Tan, S.X.-D.: Cross-layer modeling and optimization for electromigration induced reliability, *Proc. Design Automation Conf.* (*DAC*), pp.1–6, IEEE (2016).

[48] Wang, X., Yan, Y., He, J., Tan, S.X.-D., Cook, C. and Yang, S.: Fast physics-based electromigration analysis for multi-branch interconnect trees, *Proc. Int. Conf. Computer Aided Design* (*ICCAD*), pp.169–176, IEEE (2017).

[49] Tan, C.M.: *Electomigration in ULSI Interconnects, International Series on Advances in Solid State Electronics and Technology*, Word Scientific (2010).

[50] Lienig, J. and Thiele, M.: *Fundamentals of Electromigration-Aware Integrated Circuit Design*, Springer (2018).

[51] Posser, G., Mishra, V., Jain, P., Reis, R. and Sapatnekar, S.S.: A Systematic Approach for Analyzing and Optimizing Cell-Internal Signa Electromigration, *Proc. IEEE/ACM Int. Conf. Computer Aided Design* (*ICCAD*), pp.1–6, IEEE (2014).

[52] Posser, G., Mishra, V., Jain, P., Reis, R. and Sapatnekar, S.S.: Cell-internal electromigration: Analysis and pin placement based optimization, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.35, No.2, pp.220–231 DOI: 10.1109/TCAD.2015.2456427 (2016).

[53] Mishra, V. and Sapatnekar, S.S.: Circuit delay variability due to wire resistance evolution under ac electromigration, *2015 IEEE International Reliability Physics Symposium*, pp.3D.3.1–3D.3.7, DOI: 10.1109/IRPS.2015.7112713 (2015).

[54] Jain, P., Sapatnekar, S.S. and Cortadella, J.: Stochastic and topologically aware electromigration analysis for clock skew, *2015 IEEE International Reliability Physics Symposium*, pp.3D.4.1–3D.4.6, DOI: 10.1109/IRPS.2015.7112714 (2015).

© 2020 Information Processing Society of Japan

[55] Jain, P., Sapatnekar, S.S. and Cortadella, J.: A retargetable and accurate methodology for logic-ip-internal electromigration assessment, *The 20th Asia and South Pacific Design Automation Conference*, pp.346–351, DOI: 10.1109/ASPDAC.2015.7059029 (2015).

[56] Jain, P., Cortadella, J. and Sapatnekar, S.S.: A fast and retargetable framework for logic-ip-internal electromigration assessment comprehending advanced waveform effects, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, Vol.24, No.6, pp.2345–2358, DOI: 10.1109/TVLSI.2015.2505504 (2016).

[57] Chatterjee, S., Sukharev, V. and Najm, F.N.: Fast physics-based electromigration checking for on-die power grids, *2016 IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), pp.1–8, DOI: 10.1145/2966986.2967041 (2016).

[58] Chatterjee, S., Sukharev, V. and Najm, F.N.: Fast physics-based electromigration assessment by efficient solution of linear time-invariant (lti) systems, *2017 IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), pp.659–666, DOI: 10.1109/ICCAD.2017.8203840 (2017).

[59] Chatterjee, S., Sukharev, V. and Najm, F.N.: Power grid electromigration checking using physics-based models, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.37, No.7, pp.1317–1330 (2018).

[60] Mishra, V. and Sapatnekar, S.S.: The impact of electromigration in copper interconnects on power grid integrity, *2013 50th ACM/EDAC/IEEE Design Automation Conference* (*DAC*), pp.1–6, DOI: 10.1145/2463209.2488842 (2013).

[61] Mishra, V. and Sapatnekar, S.S.: Probabilistic wire resistance degradation due to electromigration in power grids, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, Vol.36, No.4, pp.628–640, DOI: 10.1109/TCAD.2016.2584054 (2017).

[62] Jain, P., Mishra, V. and Sapatnekar, S.S.: Fast stochastic analysis of electromigration in power distribution networks, *IEEE Trans. Very Large Scale Integration* (*VLSI*) *Systems*, Vol.25, No.9, pp.2512–2524, DOI: 10.1109/TVLSI.2017.2706520 (2017).

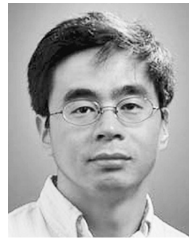
[63] Mishra, V., Jain, P., Marella, S.K., and Sapatnekar, S.S.: Incorporating the role of stress on electromigration in power grids with via arrays, *2017 54th ACM/EDAC/IEEE Design Automation Conference* (*DAC*), pp.1–6, DOI: 10.1145/3061639.3062266 (2017).

[64] Abbasinasab, A. and Marek-Sadowska, M.: Blech effect in interconnects: Applications and design guidelines, *Proc. 2015 Symposium on International Symposium on Physical Design, ISPD '15*, pp.111–118, ACM, DOI: 10.1145/2717764.2717772 (2015).

[65] Abbasinasab, A.: *Interconnect aging–Physics to software*, Ph.D. thesis, University of California Santa Barbara (June 2018).

[66] Abbasinasab, A. and Marek-Sadowska, M.: Non-uniform temperature distribution in interconnects and its impact on electromigration, *Proc. 2019 on Great Lakes Symposium on VLSI, GLSVLSI '19*, pp.117–122, ACM (2019).

[67] Demircan, E. and Shroff, M.D.: Model based method for electromigration stress determination in interconnects, *2014 IEEE International Reliability Physics Symposium*, pp.IT.5.1–IT.5.6, DOI: 10.1109/IRPS.2014.6861154 (2014).



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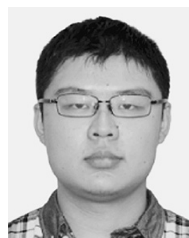

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