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Exploring BTI aging effects on spatial power density and temperature profiles of VLSI chips

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ABSTRACT

The Long-term reliability of a chip, encompassing factors like bias temperature instability (BTI), plays a substantial role in the chip's operational efficiency and overall lifespan. Most studies primarily center around performance-related aspects like delay and timing impacts, and fewer studies are performed on reliability impacts on the spatial power density and thermal profiles of the chips. In this study, we propose to investigate the BTI impacts on the spatial power density and temperature profiles of VLSI chips for the first time. We assessed the BTI aging impact on the on-chip spatial power density and temperature for two widely used circuit functional blocks (dual port RAM, Discrete Cosine Transform (DCT) block) at T = 130°C and T = 25°C to account for the worst-case BTI degradation, using degradation-aware cell libraries for a 10-year aging scenario. Furthermore, we showcased the essential role of BTI aging-aware timing analysis in evaluating the impact of BTI aging on total power, on-chip spatial power density, and thermal maps. Neglecting this aspect can result in a substantial underestimation of the results related to the parameters mentioned above. We developed a power map generation method from the circuit layout and power analysis from EDA tools. We demonstrate that both circuits' maximum power density reduction is approximately 12 % and 20 %, respectively. Furthermore, to analyze the BTI impact on spatial temperature, we built the heat transfer model using a multiphysics tool to imitate a real chip (Intel i7-8650U) and performed thermal simulations to evaluate the spatial thermal map. The resulting maximum temperature reduction for both these circuits is approximately 10 % and 12 %, respectively, which is quite significant.

Our analysis has further unveiled that, in the context of a specific circuit, the position of maximum power density and the occurrence of a hot spot remains consistent over time, unaffected by aging. However, it's important to note that these positions can vary between different circuits, primarily influenced by the workload the circuit is currently handling. Furthermore, our findings demonstrate that the effects of Bias Temperature Instability (BTI) aging are significantly more pronounced when the circuit operates at higher temperatures (T = 130°C) compared to lower operating temperatures (T = 25°C).

1. Introduction

In today's era of deep technology, the process of technology scaling has heightened the vulnerability of transistor electrical characteristics to various long-term aging phenomena. These encompass Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI), which affect devices, and Electromigration, which impacts interconnects. Among these mechanisms, BTI emerges as the predominant aging influence on CMOS devices within the sub-45nm technology nodes and beyond [1,2]. BTI arises due to the electrical field stress experienced by transistors, resulting in the generation of interface traps (caused by the rupture of Si-H bonds at the Si-SiO_2 interface) and oxide traps (formed as charges become trapped within voids in the dielectric layer). Over time, these imperfections (interface and oxide traps) accumulate within the transistor, manifesting their impact through deteriorations in its electrical characteristics, including threshold voltage ($V_{T\,H}$) and mobil-ity (μ), etc. These deteriorations, in turn, give rise to timing errors and violations.

The impact of BTI on timing and delay has been extensively explored in previous research [3–5]. These studies have pro-vided evidence indicating that timing errors induced by aging can occur not only over

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extended periods, as traditionally understood (as demonstrated in Ref. [6]), but also within signif-icantly shorter time intervals, on the order of milliseconds or even microseconds [7,8]. The notion of precise timing guard-band estimation through aging-aware timing analysis was introduced in a prior study [3].

However, there has been limited research into the influence of BTI on power consumption and chip temperature. Previous studies [9,10] have suggested that BTI can reduce power consumption and provide aging-related benefits to circuits by elevating the transistor threshold voltage ($V_{T\ H}$). For instance, in Ref. [9], simulations illustrated that the static power in a ring os-cillator composed of 10 FO4 cascaded inverters could decrease by 50 % within a month of operation and reach a sub-stantial 78 % reduction over a span of 10 years. Furthermore, a study by Sheng et al. [10] observed a significant reduction of approximately 30 % in leakage energy for FPGA-based circuits, specifically in the context of SRAM.

Nevertheless, recent findings [11] emphasize that BTI's impact extends beyond just the threshold voltage ($V_{T\ H}$), affecting various CMOS device parameters such as carrier mobility (μ), sub-threshold slope (SS), and gate-drain capac-itance (C_{gd}). Like previous state-of-the-art research [9], we should not disregard this broader impact to prevent inaccurate estimations of BTI's effects on power. Additionally, both [3,11] demonstrate that the influence of BTI aging on standard cell performance is non-uniform and dependent on operational conditions, such as input signal slew and output capacitance, rather than solely on the transistor duty cycle.

However, most existing approaches have primarily focused on assessing the effects of BTI solely on the overall power consumption of chips. Remarkably, there needs to be more research investigating the implications of BTI degradation on the spatial power density and the resulting temperature distribution across the chip. This dimension is relevant for developing future strategies for runtime, aging-aware thermal, and power management/optimization.

In this study, we have undertaken a comprehensive in-vestigation into the impact of BTI aging on various facets, including total power consumption, spatial power density, and thermal profiles, within the context of the most com-monly utilized circuit functional blocks, namely, the Dual Port Synchronous RAM and the Discrete Cosine Transform (DCT). We consider critical factors in our analysis, such as the influence of BTI aging on timing-related effects and operational temperature. We outline the primary contributions of our research as follows.

1. For the first time, we investigate the influence of BTI on the on-chip spatial power density and thermal char-acteristics of VLSI chips, incorporating these essential factors into our analysis. To evaluate the impact of BTI on total power, we conduct aging-aware power analysis using commercial EDA tools for widely employed circuits such as the Discrete Cosine Transform (DCT) and synchronous RAM circuits, based on the Nangate 45 nm degradation-aware standard cell library [11].
2. Using circuit layout data and power analysis from EDA tools, we create a power map generator to estimate spatial power density. This data is then input into a thermal model based on the finite element method (FEM) to predict the temperature distribution on the chip.
3. Our experimental results demonstrate that in the case of the sequential RAM circuit, BTI aging leads to an approximately 13 % reduction in total power, a 12 % decrease in maximum power density, and a 10 % decline in maximum temperature at an operating temperature of 130°C, as well as a reduction of about 10 % in total power, 11 % in maximum power density, and 7 % in maximum temperature at an operating temperature of 25°C. For the DCT circuit, we observed a reduction of 14 % in total power, a 20 % decrease in maximum power density, and a 12 % decline in maximum temperature at an operating temperature of 130°C, and a reduction of 9 % in total power, 9.5 % in maximum power density, and 3.6 % in maximum temperature at an operating temperature of 25°C.
4. Our study illustrates that aging can, over time, reduce both the power density and hot spots within the circuits. Interestingly, we found that although the locations of hot spots differ between these circuits, the location remains consistent for a particular circuit due to BTI aging.
5. Our investigation also demonstrates that the impact of BTI aging on total power, spatial power density, and temperature becomes more pronounced at high operating temperatures (i.e., T = 130°C) compared to lower operat-ing temperatures (i.e., T = 25°C).

This paper is structured as follows: In Section II, we introduce the methodology for estimating aging power density maps, encompassing the utilization of a degradation-aware li-brary, an aging-aware design flow, and the estimation of power density maps. Section III outlines the aging-aware thermal map estimation approach, relying on a realistic commercial chip's thermal model. Section IV delves into the timing analysis that considers aging effects. In Section V, we present the experimental results illustrating the impacts of aging on both DCT and RAM circuit designs. Finally, Section VI provides the paper's concluding remarks.

2. Aging aware power map estimation method

In this section, we will present the methodology to inves-tigate the aging effect of BTI on the on-chip spatial power density and temperature. First, we will show the aging-aware power analysis and spatial power density map estimation method. Afterwards, we will present the aging-aware thermal map estimation using a finite element method (FEM) based multi-physics tool.

A. Degradation aware cell libraries

In this study, we harnessed 45 nm degradation-aware Cell Libraries sourced from the NanGate Open cell library [12]. These specialized libraries encapsulate the response of each cell to a spectrum of conditions, considering 7 × 7 combi-nations of input signal slew and output capacitance. This comprehensive coverage empowers us to accurately capture the impact of BTI degradation in diverse operational scenarios. To investigate the effects of operating conditions on 10-year BTI-induced degradation, especially regarding spatial power density and temperature, we examined two extreme temper-ature points: high (T = 130°C) and low (T = 25°C) operating temperatures, both at a supply voltage (V_{dd}) of 1.2 V.

The selection of the extreme temperature points, T = 130°C and T = 25°C was primarily driven by the need to evaluate the BTI effects under varying thermal conditions. These tem-peratures represent the high and low extremes of operating conditions for VLSI chips, thus providing a comprehensive understanding of the BTI aging effects across the spectrum of possible operating environments. At the elevated temperature of T = 130°C, the BTI aging effects are more pronounced, showcasing the worst-case scenario for reliability and perfor-mance degradation. This high-temperature analysis is crucial for understanding the upper limits of thermal resilience and the associated risks of accelerated aging in VLSI chips. Con-versely, the lower temperature point of T = 25°C offers insights into the BTI aging effects under more typical or benign operating conditions. This temperature is representative of a standard operational environment, thus providing a baseline against which the heightened effects at T = 130°C can be compared. By examining the BTI aging impacts at these two temperature extremes, our study aims to provide a thorough understanding of how varying operating temperatures influence the aging process in VLSI chips. This approach enables a more robust and comprehensive analysis, facilitating the development of more effective aging-aware design strategies for future chip technologies.

These libraries have taken into account the BTI effect on various crucial parameters of transistors: carrier mobility(μ), sub-threshold slope(SS), gate-drain capacitance(C_{gd}) instead of only accounting for the effect on threshold voltage ($V_{T\ H}$). This holistic perspective accurately estimates BTI's influence on static and dynamic power [11]. These specialized cell libraries, comprehensive in their incorporation of BTI effects on a range of critical parameters, are available through the Karlsruhe Institute of Technology (KIT) [13].

B. Aging aware power analysis

The correlation between temperature distribution and power density map (on-chip power density distribution) is strik-ing. Our exploration began with aging-aware power analysis, mirroring the approach detailed in Ref. [11], utilizing standard commercial EDA tools. We elucidate the essence of our aging-aware power analysis method in Fig. 1. The synthesis phase involved obtaining the netlist by inputting the register transfer level (RTL) description and constraints and the original aging-free library into a synthesis tool (e.g., Synopsys Design Compiler). This synthesized netlist, along with the physical library reference and constraints, was then processed through the layout tool (Cadence Innovus) for automatic placement and routing (APR), yielding a post-layout netlist along with RC parasitic information. Multiple simulations were conducted at different stages of the flow to ensure functionality, including RTL simulation and gate-level simulation (GLS) on both gate-level and post-layout netlists. We performed an accurate power analysis using Synopsys PrimePower in the conclusive phase. We provided the post-layout netlist, RC parasitic information, and degradation-aware library reference to compute power out-put under BTI degradation. Gate-level simulation on the post-layout netlist aided in annotating it with switching activity, ensuring precision in power analysis. The final step involved comparing total power under aging and no-aging scenarios to establish the power difference.

C. Power density map estimation

We developed a Python script-based power density map generator to obtain spatial power density. The generator re-ceives three inputs: the chip's coordinates, cell placement information from the layout tool, and

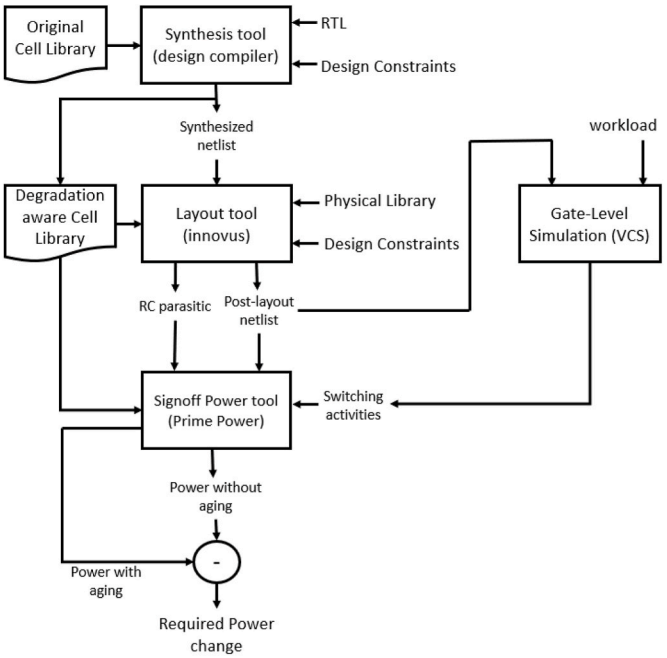


Fig. 1. The proposed aging-aware power analysis flow.

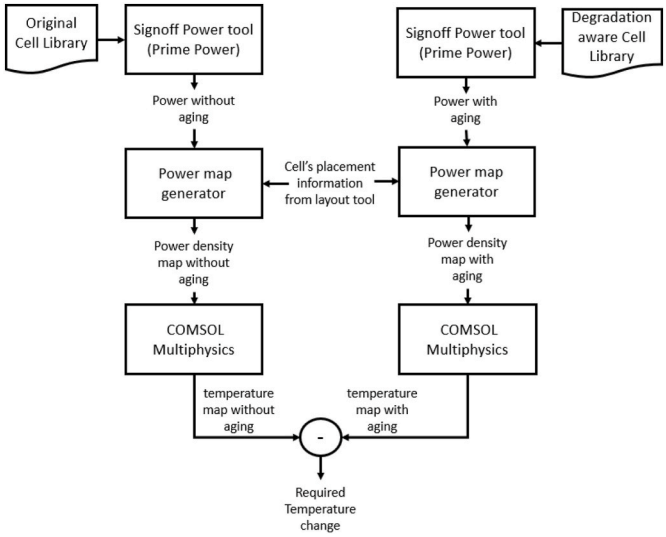


Fig. 2. The proposed aging-aware power density and temperature map estimation flow.

power data from the sign-off power tool. The generator now divides the chip geometry into 100 × 100 grids and provides the power density distribution for each grid using the power statistics of the cells and their locations. Although we have used a grid size of 100 × 100 for more granularity, the generator is extendable to different grid sizes of $N \times N$. If the finer granularity is required, N can be increased. This approach is highlighted in Fig. 2.

3. Aging aware spatial thermal map estimation

This subsection outlines the process of spatial thermal estimation based on the finite element method, utilizing the power map estimation as a foundational input. Since thermal simulation necessitates packaging information, we constructed a heat transfer model within COMSOL Multiphysics to mirror the actual CPU packaging geometry. The choice of a finite element approach for thermal simulations is grounded in its demonstrated accuracy, as indicated by the work of the author in Ref. [14], showcasing a root mean square error (RMSE) of 1.8°C. The constructed heat transfer model comprises four core components: the heat sink, processor baseboard, motherboard, and CPU processor die. We sourced measure-ments for these components to replicate the geometry of the Intel i7-8650U chip, accessible through the WikiChip group's open-sourced data [15]. The CPU package dimensions are 42 × 24 × 1.3 mm, with a baseboard thickness of 0.8 mm. Notably, the CPU die soldered onto the baseboard, the primary focus of our study, possesses dimensions of 14 × 9 × 0.5 mm, as illustrated in Fig. 3a). In our COMSOL model, the CPU die material is silicon, while FR4 represents the package baseboard. The package baseboard introduces convective heat flux, simulating the heat propagation from the CPU package to the heat sink, passing through the motherboard. COMSOL integrates information from our power map generator and specified boundary conditions to furnish spatial thermal maps, as elucidated in Fig. 2.

Given that the dimensions of the circuits employed in our assessment are smaller than those of the Intel i7-8650U chip, we utilized our power map generator to divide both chips' geometries into 100 × 100 grids. Subsequently, we mapped the power density of each grid for both chips.

Noteworthy boundary condition parameters for finite element-based thermal simulations encompass the ambient temperature and the heat sink's convective heat transfer rate (h_c) to the ambient environment. The procedure for computing these boundary conditions is detailed in Ref. [14], relying on sensor temperature data and CPU power information under both workloads and idle states, and this is just a one-time setup for this specific thermal model. It's important to highlight that

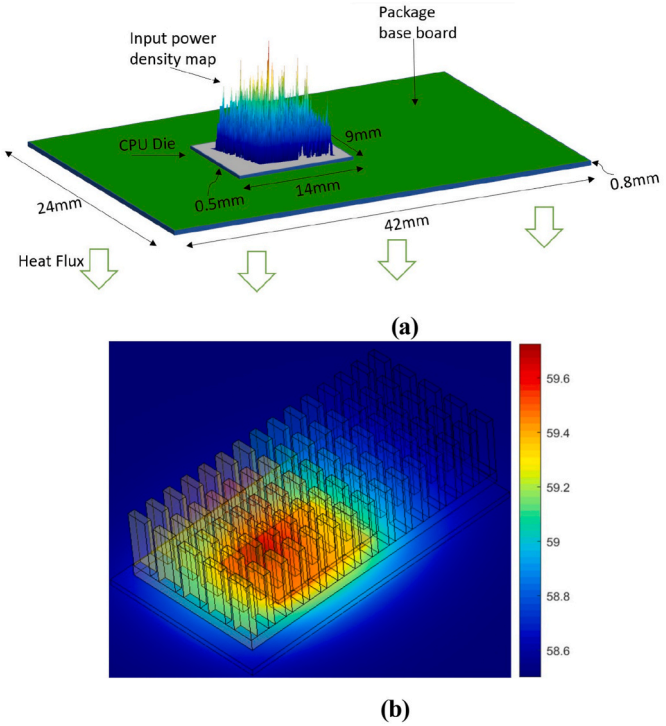


Fig. 3. (a) Thermal model based on the commercial Intel i7-8650U chip (b) 3D view for the heat sink used for thermal model.

the same boundary conditions were consistently applied for the no-aging and with-aging scenarios, thereby neutralizing any boundary-related influence when quantifying the temperature variance attributed to BTI aging.

We subsequently executed thermal simulations for both no-aging and aging scenarios to ascertain the temperature dif-ference caused by BTI aging. Utilizing an identical thermal model across both scenarios ensures a fair assessment of BTI aging's effect on temperature fluctuation. Notably, the convective heat transfer coefficient h_c is 29.5 $W{\cdot}m^{-2}\,{}^{\circ}C^{-1}$ and the ambient temperature is 33°C [14]. Fig. 3b offers a 3D visualization of the COMSOL-derived thermal map featuring a transparent heat sink.

4. Aging aware timing analysis

BTI-induced aging significantly retards transistor speed and increases the potential for timing violations. Therefore, it is crucial to consider this impact when evaluating the effects of BTI aging on total power, on-chip spatial power density, and temperature. To accurately reflect the impact of BTI aging on timing, we have embraced the concept of aging-aware timing analysis [3]. The core of this approach is illustrated in Fig. 4. Our investigation began by operating the Dual Port RAM and DCT circuits at a frequency of 500 MHz. Subsequently, our exploration focused on quantifying the frequency degradation attributed to BTI, aligning with the depiction in Fig. 4.

Our strategy follows a sequential progression. We initiated synthesis using commercial EDA tools, inputting the RTL description, design constraints, and an original cell library unaware of degradation. This synthesized netlist underwent automatic placement and routing (APR) in Cadence Innovus, resulting in a post-layout netlist enriched with RC parasitic data.

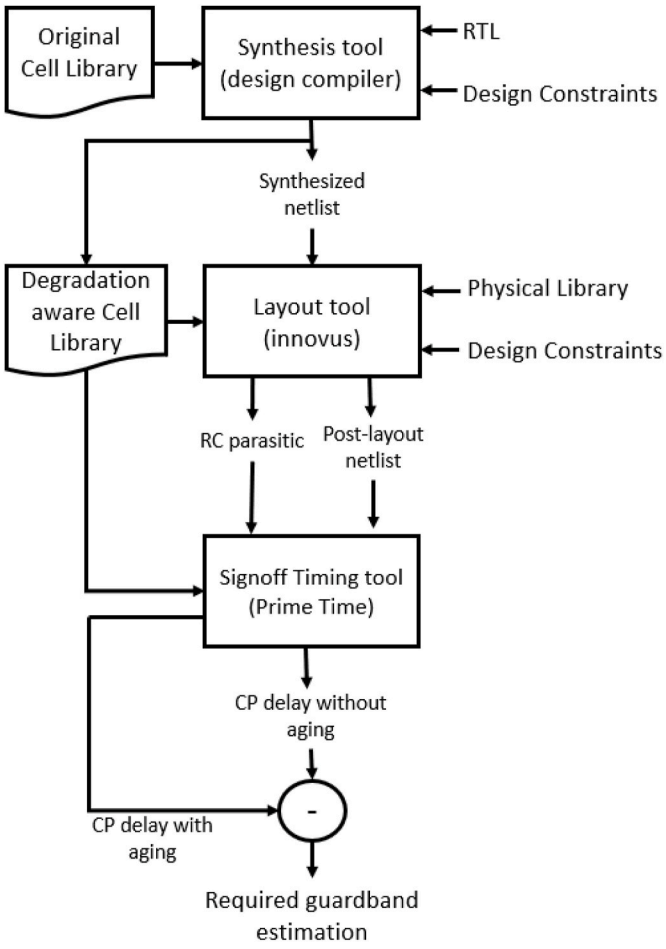


Fig. 4. The proposed aging-aware timing analysis flow.

Simulations at various stages validated the design's func-tionality, encompassing RTL and gate-level simulation (GLS) on both gate-level and post-layout netlists. The subsequent step of accurately estimating the timing guardband leveraged Synopsys PrimeTime. In this phase, the post-layout netlist, RC parasitic data, and a degradation-aware library reference provided the necessary inputs for critical path (CP) delay computation in BTI degradation. Comparative analysis of CP delays in aging and no-aging scenarios facilitated guardband determination. The calculated guardband for the RAM circuit were 140ps and 150ps at operating temperatures of 130°C and 25°C, respectively. Likewise, for the DCT circuit, the guardbands were 100ps and 90ps at operating temperatures of 130°C and 25°C, respectively.

We adjusted clock frequency using the derived guardband to accommodate aging-induced delays and ensure circuit re-liability. This recalibration laid the foundation for evaluating total power consumption, spatial power density distribution, and the impact on the temperature profile under the effects of BTI aging's timing impact. This comprehensive assessment employed methodologies outlined in Sections II-B, II-C, and III, collectively revealing the nuanced implications of BTI aging on the holistic performance of the circuit.

5. Experimental results and discussions

In this section, we present a detailed numerical analysis of the impact

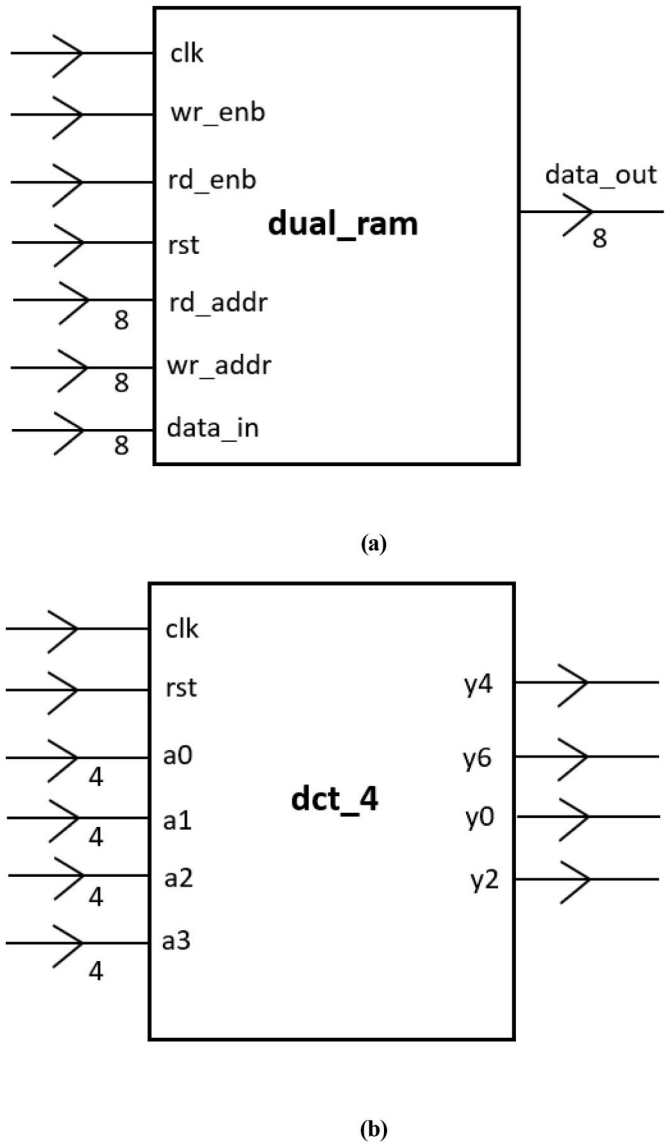


Fig. 5. Top-level module diagram for (a) Dual port RAM and (b) 4-bit DCT circuits.

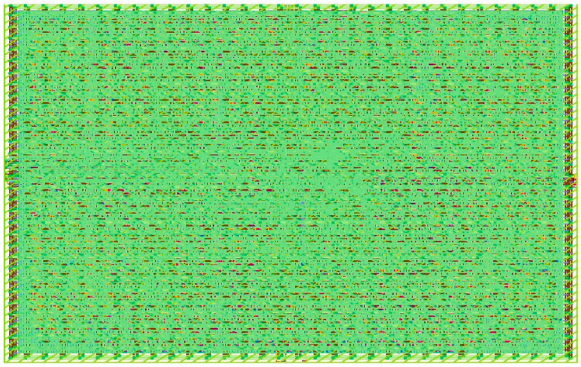
of BTI aging on spatial power density and thermal characteristics for two commonly used design blocks, Dual Port RAM (8-bit) and DCT circuit (4-bit) for which the top level module diagrams are shown in Fig. 5. Fig. 5a illustrates the key components and interactions of the dual-port RAM circuit. It features several input signals, including clk for clock synchronization, rst for reset functionality, wr_enb to enable write operations, rd_enb for read opera-tions, rd_addr and wr_addr to specify memory addresses, and data_in for input data to be written. On the output side, data_out represents the data read from the memory. This diagram provides an overview of the control and data flow within the dual-port RAM circuit, essential for its operation in various applications. In the same way, Fig. 5b depicts the top-level module diagram for the 4-bit dct circuit. It showcases the essential inputs (clk, rst, a0, a1, a2, a3) and outputs (y0, y2, y4, y6) of the circuit. clk is the clock signal, rst is the reset signal, and a0, a1, a2, a3 are the input values. On the output side, y0, y2, y4, y6 represent the DCT coefficients computed by the circuit.

The detailed layouts of the RAM and DCT circuits are depicted in Figs. 6 and 7, respectively. Figs. 6a and 7a present the comprehensive layout views of the RAM and DCT circuits, showcasing the arrangement of components and interconnections. Furthermore, Figs. 6b and 7b zoom in on specific areas, emphasizing the placement of standard cells at the four corners of the chip area. This detailed visualization is crucial for analyzing the power density distribution across the chip area, which is pivotal for evaluating circuit performance and reliability.

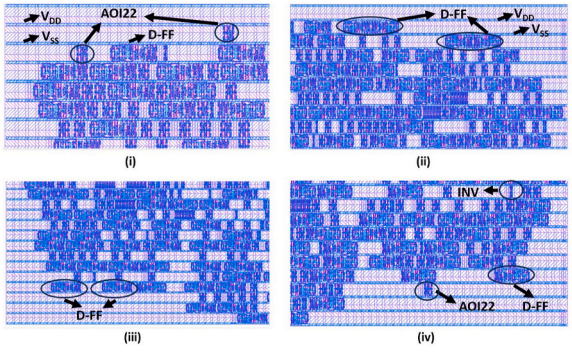
We highlight the significance of accounting for BTI aging-aware timing effects and emphasize the differences observed at both high operating temperature (T = 130°C) and low oper-ating temperature (T = 25°C). Our results underscore that the impacts of BTI aging on power and temperature are notably more pronounced at high operating temperatures (T = 130°C) compared to low operating temperatures (T = 25°C).

A. Impact of BTI on the on-chip power density

1) RAM Circuit Analysis at High Temperature: Figs. 8 and 9 illustrate the spatial power density distribution within the RAM circuit at an elevated temperature (T = 130°C). The initial maximum power density registers around 8100 MW/m^3 (Figs. 8a and 9a). After a decade of aging, without considering BTI timing impact (Fig. 8b), this diminishes to approximately 7873 MW/m^3. Incorporating BTI aging timing impact (Fig. 9b) further reduces it to 7154 MW/m^3. Power density difference maps (Figs. 8c and 9c) emphasize the effect. Excluding BTI timing impact, the maximum power density difference equals around 227 MW/m^3 (Fig. 8c). Conversely, when BTI aging-aware timing impact is factored in (Fig. 9c), the difference substantially increases to about 946 MW/m^3. This highlights the critical role of considering BTI aging timing and its potential to lead to significant

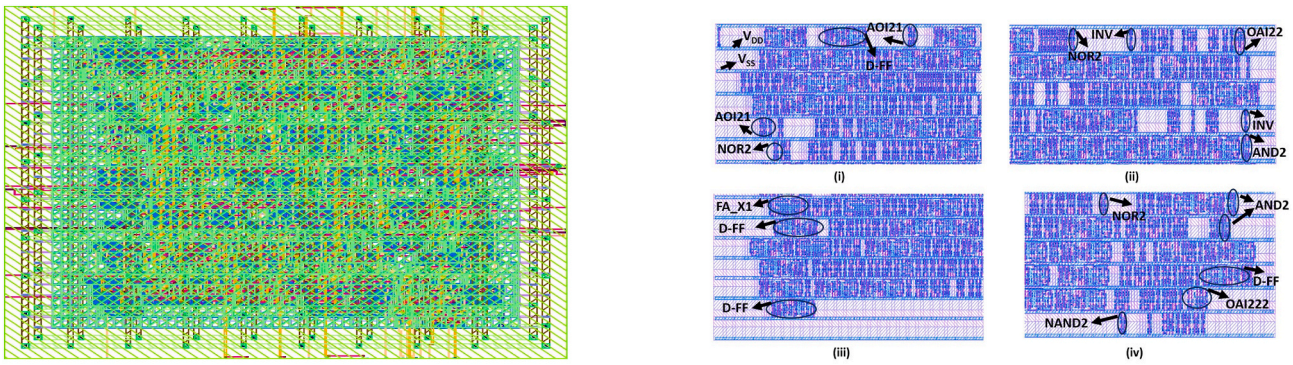


(a) RAM circuit layout overall view



(b) RAM circuit layout highlighting a view of selected standard cells

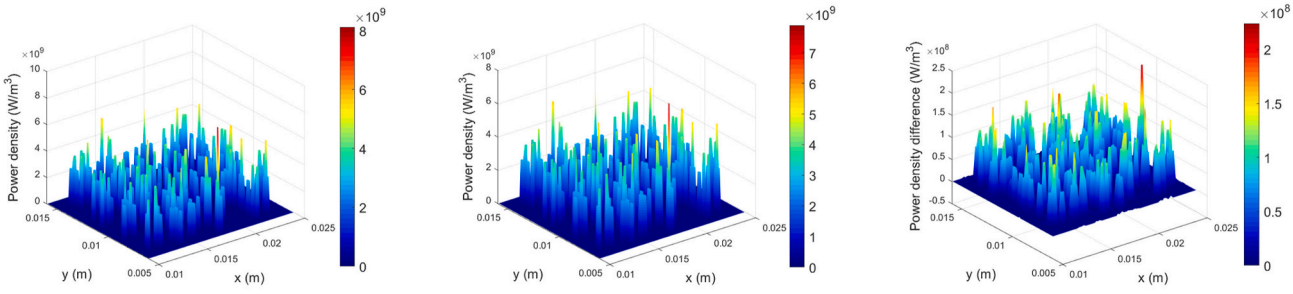
Fig. 6. RAM circuit layout diagram with two distinct perspectives: (a) presenting the comprehensive layout diagram and (b) providing a detailed layout view that highlights the arrangement of standard cells at all four corners.



(a) DCT circuit layout overall view

(b) DCT circuit layout highlighting a view of selected standard cells

Fig. 7. DCT circuit layout diagram with two distinct perspectives: (a) presenting the comprehensive layout diagram and (b) providing a detailed layout view that highlights the arrangement of standard cells at all four corners.

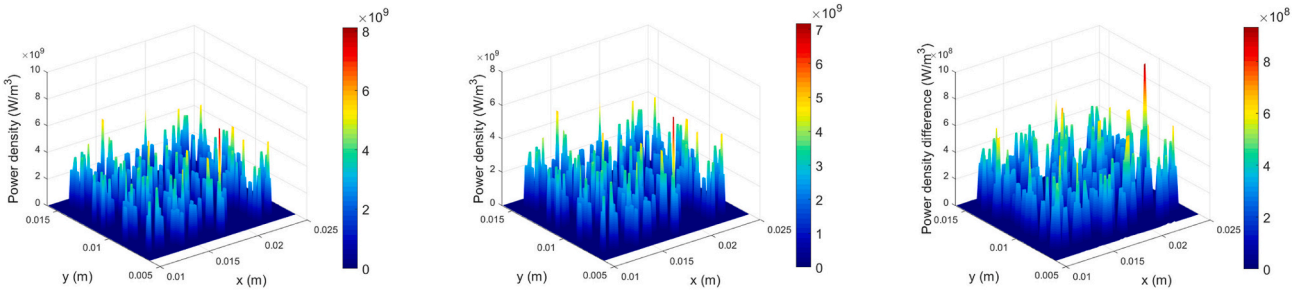


(a) RAM non-aging power density

(b) RAM with-aging power density without including BTI timing effect

(c) RAM power density difference

Fig. 8. On-chip spatial power density and power density difference maps for RAM circuit at 130°C operating temperature library.

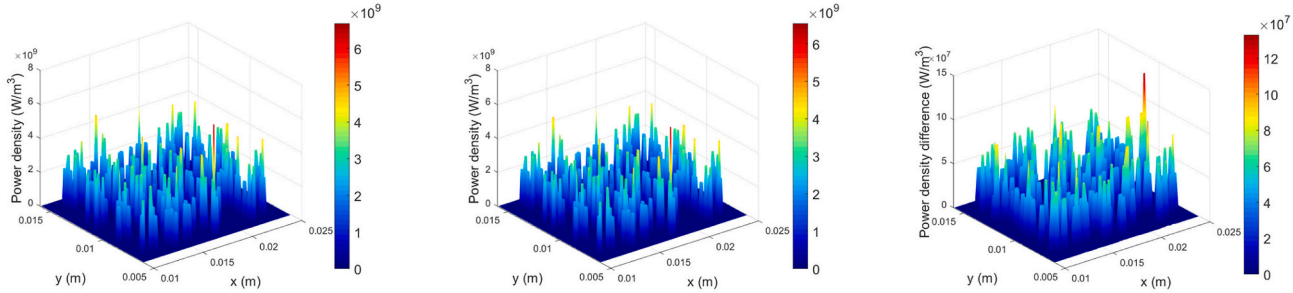


(a) RAM non-aging power density

(b) RAM with-aging power density including BTI timing effect

(c) RAM power density difference

Fig. 9. On-chip spatial power density and power density difference maps for RAM circuit at 130°C operating temperature library.

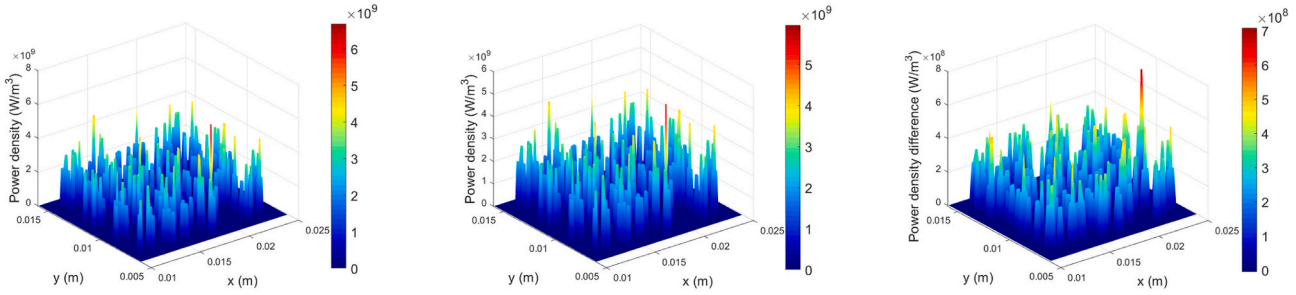


(a) RAM non-aging power density

(b) RAM with-aging power density without including BTI timing effect

(c) RAM power density difference

Fig. 10. On-chip spatial power density and power density difference maps for RAM circuit at 25°C operating temperature library.

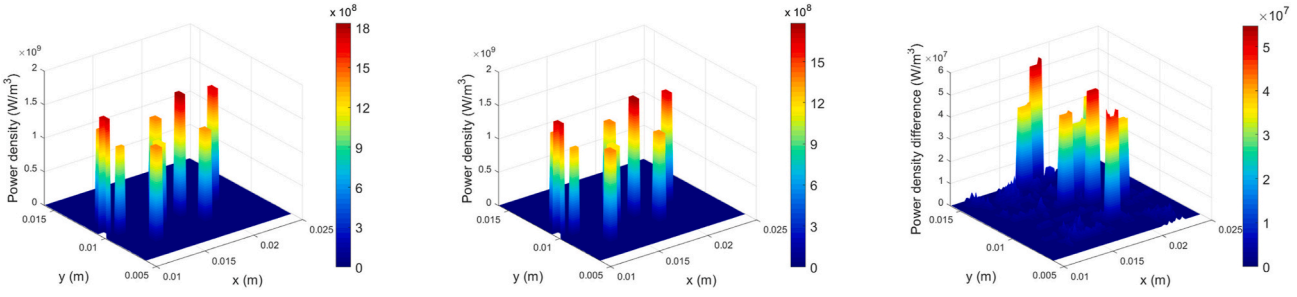


(a) RAM non-aging power density

(b) RAM with-aging power density including BTI timing effect

(c) RAM power density difference

Fig. 11. On-chip spatial power density and power density difference maps for RAM circuit at 25°C operating temperature library.



(a) DCT non-aging power density

(b) DCT with-aging power density without including BTI timing effect

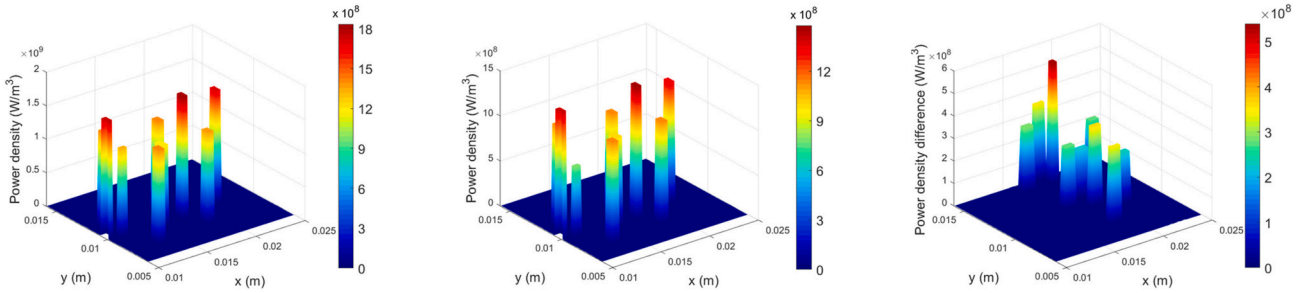
(c) DCT power density difference

Fig. 12. On-chip spatial power density and power density difference maps for DCT circuit at 130°C operating temperature library.

underestimations, as underscored in Fig. 24b. Furthermore, Fig. 24a vividly illustrates the underestimation in total power associated with this phenomenon.

2) RAM Circuit Analysis at low Temperature: Similarly, Figs. 10 and 11 depict the power density distribution within the RAM circuit at a lower operating temperature (T = 25°C). Initial observations reveal a peak power density nearing 6630 MW/m^3 (Figs. 10a and 11a). Over a decade of aging, without considering BTI aging impact, the maximum power density is approximately 6500 MW/m^3 (Fig. 10b), while including BTI aging timing impact lowers it further to around 5913 MW/m^3 (Fig. 11b).Power density difference maps (Figs. 10c and 11c) illustrate considerable variations. With-out BTI timing impact, the maximum power density difference after a decade of aging is approximately 130 MW/m^3 (Fig. 10c). With BTI aging timing impact considered, this difference increases significantly to around 717 MW/m^3 (Fig. 11c). This underscores the paramount importance of accounting for BTI aging timing and its capacity to result in substantial underestimations, as emphasized in Fig. 25b. Additionally, Fig. 25a underscores the total power underestimation that aligns with this finding.
3) *DCT Circuit Analysis at High Temperature:* In a parallel vein, Figs. 12 and 13 exhibit the spatial power density distribution within the DCT circuit at high operating tempera-ture (T = 130°C). The initial maximum power density measures around 1800 MW/m^3 (Figs. 12a and 13a). After a decade of aging, without considering BTI timing impact (Fig. 12b), this reduces to approximately 1751 MW/m^3, and with BTI aging timing impact considered, it further decreases to around 1450 MW/m^3 (Fig. 13b). Power density difference maps (Figs. 12c and 13c) spotlight the difference. Not accounting for BTI timing impact, the maximum power density difference approximates 49 MW/m^3 (Fig. 12c). Contrastingly, with BTI aging-aware timing impact considered (Fig. 13c), the difference magnifies significantly to about 350 MW/m^3. This reiterates the importance of factoring in BTI aging timing and its potential to lead to substantial underestimations, as illuminated in Fig. 26b. Similarly, Fig. 26a spotlights the underestimation in total power related to this aspect.
4) DCT Circuit Analysis at low Temperature: Likewise, Figs. 14 and 15 present the power density distribution within the DCT circuit at a lower operating temperature (T = 25°C). Initial assessments unveil a peak power density of 630 MW/m^3 (Figs. 14a and 15a). After a decade of aging, without considering BTI aging impact, the maximum power density is approximately 625 MW/m^3 (Fig. 14b). With BTI aging timing impact incorporated, this Figure further decreases to around 569 MW/m^3 (Fig. 15b). Power density difference maps (Figs. 14c and 15c) elucidate substantial variations. Without BTI timing impact, the maximum power density difference following a decade of aging is roughly 5 MW/m^3 (Fig. 14c). With BTI aging timing impact taken into account, this difference substantially escalates to around 61 MW/m^3 (Fig. 15c). This noteworthy underestimation is further elucidated in Fig. 27b. Fig. 27a also highlights the corresponding underestimation in total power.

In summary, the pronounced decrease in power density observed upon incorporating BTI aging timing impact can be attributed to the following mechanism: BTI aging induces a gradual elevation in the threshold voltage ($V_{T\ H}$) of tran-sistors, which in turn leads to diminished switching speeds and an extended switching delay. This escalation in delay substantially influences the dynamic power consumption as mathematically represented by ($P_{\text{dynamic}} = C \cdot V^2 \cdot f$), with C denotes capacitance, and f signifies the operational frequency. An increase in

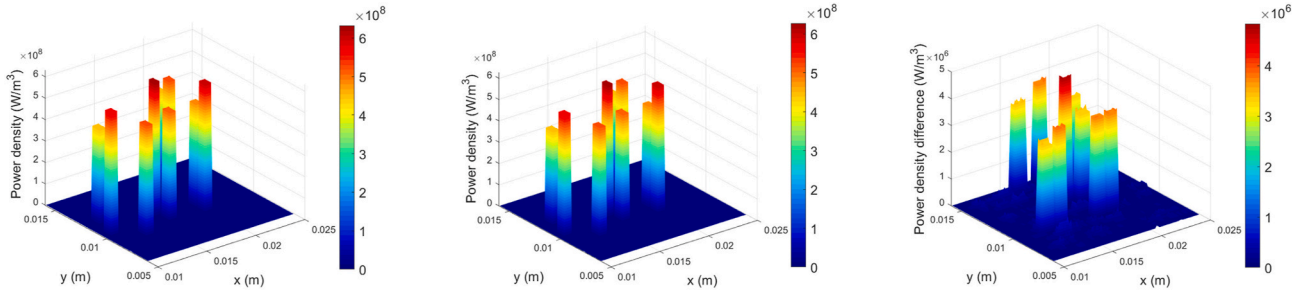


(a) DCT non-aging power density

(b) DCT with-aging power density including BTI timing effect

(c) DCT power density difference

Fig. 13. On-chip spatial power density and power density difference maps for DCT circuit at 130°C operating temperature library.

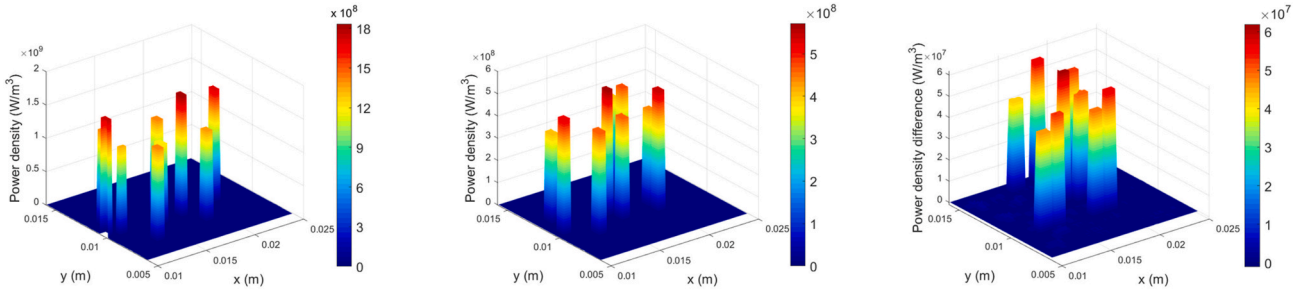


(a) DCT non-aging power density

(b) DCT with-aging power density without including BTI timing effect

(c) DCT power density difference

Fig. 14. On-chip spatial power density and power density difference maps for DCT circuit at 25°C operating temperature library.

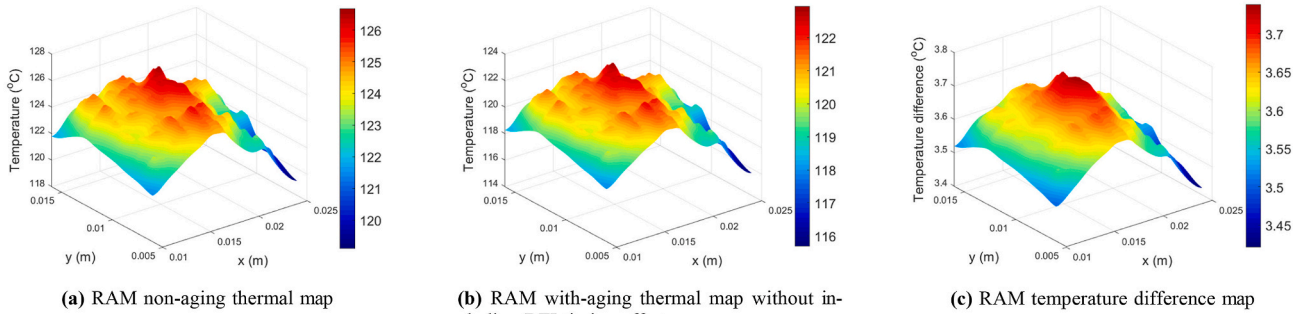


(a) DCT non-aging power density

(b) DCT with-aging power density including BTI timing effect

(c) DCT power density difference

Fig. 15. On-chip spatial power density and power density difference maps for DCT circuit at 25°C operating temperature library.

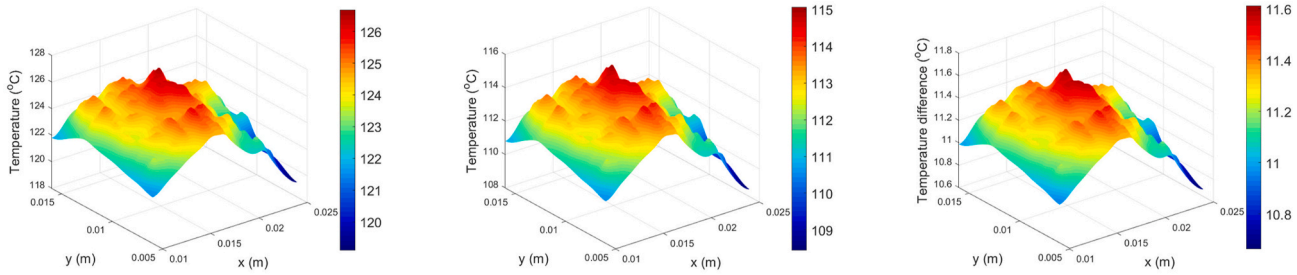


(a) RAM non-aging thermal map

(b) RAM with-aging thermal map without including BTI timing effect

(c) RAM temperature difference map

Fig. 16. On-chip spatial temperature and temperature difference maps for Dual port RAM circuit at 130°C operating temperature library.

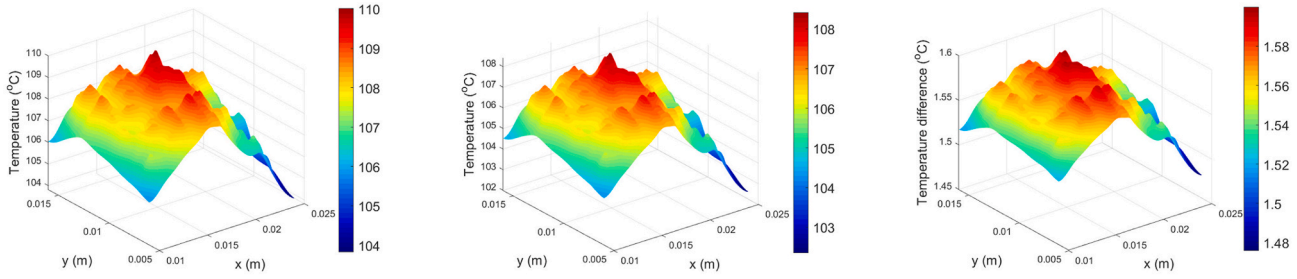


(a) RAM non-aging thermal map

(b) RAM with-aging thermal map including BTI timing effect

(c) RAM thermal difference map

Fig. 17. On-chip spatial temperature and temperature difference maps for Dual port RAM circuit at 130°C operating temperature library.

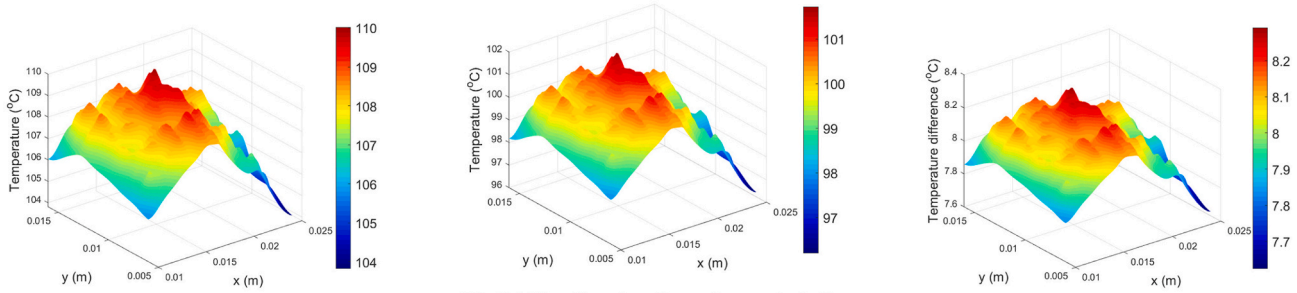


(a) RAM non-aging thermal map

(b) RAM with-aging thermal map without including BTI timing effect

(c) RAM temperature difference map

Fig. 18. On-chip spatial temperature and temperature difference maps for Dual port RAM circuit at 25°C operating temperature library.



(a) RAM non-aging thermal map

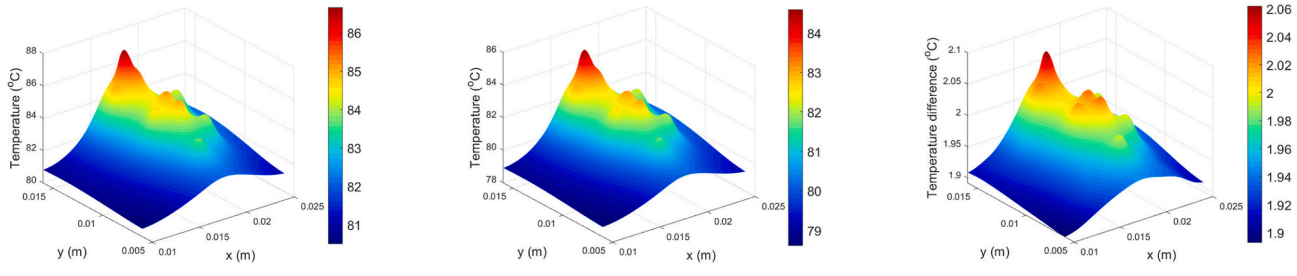
(b) RAM with-aging thermal map including BTI timing effect

(c) RAM thermal difference map

Fig. 19. On-chip spatial temperature and temperature difference maps for Dual port RAM circuit at 25°C operating temperature library.

delay inversely affects the effective frequency of operation (as elaborated in Section IV concerning RAM and DCT circuits), consequently impacting both dynamic and total power consumption more significantly. Consequently, power density, which is defined as the quotient of total power and unit area ($P_{total}/Area$), undergoes a notable alteration when the timing impact of BTI aging is accounted for.dd.

B. Impact of BTI for on-chip temperature map

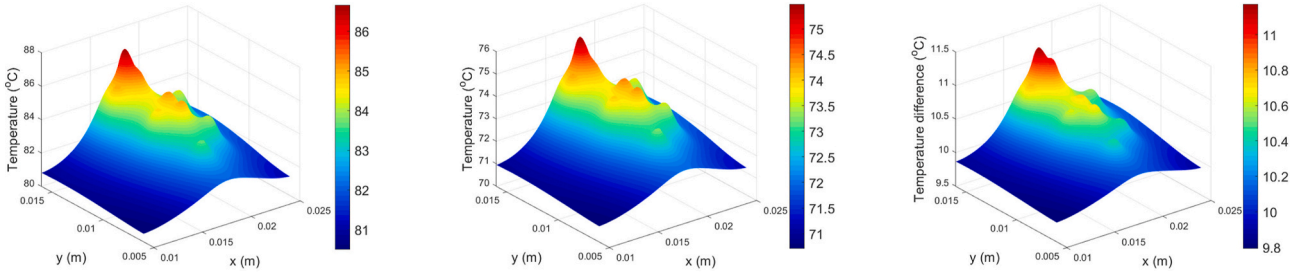


(a) DCT non-aging thermal map

(b) DCT with-aging thermal map without including BTI timing effect

(c) DCT temperature difference map

Fig. 20. On-chip spatial temperature and temperature difference maps for DCT circuit at 130°C operating temperature library.

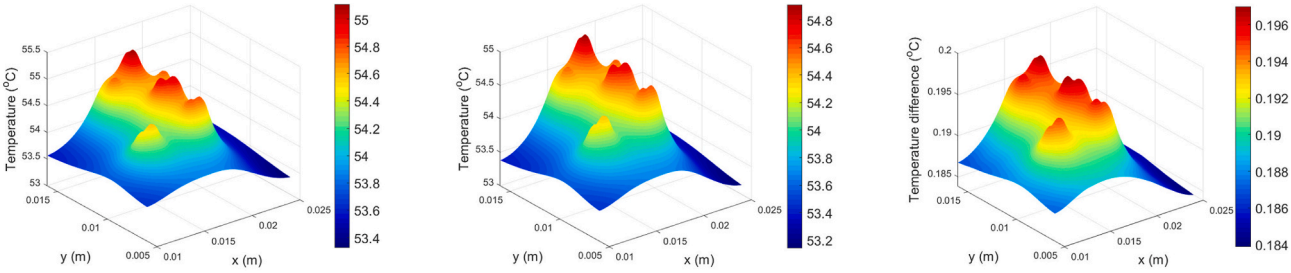


(a) DCT non-aging thermal map

(b) DCT with-aging thermal map including BTI timing effect

(c) DCT temperature difference map

Fig. 21. On-chip spatial temperature and temperature difference maps for DCT circuit at 130°C operating temperature library.

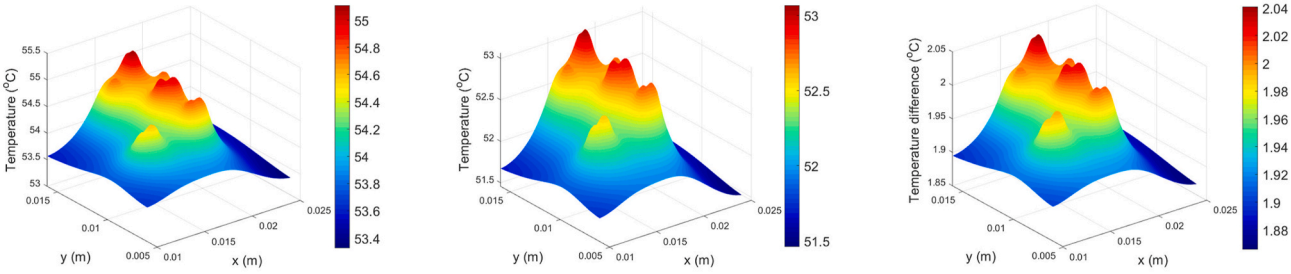


(a) DCT non-aging thermal map

(b) DCT with-aging thermal map without including BTI timing effect

(c) DCT temperature difference map

Fig. 22. On-chip spatial temperature and temperature difference maps for DCT circuit at 25°C operating temperature library.

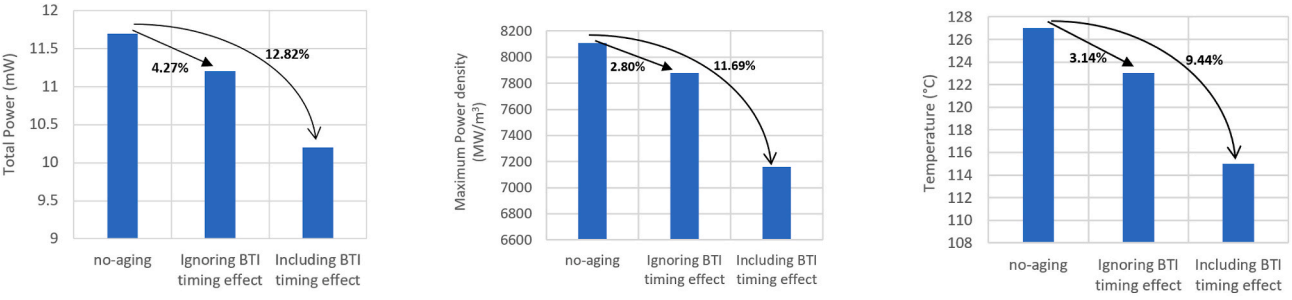


(a) DCT non-aging thermal map

(b) DCT with-aging thermal map including BTI timing effect

(c) DCT temperature difference map

Fig. 23. On-chip spatial temperature and temperature difference maps for DCT circuit at 25°C operating temperature library.



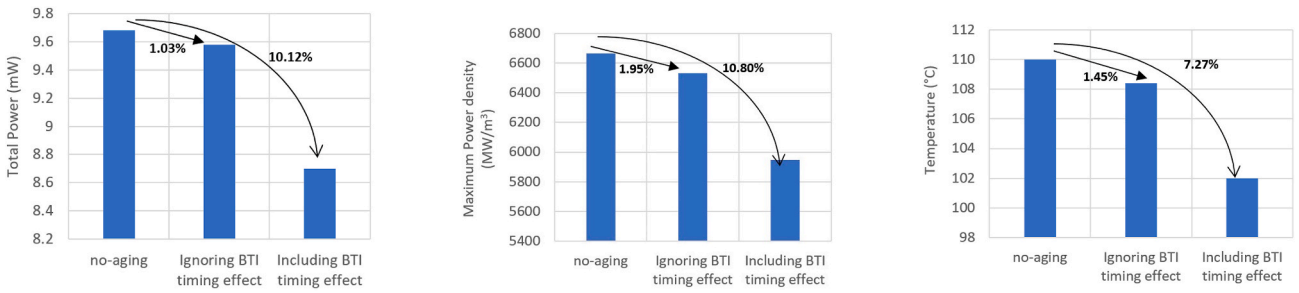
(a) RAM total power underestimation

(b) RAM power density underestimation

(c) RAM temperature underestimation

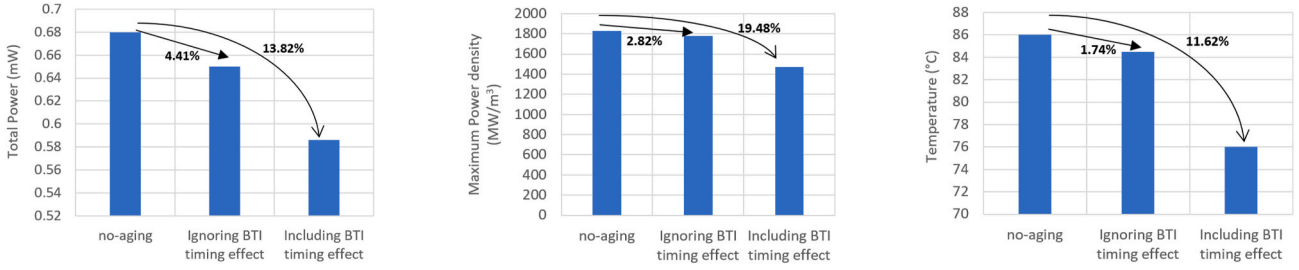
Fig. 24. On-chip spatial temperature and temperature difference maps for Dual port RAM circuit at 130°C operating temperature library.

1) RAM Circuit Analysis at *High Temperature:* Figs. 16 and 17 illustrate the spatial temperature distribution within the RAM circuit at high operating temperature (T = 130°C). The initial maximum temperature registers around 127°C (Figs. 16a and 17a). Without considering BTI timing impact after a decade of aging (Fig. 16b), this diminishes to approxi-mately 123°C. Incorporating BTI aging timing impact (Fig. 17b) further reduces it to 115°C. Temperature difference maps (Figs. 16c and 17c) emphasize the effect. Excluding BTI timing impact, the maximum temperature difference equals around 4°C (Fig. 16c). Conversely, when BTI aging-aware timing impact is factored in (Fig. 17c), the difference substantially increases to about 12°C. This highlights the critical role of considering BTI aging timing



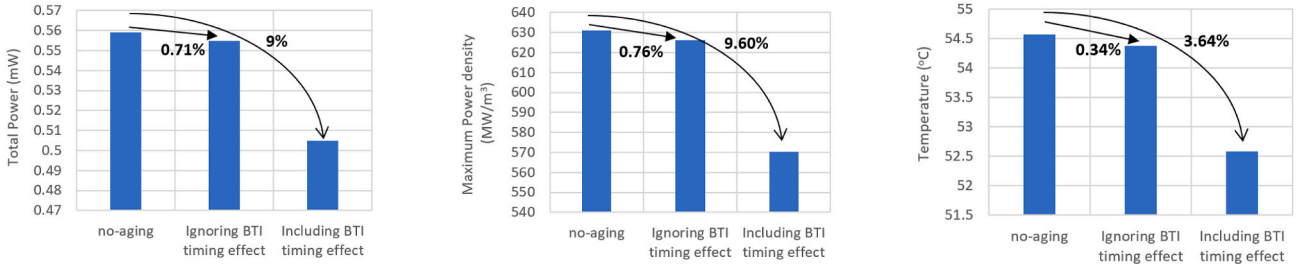
(a) RAM total power underestimation **(b)** RAM power density underestimation **(c)** RAM temperature underestimation

Fig. 25. On-chip spatial temperature and temperature difference maps for Dual port RAM circuit at 25°C operating temperature library.



(a) DCT total power underestimation **(b)** DCT power density underestimation **(c)** DCT temperature underestimation

Fig. 26. On-chip spatial temperature and temperature difference maps for DCT circuit at 130°C operating temperature library.



(a) DCT total power underestimation **(b)** DCT power density underestimation **(c)** DCT temperature underestimation

Fig. 27. On-chip spatial temperature and temperature difference maps for DCT circuit at 25°C operating temperature library.

and its potential to lead to significant underestimations, as underscored in Fig. 24c.

2) *RAM Circuit Analysis at low Temperature:* Similarly, Figs. 18 and 19 depict the temperature distribution within the RAM circuit at a lower operating temperature (T = 25°C). Initial observations reveal a peak temperature nearing 110°C (Figs. 18a and 19a)). Over a decade of aging, without considering BTI aging impact, the maximum temperature is approximately 108.5°C (Fig. 18b), while including BTI aging timing impact lowers it further to around 102°C (Fig. 19b). Temperature difference maps (Figs. 18c and 19c)) illustrate considerable variations. Without BTI timing impact, the maximum temperature difference after a decade of aging is approximately 1.5°C (Fig. 18c). With BTI aging timing impact considered, this difference increases significantly to around 8°C (Fig. 19c). Fig. 25c elaborates on this marked underestimation.
3) *DCT Circuit Analysis at High Temperature:* In a parallel vein, Figs. 20 and 21 exhibit the spatial temperature distribution within the DCT circuit at high operating temper-ature (T = 130°C). The initial maximum temperature measures around 87°C (Figs. 20a and 21a). Without considering BTI timing impact after a decade of aging (Fig. 20b), this reduces to approximately 85°C. With BTI aging timing impact considered, it further decreases to around 76°C (Fig. 21b). Temperature difference maps (Figs. 20c and 21c) spotlight the difference. Not accounting for BTI timing impact, the max-imum temperature difference approximates 2°C (Fig. 20c). Contrastingly, with BTI aging-aware timing impact considered (Fig. 21c), the difference magnifies significantly to about 11°C. This reiterates the importance of factoring in BTI aging timing and its potential to lead to substantial underestimations, as illuminated in Fig. 26c.
4) *DCT Circuit* Analysis *at low Temperature:* Likewise, Figs. 22 and 23 present the temperature distribution within the DCT circuit at a lower operating temperature (T = 25°C). Initial assessments unveil a peak temperature of 55°C (Figs. 22a and 23a). After a decade of aging, without considering BTI aging impact, the maximum temperature is approximately 54.8°C (Fig. 22b). With BTI aging timing impact incorporated, this Figure further decreases to around 53°C (Fig. 23b). Temperature difference maps (Figs. 22c and 23c) elucidate substantial variations. Without BTI timing impact, the maximum temperature difference following a decade of aging is roughly 0.196°C (Fig. 22c). With BTI aging timing impact taken into account, this difference substantially escalates to around 2°C (Fig. 23c). This noteworthy underestimation is further elucidated in Fig. 27c.

6. Conclusion

In this article, we have conducted a comprehensive in-vestigation into the impact of BTI aging on the on-chip spatial power density and temperature for two widely used circuit functional blocks, Dual port RAM and the Discrete Cosine Transform (DCT) block, under operating conditions of T = 130°C and T = 25°C to account for worst-case BTI degradation for 10 years. Our experimental findings reveal that BTI aging for the sequential RAM circuit results in an approximately 13 % reduction in total power, a 12 % decrease in maximum power density, and a 10 % decline in maximum temperature at an operating temperature of 130°C. Similarly, at an operating temperature of 25°C, we observe reductions of about 10 % in total power, 11 % in maximum power density, and 7 % in maximum temperature due to BTI aging. For the DCT circuit, our analysis indicates a reduction of 14 % in total power, a 20 % decrease in maximum power density, and a 12 % decline in maximum temperature at 130°C operating temper-ature. At 25°C operating temperature, we observe reductions of 9 % in total power, 9.5 % in maximum power density, and 3.6 % in maximum temperature due to BTI aging. Furthermore, our investigation reveals that the location of maximum power density and the hot spot within a specific circuit re-mains consistent due to aging. However, the locations vary among different circuits, depending on their respective workloads. Notably, the impact of BTI aging is more pronounced at high operating temperatures (T = 130°C) compared to low operating temperatures (T = 25°C). These findings highlight the critical role of BTI aging effects on power density and temperature profiles in VLSI chips, emphasizing the need for aging-aware thermal and power management strategies in contemporary chip design.

7. Submission note

Some preliminary results of this work have been published in 2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) [16], which focuses on aging impacts on the spatial power and temperature for combinational circuits or without the circuit's timing considerations. This submission extended this work to thoroughly study sequential circuits like RAM and DCT circuit function blocks. As a result, this is more comprehensive and provides a more detailed analysis. Nevertheless, we would like to point out the significant differences between this submission and [16], and we believe that the difference is more than 40%. Specifically, this submission has the following significant changes and updates compared to the early conference version.

1) In this investigation, we conducted an exhaustive anal-ysis of the aging effects due to Bias Temperature In- stability (BTI) in sequential circuits, such as the Dual Port RAM and DCT circuit. In contrast to previous research [16], where the timing impact of BTI aging was not taken into account, we incorporated it in our study to achieve a more accurate assessment of the cumulative effects of BTI aging on various metrics, including total power consumption, on-chip spatial power density, and temperature profiles.

2) Given the critical role of timing in sequential circuits, we emphasize the necessity of accounting for BTI agingaware timing impacts in our analysis. To precisely evaluate BTI aging effects on total power consumption, onchip spatial power density, and temperature distribution, we demonstrate the vital importance of incorporating BTI aging-aware timing considerations. Disregarding this crucial aspect can result in substantial underestimations. Consequently, we introduce Section IV in this paper to provide comprehensive insight into our methodology.

3) Given the Increased sensitivity of BTI aging outcomes to variations in operating temperature, our investigation meticulously evaluates the impact of temperature across two contrasting extremes: high operating temperature (T=130°C) and low operating temperature (T=25°C). Our analysis underscores the observation that the effects of BTI aging on total power, on-chip spatial power density, and temperature profiles are notably more pronounced under high operating temperature conditions.

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CRediT authorship contribution statement

Sachin Sachdeva: Conceptualization, Methodology, Investigation, Software, Writing – original draft, Validation. **Jincong Lu:** Methodology, Validation. **Hussam Amrouch:** Resources, Validation. **Sheldon X.-D. Tan:** Supervision, Project administration, Funding acquisition, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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