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Recent advances in EM and BTI induced reliability modeling, analysis and optimization (invited)☆

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ABSTRACT

In this article, we will present recent advances in reliability effects such as electromigration on interconnects and Negative/Positive Bias Temperature Instability (N/P BTI) effects on CMOS devices, which are the most important reliability concerns for VLSI systems specifically at the nanometer regime. We will start with the grand reliability challenges facing the semi-conductor and computing industry. Then, we will first present recent advances in the electromigration (EM) modeling and assessment techniques at the circuit level, the full-chip level and the system level. We will focus on the recently proposed advanced EM modeling techniques including stress-oriented physic-based EM models, EM modeling considering the time-varying temperature and current density changes, EM recovery effect modeling, the more general physics-based 3-phase EM models and the finite-difference-method based numerical analysis technique for dynamic EM stress analysis. Then we will present recent developments for dynamic reliability management at the system level, where EM-induced lifetime and performance can be traded off and the EM recovery effects can be leveraged for a longer lifetime on different computing platforms.

For BTI effects, we will briefly explain the key mechanisms behind it first. Then, we will demonstrate how to bring *aging-awareness* to EDA tool flows based on our so-called degradation-aware cell libraries. Afterwards, we will present the impact of BTI effects on the leakage and dynamic power showing that BTI impact not only affects circuits' delay over time (as in the traditional view), but also the overall power of circuits. Towards removing guard-bands and hence increase the efficiency, we will present how aging-induced stochastic timing errors can be translated into deterministic and controlled approximations in which aging effects are suppressed with a minimum loss in quality. Finally, we will demonstrate *short-term aging effect* which is a recent discovery that is hardly explored until now. In fact, *short-term* aging effects are a paradigm shift in BTI from sole long-term reliability degradation, which is observable in the order of months and years as in the traditional view, to an emerging reliability degradation, which is observable in a significantly smaller time domain in the order of milliseconds and even microseconds. Some of the developed EM models and assessment programs can be downloaded at https://github.com/sheldonucr/physics_based_em_assessment_analysis. The developed aging models, degradation-aware cell libraries, reliability framework, etc. are publicly available at: http://ces.itec.kit.edu/dependable-hardware.php. They are ready to be directly used with existing EDA tool flows like Synopsys without requiring any modifications.

1. Introduction

Reliability has become a major design challenge and limiting factor for nanometer VLSI designs due to the high failure rates in deep submicron and nanoscale devices. It is expected that the future chips would show signs of reliability-induced aging much faster than previous generations. Among many reliability effects, the most concerning are electromigration (EM) in interconnects and Bias Temperature Instability (BTI) for CMOS devices as a result of increasing power density and aggressive transistor scaling. In fact, as technology nodes were being reduced to below 45 nm, the quality of the gate dielectric became severely less leading to higher leakage currents due to tunneling. To overcome this problem, manufacturers like Intel replaced silicon dioxide with the so-called "high-k material"

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which is a new kind of materials composition that gives a higher dielectric constant [1]. However, the susceptibility of transistors to strain/stress in such new materials (e.g., HfO_2) is higher than the older materials (e.g., SiO_2) [2,3]. For instance, measurements [2] demonstrated that the using the new high-k material results in higher degradation with respect to Positive Bias Temperature Instability (PBTI) and a similar degradation with respect to Negative Bias Temperature Instability (NBTI). As a result, scaling in conjunction with high-K materials has made aging phenomena that have often been assumed to be negligible become noticeable.

Electromigration failure of interconnects has been a long-standing concern for the development of highly reliable VLSI systems. Despite intense efforts from both industry and academia following the first observation of EM-related failure of Al circuit interconnects by James Black [4], it has proven impossible to find a robust process solution by material modification for either Al or the more recently introduced Cu metal system. EM failure can only partially be mitigated with process solutions and ultimately needs to be controlled and managed at circuits and even system levels in a cross-layer a fashion. The International Technology Roadmap for Semiconductors (ITRS 2014) predicts that the lifetime of wires due to EM will decrease by half for each new generation as shown in Fig. 1, which shows the actual and predicted lifetime scaling versus interconnect geometry [5]. It has been predicted that EM failure will become more significant for interconnects in FinFET based technologies at 10 nm and it is urgent to address this “EM crisis” which has recently prompted intense efforts to develop more robust interconnect materials, structures and design solutions [6,7].

Traditional compact EM checking approaches such as Black's equation [4] and Blech product [8] can lead to significant over-design [9]. These conservative design rules are not suitable for future technology scaling since more design guard bands are required for chip timing accuracy, and thus such a worst-case design methodology results in inefficiency and considerable penalties in the area, performance, power, and reliability budgets. Therefore, during the design process, a balance must be found to ensure circuit performance without seriously impairing electromigration reliability. Achieving this balance requires a thorough fundamental understanding of EM physics kinetics and the dominant factors for the failure process.

In this article, we review some of the recent advances in EM modeling and cross-layer EM-induced dynamic reliability management techniques and recent BTI modeling and optimization techniques. The review article does not intend to cover all the recent development for the EM and BTI related topics. The topics not covered in this article does not diminish their contributions and values to the communities.

The article is organized into two major sections: Section 2 for EM related modeling, analysis and optimization and Section 3 presents the BTI impacts on circuits.

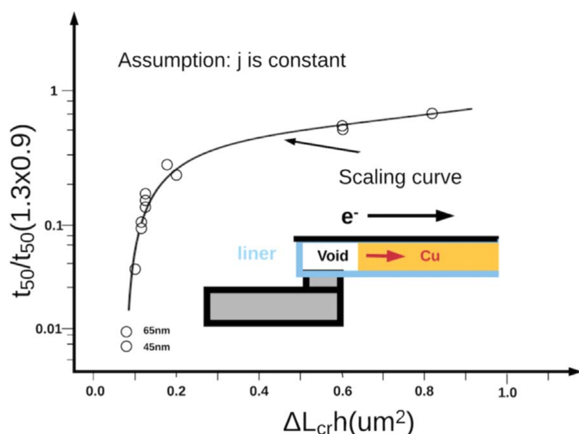

Fig. 1. The lifetime of interconnect wires versus technology nodes by ITRS2014.

Specifically, for the first EM Sections 2, 2.1 reviews the classic EM physics and existing EM failure models and discusses limitations of those models. Section 2.2 reviews the mainstream stress-based modeling of EM failure kinetics and the important Korhonen's equation. It further presents the physics-based EM models and recently proposed physics-based compact EM models and more accurate physics-based three-phase EM model. Section 2.3 present the recently proposed compact two-phase EM models and the more general three-phase EM models, which can better describe the wire EM-induced resistance changes over time. Section 2.4 introduces the dynamic EM model to consider transient stress evolution when the wires are stressed under time-varying current flows and the EM recovery effects. We also present a parameterized new equivalent DC current based EM model to consider the recovery and transient effects. Section 2.5 gives the closed form expressions (for the Korhonen's equation) for stress evolution over time for some commonly seen multi-segment wires based on Laplace transformation method. Section 2.6 introduce another closed form solutions to the Korhonen's equation for stress developments of multi-segment wires in a straight line using the integral transformation method. Section 2.7 presents the new voltage-based steady-state EM-induced stress analysis and new EM immortality check method for general interconnect trees. Section 2.8 presents the recently developed finite difference based analysis technique for Korhonen's equations. Section 2.9 shows the recently developed EM-induced dynamic reliability management and energy or lifetime optimization techniques for many-core dark silicon microprocessors and datacenters.

For the second BTI Section 3, we start in Section 3.1 by explaining briefly the key mechanisms at the physical level behind aging phenomena. Then, in Section 3.2 we demonstrate the impact of aging-induced degradation on the performance and power of circuits. Afterwards, we show in Section 3.3 the ultimate impact of aging effects at the system level. We also show how approximate computing principles can be applied to translate stochastic aging-induced timing errors into deterministic and controlled approximations. In Section 3.4 we show how BTI effects in conjunction with voltage scaling can result in short-term reliability degradation leading to transient errors akin to the temporal violation of aging guardbands at the moment of voltage switch. Finally, Section 4 concludes the article.

2. Electromigration (EM) modeling, analysis and optimization

2.1. Electromigration fundamentals

Electromigration (EM) is a physical phenomenon of the oriented migration of metal (Cu) atoms along a direction of applied electrical field due to the momentum exchange between atoms and the conducting electrons. Atoms (either lattice atoms or impurities) migrate toward the anode end of the metal wire along the trajectory of conducting electrons. This oriented atomic flow results in metal density depletion at the cathode, and a corresponding metal accumulation at the anode end of the metal wire. This depletion and accumulation happen because atoms cannot easily escape the metal volume as the metal wires are confined by the so-called diffusion barriers. A Cu damascene interconnect wire typically is confined or embedded by metallic barriers such as Ta and capped with either a dielectric (such as SiN) or a metallic layer (CoWP) as shown in Fig. 2.

As a result, the wire volume changes, which is induced by the atom depletion and accumulation due to migration leading to build-up of hydrostatic stresses across the conductor resulting in tension at the cathode end and compression at the anode end of the wire [10–12]. Over time, the continuous unidirectional current flow increases these stresses, as well as the stress gradient along the metal line. The stress gradient actually serves as the back-force to reduce the EM-induced metal migration flow. In some cases, usually when a wire is long or

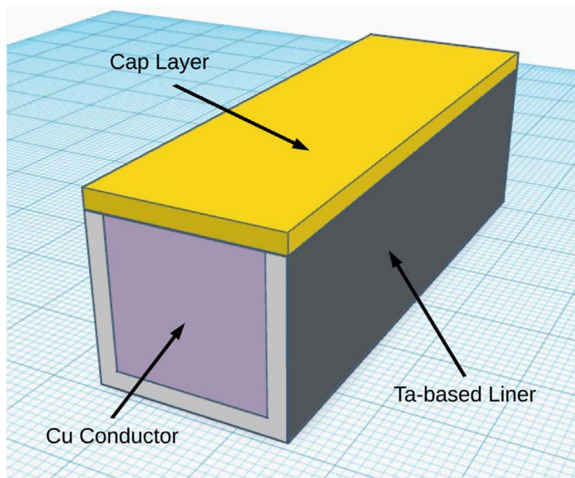

Fig. 2. The 3D view of the confined Cu damascene structure with barrier and capping layers.

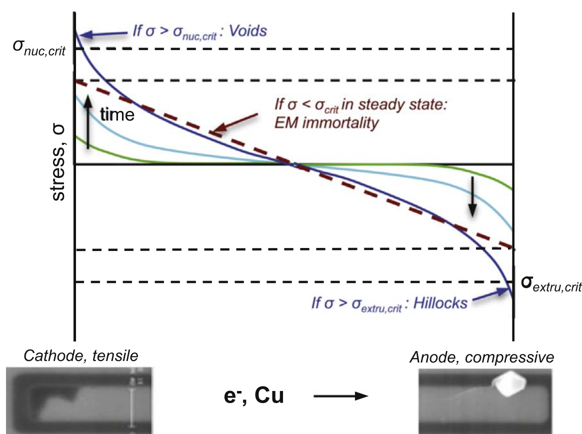

Fig. 3. The stress development and distribution in EM, [13].

current is large, this stress can reach critical levels, resulting in a void nucleation at the cathode and/or hillock formation at the anode end of wire as shown in Fig. 3. Voids are typically formed when existing cohesive or inter-facial micro-cracks near, or at, the barrier/Cu interfaces develop into a void by action of the appropriate stresses. On the other hand, a hillock is formed by compression-induced extrusion of metal into the surrounding dielectric which can cause a shortage between neighboring metal wires. EM can degrade both global interconnects such as power grid networks and signal wires when the current densities are sufficiently high (about 1 MA/cm^2). However, the power grid networks are more susceptible to EM effects due to the conduction of unidirectional currents.

The currently employed method of predicting the time to failure is based on the approximate statistical Black's equation [4].

$$MTTF = Aj^{-n}\exp\{E_a/k_BT\} \tag{1}$$

However, calculating the MTTF of individual branches characterized by known current densities and temperatures, is the subject of growing criticism. Here, j is the current density, k_B is the Boltzmann's constant; T is the absolute temperature; E_a is the EM activation energy. The symbol A is a constant, which depends on a number of factors, including grain size, line structure and geometry, test conditions, current density, thermal history, etc. Here current exponent n was found to be 2 by James Black. Typically, the values n and E_a are obtained at the highly stressed testing condition, then we can use them to extrapolate the MTTF at the use condition by using the following equation:

$$MTTF_{\text{use}} = MTTF_{\text{stress}}\left(\frac{j_{\text{stress}}}{j_{\text{use}}}\right)^n exp\left\{\frac{E_a}{k_B}\left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}}\right)\right\} \tag{2}$$

where $MTTF_{stress}$ and $MTTF_{use}$ are MTTF for the testing stress and normal use conditions respectively. However, it is today's common understanding that n is actually not constant over different stressing conditions (different current densities and temperatures) and its value has been highly debated in the past [14–17]. As a result, Black's equation does not scale very well over a wide range of current densities.

On the other hand, the Blech limit or Blech product [8]

$$(j \times L) \le (j \times L)_{\text{crit}} = \frac{\Omega\sigma_{\text{crit}}}{eZ\rho} \tag{3}$$

is used for the filtering out of immortal branches, which can only be applied to a single wire branch. Here, L is the wire branch length, Ω is the atomic volume; e is the electron charge, eZ is the effective charge of the migrating atoms, ρ is the wire electrical resistivity, σ_{crit} is the critical stress needed for void or hillock formation as a precursor to failure. The immortality condition of the Eq. (3) means that the atomic flux, generated by stress gradient in the metal lines characterized by $(j \times L) \le (j \times L)_{\text{crit}}$, compensates the atomic flux caused by electrical current density. It should be mentioned that the Blech limit is valid only for a single wire segment or branch within the diffusion blocking boundaries. It does not work for multi-segment interconnect trees, which are commonly used in practical VLSI layouts. An interconnect tree wire is defined as continuously connected metal (copper or aluminum) within one layer of metallization. These trees are terminated by diffusion barriers at vias and contacts and can have more than one terminating segment, as shown in Fig. 4. Existing EM modeling and analysis techniques mainly focus on the simple straight line interconnect with two line-end terminals. However, a practical integrated circuit layout often has interconnects such as clock and power grid networks containing many such interconnect tree wires. The EM effects in the segments of a wire are not independent and they have to be considered simultaneously.

To mitigate those mentioned problems, some physics-based EM analysis methods for the TSV and power grid networks have been proposed recently based on solving the basic mass transport equations [18–21]. Those model can give a better explanation for the resistance changes over time for a wire (modeled as the atomic concentration changes due to atomic flux). Since these proposed methods solve the basic mass transport equations using the finite element method, they can only solve for very small structures such as one TSV structure. As a result, a complicated look-up table has to be built for different TSVs and wire segments for full-chip power grid analysis at reduced accuracy.

Alternatively, a number of physics-based EM compact models have been proposed recently where void nucleation and void evolution are explicitly characterized, which is responsible for time-dependent resistance degradation of interconnect wires, which mitigates the major flaws in the Black-Blech models [22,23]. In the new approach, the EM

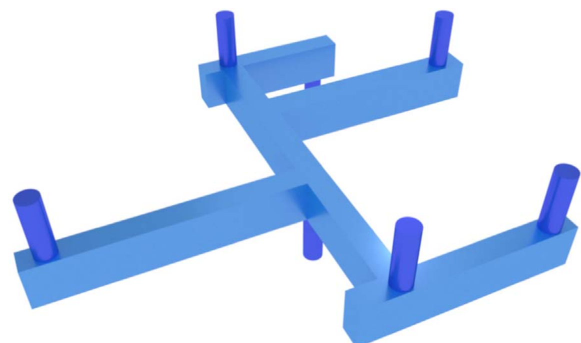

Fig. 4. Interconnect tree confined by diffusion barriers/liners.

process is characterized in two phases: void nucleation and a subsequent void growth. In the void nucleation phase, void nucleation time (t_{nuc}) is determined as an instant in time when stress at the cathode end of the line, characterized by the biggest tensile stress, reaches the critical stress [22]. In the void growth phase, the void starts to grow its volume at a velocity that is a function of temperature and its current density, which will lead to the resistance increase with time. In the following sections, we will give more detailed presentations for the proposed physics-based EM models.

2.2. Stress-based EM modeling and stress diffusion equations

In addition to the Black and Blech equations, which are semi-physics based EM models supported by early experimental results, many more physics models of electromigration phenomenon have been developed for new interconnect wiring structures. In this section, we present the most well-developed stress evolution based EM models characterized by the Korhonen's equation first. Then we will present recently developed physics-based EM models and the new three-phase EM model, which is more consistent with the measured results for Cu damascene interconnect wires.

2.2.1. EM-induced material transport equation

Blech first observed in his experiments that the end of strips which carries current flow will drift with the following velocity, which is also the Nernst-Einstein equation [8,17]:

$$v_d = D_a\frac{F_{em}}{k_BT} = D_a\frac{eZ\rho j}{k_BT} \tag{4}$$

where F_{em} can be viewed as the EM-induced force due to the electronic wind. D_a is the atomic diffusion coefficient, which is given by

$$D_a = D_0\exp\left(-\frac{E_a}{k_BT}\right) \tag{5}$$

where D_0 is the diffusion coefficient and E_a is the EM activation energy. The flux of metal atoms during the EM mainly consists of two major forces, one is the electron wind induced force, F_{em} and the second one back-force due to the atomic concentration changes (or the stress gradients due to the depletion of atoms at the cathode end and the accumulation of the atoms at the anode end) [24,25]. Since the atomic migration occurs via a vacancy exchange mechanism, the material transport can be described in terms of a vacancy flux as follows:

$$\begin{aligned} J_v &= -D_v\nabla\cdot C_v + C_v v_d \\ &= -D_v\left(\nabla\cdot C_v - C_v\frac{eZ\rho j}{k_BT}\right) \end{aligned} \tag{6}$$

where D_v is the vacancy diffusivity, C_v is the vacancy concentration. Note that we ignore the transient force in (6) due to temperature gradients as EM is a long term effect and transient temperature has marginal impacts on it.

When the divergence occurs in vacancy flux due to the different diffusivities around metal grain boundaries, or pre-existing micro-cracks near or at the barrier(capping)/Cu interfaces, vacancies or metal atoms will accumulate or vanish, and in some cases void or hillocks can be formed as well. The vacancy continuity equation can be written as [26]

$$\frac{\partial Cv}{\partial t} = -\nabla\cdot J_v + G \tag{7}$$

where G represents a generation and annihilation term. Eq. (7) presents the fundamental EM-induced material diffusion equation.

2.2.2. One-dimensional stress evolution model

To simplify our presentation, we only consider the one dimensional case. However, the results can be extended to two or three dimensional cases easily. One important observation is that in today's interconnect wires, such as Cu damascene structures, the metal wires are confined by barriers or capping layers, thus, metal wire volume can't be changed as a result of the atomic/vacancy concentration changes. It follows then, that hydrostatic stress/strain will be developed in the metal wires. Instead of using the vacancy concentration, C_v, as the variables in (7), using the hydrostatic stress σ inside wires as the variables is more convenient as stress is directly related to the EM failure damage forming process (such as the critical stress concept).

Korhonen et al. [27] developed the simplified stress diffusion based EM models. Specifically, they show that the concentration of lattice sites (grain boundary dislocation), changes dC_L/C_L will lead to the stress increments due to Hooke's law:

$$\frac{dC_L}{C_L} = -\frac{d\sigma}{B} \tag{8}$$

where B is applicable modulus. Notice that $G = \frac{\partial C_L}{\partial t}$ in (7) [28], we have

$$-\frac{\partial J_v}{\partial x} = \frac{\partial C_v}{\partial t} + \frac{C_L}{B}\frac{\partial\sigma}{\partial t} \tag{9}$$

Assume that vacancy concentration in equilibrium is related with the mechanical stress as follows [26],

$$C_v = C_{v0}\exp\left(\frac{\Omega\sigma}{k_BT}\right) \tag{10}$$

As a result, we have

$$\frac{\partial C_v}{\partial t} = C_v\frac{\Omega}{k_BT}\frac{\partial\sigma}{\partial t};\ \frac{\partial C_v}{\partial x} = C_v\frac{\Omega}{k_BT}\frac{\partial\sigma}{\partial x}, \tag{11}$$

With (11), (9) becomes

$$-\frac{\partial J_v}{\partial x} = \frac{\partial\sigma}{\partial t}\left(\frac{C_v\Omega}{k_BT}\frac{\partial\sigma}{\partial t} + \frac{C_L}{B}\right) \tag{12}$$

If we substitute J_v defined in (6) into (12) with information from (11), we have following hydrostatic stress diffusion equation in partial differential form:

$$\frac{\partial\sigma}{\partial t}\left(\frac{C_v\Omega}{k_BT} + \frac{C_L}{B}\right) = \frac{\partial}{\partial x}\left[D_vC_v\left(\frac{\Omega}{k_BT}\frac{\partial\sigma}{\partial x} - \frac{eZ\rho j}{k_BT}\right)\right] \tag{13}$$

Korhonen noticed that $(C_V/C_L)(\Omega B/k_BT)\ll 1$ and $C_L = C_v = 1/\Omega$ and $D_a = D_vC_v/C_L$ [27], he obtained the Korhonen's equation

$$\frac{\partial\sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_aB}{k_BT}\left(\Omega\frac{\partial\sigma}{\partial x} - eZ\rho j\right)\right] \tag{14}$$

Korhonen's equation completely describes how the hydrostatic stress develops in confined metal wires with material flux blocked at the barrier terminals such as vias. It can be applied to a single wire in one-dimensional case and multi-segment wires in 2-dimensional cases, which will be discussed in the sequel soon.

Fig. 5 shows stress evolution for a single wire line over time obtained from the Korhonen's equation. The steady state will be reached when the backward flux compensates the current-induced flux, and the stress will be linearly distributed along the wire. Fig. 5(a) shows the stress evolution along the wire (with the left end as the cathode node and right as the anode node). This is a typical hydrostatic stress evolution pattern driven by DC current. Fig. 5(b) shows the evolution of the electric current induced hydrostatic stress at the cathode end of a metal wire (biggest tensile stress) under different DC densities and temperatures. It indicates that both the current density and the temperature affect the stress evolution rate. Table 1 shows the parameters used for the simulation from the Fig. 5.

For Korhonen's equation, if we consider a simple line wire of length L with the blocking boundary conditions at the two blocked ends located at $x = 0$ and l and initial condition:

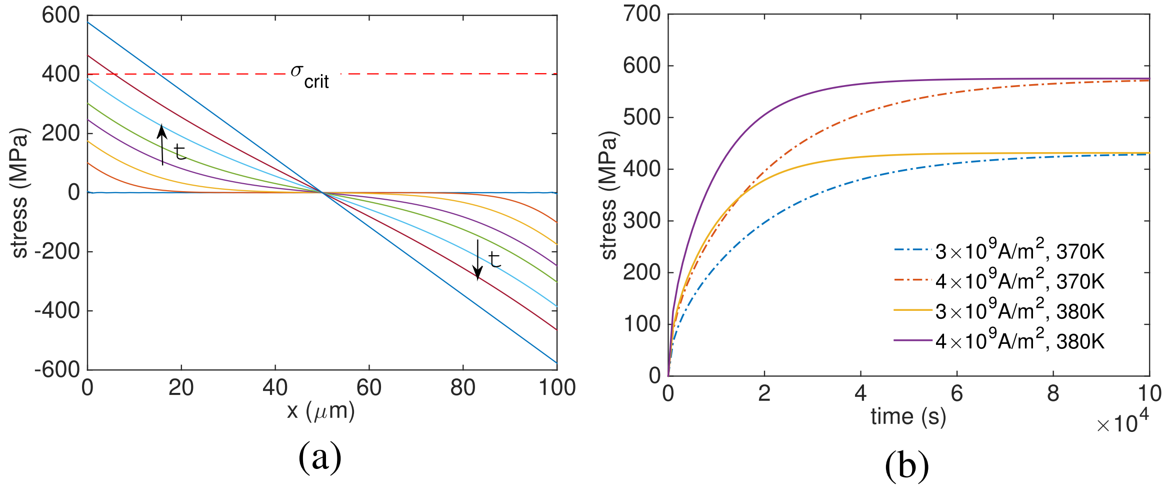

Fig. 5. Evolution of hydrostatic stress along the wire, (a), and at the cathode end, (b), over time stressed under different current densities and temperatures, in the case of zero initial stress [29].

Table 1
Parameters and typical values used.

Parameter	Value	Parameter	Value
E_a	0.86 eV	B	1×10^{11} Pa
Z	10	Ω	1.66×10^{-29} m^3
σ_{crit}	400 MPa	ρ	3×10^{-8} Ω
l	1×10^{-4} m	D_0	7.56×10^{-5} m^2/s

$$J_v(0, t) = J_v(L, t) = 0$$
$$\sigma(x, 0) = \sigma_T \tag{15}$$

where σ_T is the thermal stress developed in the metal line during cooling from the zero stress temperature T_{ZS} down to the temperature of use condition. The exact analytic solution of this initial-boundary value problem for a finite wire can be found as

$$\sigma = \sigma_T + \frac{eZ\rho jL}{\Omega}\left[\frac{1}{2} - \frac{x}{L} - 4\sum_{n=0}^{\infty}\frac{\cos\left(\frac{(2n+1)\pi x}{L}\right)}{(2n+1)^2\pi^2}e^{-\kappa\frac{(2n+1)^2\pi^2}{L^2}t}\right] \tag{16}$$

2.3. Compact physics-based EM model for a single wire

In this section, we present the compact physics-based EM models and time to failure assessment methods for a single wire based on the stress-based EM modeling techniques developed in Section 2.2

2.3.1. Physics-based two-phase EM model

As mentioned earlier in Section 2.1, the EM failure process consists of two important phases: the void nucleation phase and void growth phase. When current is applied to a wire, stress starts to build up in the wire based on Korhonen's equation.

Void nucleation phase: At the cathode end of line (where $x = 0$), the tensile stress will start to increase over time. When the tensile stress reaches the critical stress $\sigma_{\rm crit}$, the void will be nucleated. To determine the nucleation time t_{nuc}, one can take the first term, which is assumed to be dominant term, to solve for t_{nuc} (16) [22,30]

$$t_{\rm nuc} \approx \frac{L^2 k_B T}{2D_a B\Omega}\ln\left[\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_T + \frac{eZ\rho jL}{2\Omega} - \sigma_{\rm crit}}\right] \tag{17}$$

Void growth phase: For the void growth phase, which follows the nucleation phase, voids are formed at t_{nuc} and grow at $t > t_{nuc}$. In this phase, the wire resistance may start to increase over the time. The void growth phase can also be described by the Korhonen's equation with different boundary conditions. In the following, we present a simple void growth model. Since the drift velocity of the void edge relates to atomic flux as shown in (4). A confined Cu wire structure with the marked width and length and height are shown in Fig. 6, where the Cu wire is confined by the highly resistive barrier layer (such as Na/TaN) with a capping layer (such as SiN) (which is typically dielectric with very high resistance, so its resistance can be ignored) at the top.

The wire resistance change can be approximately described as [31]:

$$\Delta r(t) = v_d(t - t_{nuc})\left[\frac{\rho_{Ta}}{h_{Ta}(2H + W)} - \frac{\rho_{Cu}}{HW}\right] \tag{18}$$

Here ρ_{Ta} and ρ_{Cu} are the resistivity of the barrier material (Ta/TaN) and copper, W is the line width, H is the copper thickness, and h_{Ta} is the barrier layer thickness.

The evolution of void growth and wire resistance is a pretty complicated process due to many failure mechanisms. Actually, void nucleation is a necessary condition for wire resistance changes, not a sufficient condition, as the void growth may stop (saturate) before the void volume can lead to significant wire resistance change. During the void growth process, the stress gradient will produce a back flow atomic drift velocity, v_b, so the total drift velocity, d_t, is given by [32]

$$v_t = v_d - v_b = \left(j\rho eZ - \frac{\Delta\sigma\Omega}{L}\right)\frac{D_a}{k_B T} \tag{19}$$

where $\Delta\sigma$ is the back-flow stress and L is the wire length. Once the wire-stress gradient balances the EM driving force (i.e. $v_t = 0$), metal atom depletion will stop. Korhonen et al. derives the maximum void volume in the one dimensional case, V_{max} [27] as

$$V_{max} = \frac{\sigma_T L}{B} + \frac{j\rho eZL^2}{2\Omega B} \tag{20}$$

where σ_T is the initial thermal stress.

In addition, EM failure due to void-induce damage, void nucleation locations is statistically correlated to the electronic flow direction. As a

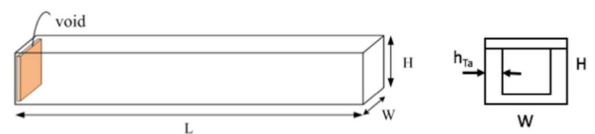

Fig. 6. The structure of a confined Cu damascene wire.

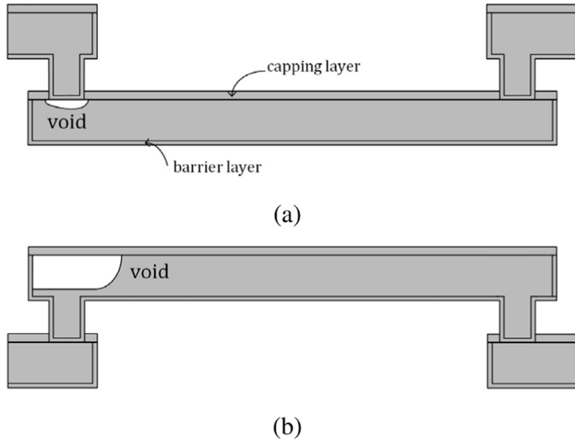

Fig. 7. Side-view of void formation: (a) void in a via-above line (early failure mode); (b) void in a via-below line (later failure mode).

result, there is so-called EM early failure or EM late failure of the wire [33]. Early failure typically happens in via-to via structure as shown in Fig. 7(a), when the void forms in a via-above line (the void is also called slit-voids) and reaches critical size [34,35], which equals to via's diameter, the via is blocked by the void and thus electronic connection to the upper layer is also blocked (capping layer is fabricated with dielectrics such as Si_3N_4 which does not shunt current flow). Late failure typically happens in so-called via-below structure as shown in Fig. 7(b), when the void typically forms in a via-below line (the void is also called trench voids) and reaches critical size, current can still go through the barrier layer (barrier layer is fabricated with Ta whose resistivity is much higher than Cu) and resistance will increase over time. However, statistically early failure can happen in via-below structure and late failure can happen in via up structure. Although the void can grow at these positions, the possibility is very low.

2.3.2. Physics-based three-phase EM models

The proposed two-phase EM models mentioned earlier still cannot completely describe the many observed wire resistance change behaviors from EM failure processes. Furthermore, we show in the section that the current density impacts on the stress developments is not consistent with the Korhonen's equation.

First, we show that the current exponent n computed by the Korhonen [27] is actually closer to 2, which is consistent with the measured data. Fig. 8 show the current exponent n from the numerical analysis results using COMSOL under different current densities. We found that this shows n is actually around 2 for different current densities. On the other hand, the compact EM models predicted by (17) gives different n values over current densities as shown in Fig. 8.

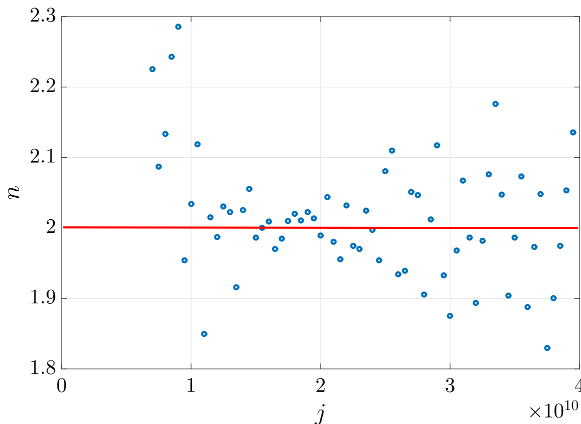

Fig. 8. Current exponent n fitting for Korhonen's equation.

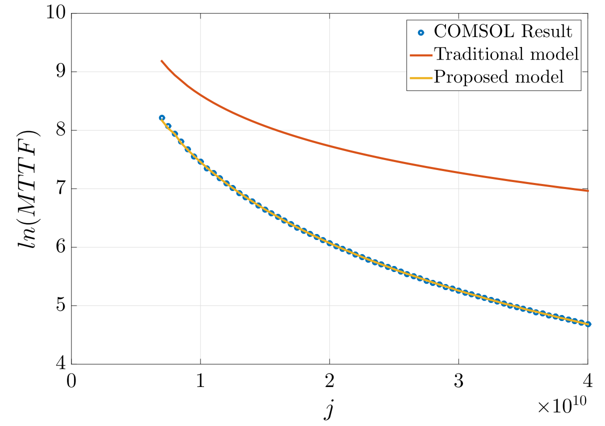

Fig. 9. Compare t_{nuc} in proposed model and COMSOL result.

To mitigate this problem, one way is just to keep the second order terms for the current density related term, which can be obtained by performed the Taylor's expansion on (17).

As a result, a more scalable physics-based compact model for nucleation can be obtained as

$$t_{nuc} \approx \frac{L^2 k_B T}{2 D_a \Omega B}\left(\frac{\gamma \alpha^2}{2}\right) \tag{21}$$

where $\alpha = \frac{\sigma_{crit} - \sigma_T}{\beta}$ and $\beta = \frac{eZ\rho jL}{2\Omega}$ and γ is a fitting parameter, which can be obtained by fitting with measured or computed results. Fig. 9 shows the compared result between our proposed model and the simulation result for one single wire. Here γ is found to be 0.78. As can be seen, this model is much closer to Korhonen's equation compared with the model in [31].

As mentioned above, the EM failure process in general can be viewed as two phases: the nucleation phase, in which void is generated after critical stress is reached, and the growth phase, in which void starts to grow. Existing compact EM models are also versed in terms of the two phases and each phase is described by time to failure as a function of current density and other parameters [15,36]. However, such a simple EM model ignores the fact that when the void is nucleated or formed, it will not change the wire resistance immediately. It is observed experimentally that there exists the so-called *critical void size* [34,35], which is typically the via size diameter or height or width of interconnect wires. Since the conductivity of Cu is much higher than the barrier layers, the resistance of wire does not change even there is a small void until the void grows into a point where its volume equals or becomes larger than the cross-section of the via or wire. Then all the current will starts to flow over the very thin barrier layer, which will lead to very higher current density and the resulted joule heating. The joule heating in turn will lead to small resistance jump, which indicated end of such period. Fig. 10(b) shows the experimentally measured resistance change over time. The small resistance jumps are obviously visible. Also, sometimes the barrier layers are not very stable due to the manufacturing process variations, causing the barrier layer to very quickly burn out completely once entire current flows through it. This will lead to an open circuit very quick as is shown in Fig. 10(b) [35].

As a result, we present more general physics-based three-phase EM model shown Fig. 10(a) [37]. In this model, there are three phases: (1) nucleation phase from $t = 0$ to t_{nuc}; (2) the incubation phase from t_{nuc} to the t_i; then (3) growth phase starting from t_i to t_{50}, t_{50} indicates the time to failure in statistical term (50% samples fail). In the following, we give the description of each phase.

(1) Nucleation phase: this is defined as time period from $t = 0$ (when the wire is stressed at $t = 0$) to t_{nuc}. In this phase, a void is not formed until time t_{nuc}. That means the resistance does not increase. The stress can be modeled by Korhonen's equation and the nucleation time can be estimated using the proposed new nucleation model in (21).

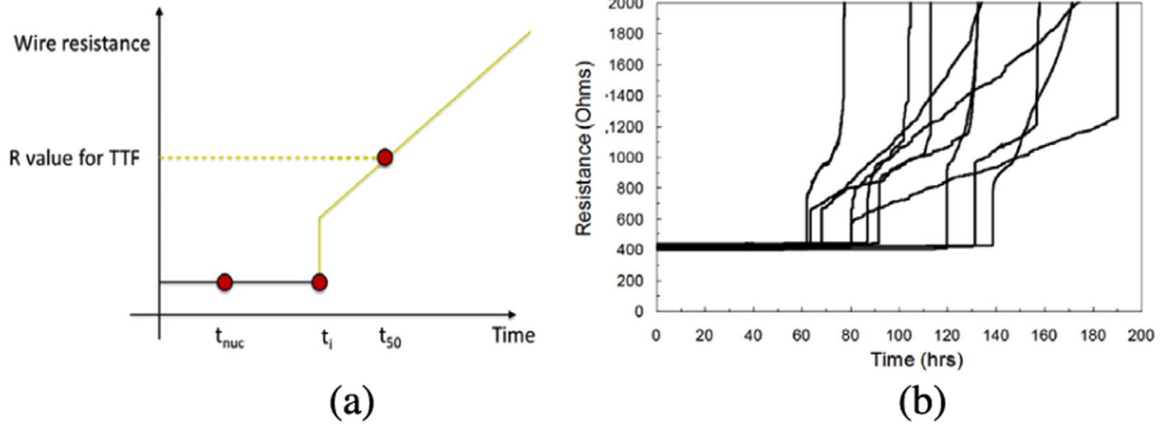

Fig. 10. (a) The 3-phase EM model and the resulting resistance change over time. (b) Measured resistance change, Courtesy of [35].

(2) Incubation phase: this is defined a time period from t_{nuc} to the t_i; In this phase, the void is nucleated, but its size is not significant and the void does not cover the cross section of via or the wire. Hence the resistance will remain almost the same. To model the incubation phase, we notice, the void growth rate v_d is given by the mobility (D_a/k_BT) times the electromigration driving force, which $F_e = eZE = eZ\rho j$, then we have [34]

$$v_d = \frac{D_a}{k_BT}F_e = \frac{D_a}{k_BT}eZ\rho j \tag{22}$$

Then the incubation time $(t_i - t_{nuc})$ can be expressed as:

$$t_i - t_{nuc} = \frac{\Delta L_{crit}}{v_d} \tag{23}$$

Here ΔL_{crit} is length of critical void size. It is noted that in this phase, since the approximated drift velocity v is proportional to current density j and the $t_i - t_{nuc}$ is related to j^{-1}.

We note that the incubation period defined in (23) better reflect the technology scaling impacts on EM, which predicts that life time of wires are reduced by half by each technology generation, characterized by the feature sizes, which is closely related to minimum via or wire sizes [38,34,39]. As a result, the new EM model is also scalable and predictable for technology scaling in addition to scalability in stressing current density.

(3) Growth phase: this is defined as time period from t_i to t_{50}. Aft the beginning of growth phase, the void reaches the critical void size and blocks the cross section above the via. Then the current starts to flow over the liner or barrier layers with much higher current density. As a result, the current density at the liner part can be much higher than other part of copper. Since resistivity of the liner is much larger than copper and this liner is very thin, current density and resistance on the linear can be very high. The high current density and higher resistance will lead to significant joule heating. It is observed that the temperature increase due to joule heating can be 5–15 °C [40], which will also lead to the wire resistance jump at the beginning of this phase we discussed.

After this jump, the resistance will increase linearly. For a combined Cu wire with liner such as Ta surrounding the three sides of the wire, using the same the drift velocity (v_d), the resistance change over time can be computed as [22] in Eq. (18)

To illustrate the 3-phase EM mode, we compute the resistance changes for the three phases over time. The results is shown in Fig. 11. As can be seen, after a period of time, the void is nucleated at 3800. At that time the resistance does not increase. When the void reaches the critical size, there is a resistance jump due to the joule heating at around 9800. Then the temperature increases 10 °C and the resistance jump is 3.86%. When the cross-section is blocked by void, the resistance begins to increase linearly. When the resistance is larger than 10% of the total resistance, the wire is considered failed.

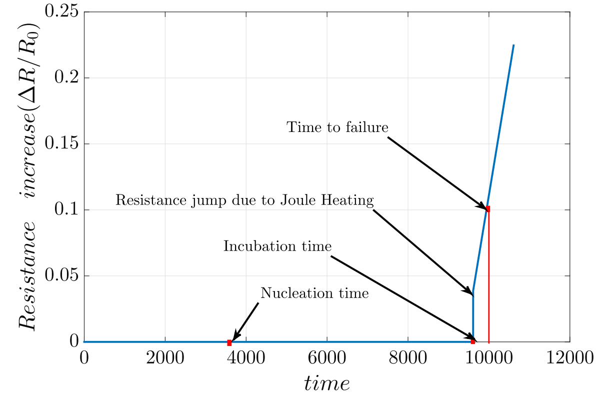

Fig. 11. The computed resistance change over time based on the proposed 3-phase EM model.

Another important observation is that the proposed 3-phase EM model leads to more accurate time to failure prediction over different current densities compared with experimentally observed data. Fig. 12(a) shows computed current density exponent n versus current density in log scale using proposed 3 phase EM model for the pre-void period (nucleation phase) and post-void period.

2.4. Transient EM simulation and EM recovery effect modeling

For practical chip working environments, the current and temperatures are now constant, which is assumed in the existing EM models. Also EM failure effects (like other long-term reliability effects), has the recovery effects when the wire is stressed with time varying current densities, which was shown in Fig. 13.

In this section, we consider transient effects on the EM stress evolution and made model based on this effect. We present the new physics based EM recovery models, which are derived from Korhonen's equation [29]. In the case of time-dependent current density, one-dimensional continuity equation Eq. (14) can be converted into the following nonhomogeneous form, [41]:

$$\frac{\partial\left(\sigma + \frac{eZ\rho j}{\Omega}(x - \frac{L}{2}) - \sigma_T\right)}{\partial t} - \kappa\frac{\partial^2}{\partial x^2}\left(\sigma + \frac{eZ\rho j}{\Omega}\left(x - \frac{L}{2}\right) - \sigma_T\right) = \frac{eZ\rho j}{\Omega}\left(x - \frac{L}{2}\right)\frac{\partial j}{\partial t} \tag{24}$$

with the boundary condition: $\frac{\partial\sigma}{\partial t}|_{x=0,L} = -\frac{eZ\rho j}{\Omega}$ and the initial condition: $\sigma(x, t = 0) = \sigma_T$. As it was shown in [41], the Eq. (24) can be solved analytically. The analytical solution for stress evolution kinetics takes the form:

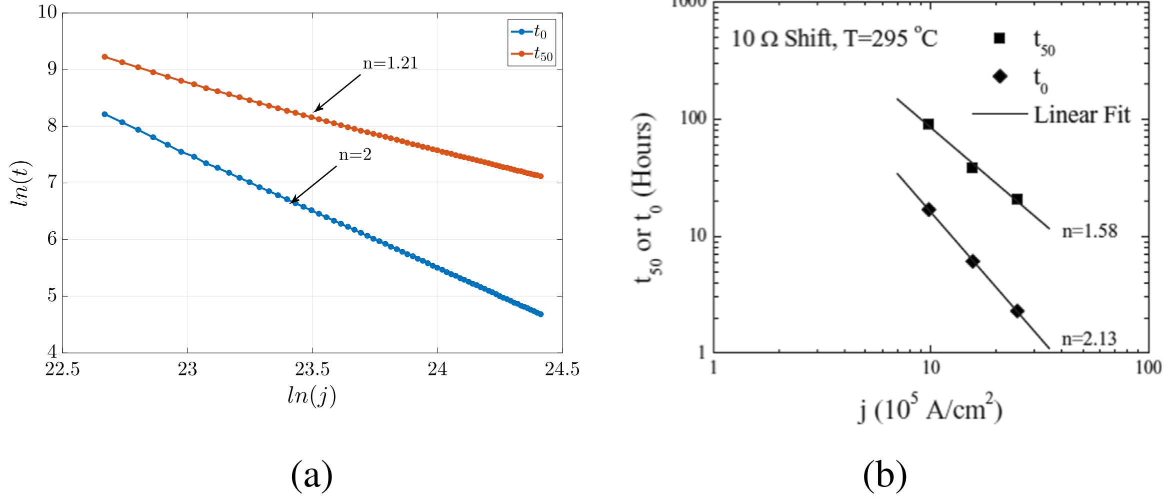

Fig. 12. (a) The computed current exponent values from the 3 phase EM model; (b) Measured current exponent values versus current densities, Courtesy of [16].

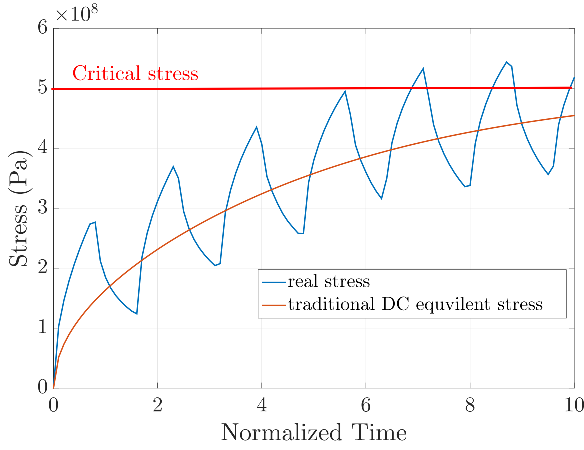

Fig. 13. Stress evolution caused by actual currents and traditional effective DC current.

$$\sigma(x,t_i)=\sigma_T+\frac{4eZ\rho}{\Omega L}\sum_{n=0}^{\infty}cos\frac{(2n+1)\pi x}{L}e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_i\tau}\times\left(\kappa_i\int_0^{\tau}j_ie^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_i\tilde{\tau}}d\tilde{\tau}+\phi(t_{i-1})\right)\tag{25}$$

where,

$$\phi(t_{i-1})=e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa(t)t_{i-1}}\kappa(t)\int_0^{t_{i-1}}j(t)e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa(t)\tilde{\tau}}d\tilde{\tau}$$

Here, $\kappa_i=\frac{D_0exp(-Ea/k_BT_i)B\Omega}{k_BT_i}$, where T_i is the constant temperature value during time interval $[t_{i-1},t_i]$ and $\kappa(t)=\frac{D_0exp(-Ea/k_BT(t))B\Omega}{k_BT(t)}$, where $T(t)$ describes the temperature variation during the period of time $[0,t_{i-1}]$.

However, for most interconnects, the driving currents are periodic. A recovery model for periodic pulse current is also proposed in this work. $j(t)$ is current density over time which is assumed to be

$$j(t)=\begin{cases}j_1, & mP\le t<mP+t_1,\\ j_2, & mP+t_1\le t<(m+1)P,\end{cases}\tag{26}$$

j_1 and j_2 are current densities for corresponding phase, P is the period of the current waveform. Temperature is $T(t)$ which can be written as

$$T(t)=\begin{cases}T_1, & mP\le t<mP+t_1,\\ T_2, & mP+t_1\le t<(m+1)P,\end{cases}\tag{27}$$

And T_1 and T_2 are corresponding temperature for each phase.

The stress evolution for two phase periodic pulse current recovery model proposed in that work [29] is

- **If** $mP\le t<mP+t_1$ $(\tau=t-mP)$:

$$\sigma(x,t)=\sigma_T+\frac{4eZ\rho}{\Omega L}\sum_{n=0}^{\infty}\cos\frac{(2n+1)\pi x}{L}e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_1\tau}\times\left(\kappa_1\int_0^{\tau}j_1e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_1\tilde{\tau}}d\tilde{\tau}+M\phi_P\right)\tag{28}$$

where,

$$\phi_P=e^{-\frac{(2n+1)^2\pi^2}{L^2}(\kappa_1t_1+\kappa_2t_2)}\kappa_1\int_0^{t_1}j_1e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_1\tilde{\tau}}d\tilde{\tau}+e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_2t_2}\kappa_2\int_0^{t_2}j_2e^{\frac{(2n+1)^2\pi^2}{l^2}\kappa_2\tilde{\tau}}d\tilde{\tau}$$

- **If** $mP+t_1\le t<(m+1)P$ $(\tau=t-mP-t_1)$:

$$\sigma(x,t)=\sigma_T+\frac{4eZ\rho}{\Omega L}\sum_{n=0}^{\infty}\cos\frac{(2n+1)\pi x}{L}e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tau}\times\left(\kappa_2\int_0^{\tau}j_2e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tilde{\tau}}d\tilde{\tau}+\phi_1+M\phi_P\right)\tag{29}$$

where,

$$\phi_1=e^{-\frac{(2n+1)^2\pi^2}{L^2}\kappa_1t_1}\kappa_1\int_0^{t_1}j_1e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_1\tilde{\tau}}d\tilde{\tau}$$

$$\phi_P=e^{-\frac{(2n+1)^2\pi^2}{L^2}(\kappa_1t_1+\kappa_2t_2)}\times\left(\phi_1+\kappa_2\int_0^{t_2}j_2e^{\frac{(2n+1)^2\pi^2}{L^2}\kappa_2\tilde{\tau}}d\tilde{\tau}\right)$$

In both cases, it has

$$t_2=P-t_1\quad M=\frac{1-e^{\frac{-(2n+1)^2\pi^2}{L^2}m(\kappa_1t_1+\kappa_2t_2)}}{1-e^{\frac{-(2n+1)^2\pi^2}{L^2}(\kappa_1t_1+\kappa_2t_2)}}$$

$$\kappa_1=\frac{D_0e^{-\frac{E_a}{k_BT_1}}B\Omega}{k_BT_1},\quad \kappa_2=\frac{D_0e^{-\frac{E_a}{k_BT_2}}B\Omega}{k_BT_2}$$

As can be seen in Fig. 14(b), this model can take care of transient effect of periodic current density and temperature.

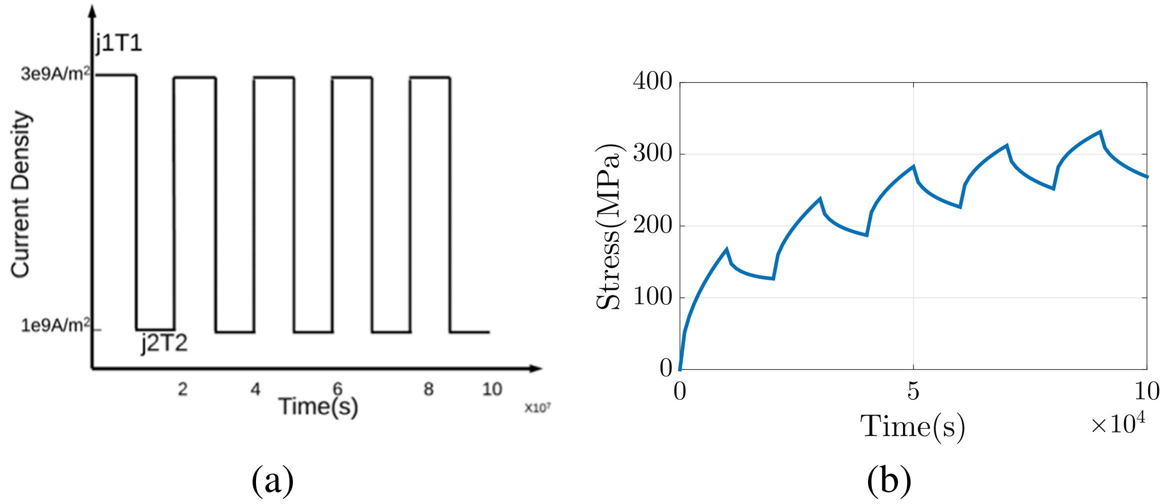

Fig. 14. (a) Periodic current and temperature (b) EM-stress distribution with periodic current and temperature.

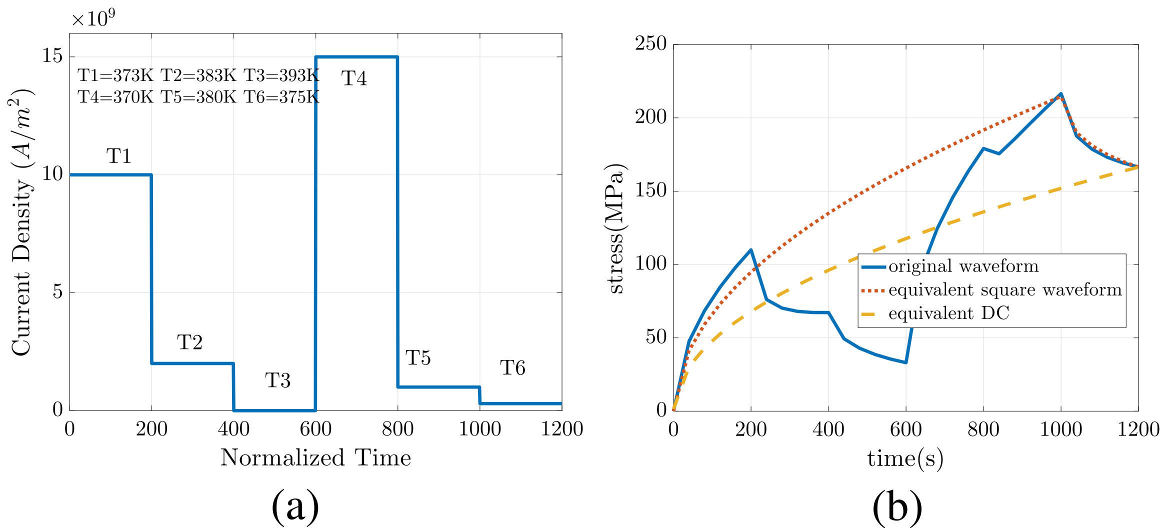

Fig. 15. (a) Original input driving current density. (b) Calculated EM DC equivalent current density with two methods.

However this model is still complicated. An empirical model using fitting method is proposed in [42]. In this work, they convert periodic current density to an equivalent DC current density. Instead, it takes average current density, the transient effect is considered in this new equivalent DC current density. Stress at the peak is used for fitting so that transient effect can be fully considered. In one period, the current density is converted to an equivalent square wave current density. Stress estimated using the new square current density has same peak value and end value as the original waveform as shown in Fig. 15. It can be seen that if peak stress and final stress at the end of period can be fitted, it is more accurate than the case only fit for final stress.

Besides, temperature, frequency and duty cycle are also used as parameters for the model building. The fitted model is

$$\begin{aligned} j_{em} = {} & 4.988*10^9 - 0.0663*10^9*X_1^2 - 1.114*10^9*X_1*X_2 \\ & - 0.9981*10^9*X_1*X_3 - 0.1390*10^9*X_1*X_4 \\ & - 0.3485*10^9*X_1*X_5 - 0.0315*10^9*X_2^2 \\ & - 0.1728*10^9*X_3^2 - 0.3461*10^9*X_3*X_4 \\ & + 0.0181*10^9*X_4^2 + 0.0934*10^9*X_5^2 \end{aligned} \quad (30)$$

where

$$X_1 = \frac{j_1 - 7.5*10^9\ (\mathrm{A/m^2})}{2.5*10^9\ (\mathrm{A/m^2})} \quad X_2 = \frac{j_2 - 1.75*10^9\ (\mathrm{A/m^2})}{2.75*10^9\ (\mathrm{A/m^2})}$$

$$X_3 = \frac{D - 70\%}{25\%} \quad X_4 = \frac{P - 5.5*10^3\ (\mathrm{s})}{4.5*10^3\ (\mathrm{s})}$$

$$X_5 = \frac{T - 380\ (\mathrm{K})}{20\ (\mathrm{K})}$$

j_1 is current density of upper phase, j_2 is current density of lower phase, P is period and D is duty cycle.

An example is shown in Fig. 16 As can be seen, the nucleation predicted by equivalent DC model is close to the real stress. The equivalent DC method is more convenient to be integrated into the CAD tools. However, with limited range of training data, this model cannot take care of all the possible current densities,temperatures, etc.

2.5. Dynamic stress evolution in multi-branch interconnects

The previously discussed EM models can only deal with a single wire. However, in practical VLSI layout, multi-segment intercon-

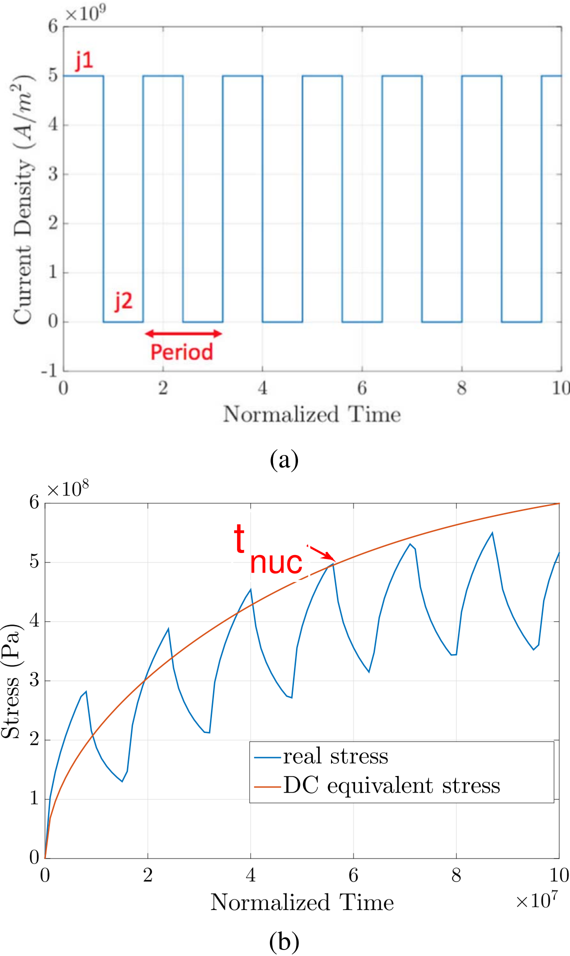

Fig. 16. (a) Original input driving current density. (b) Calculated EM DC equivalent current density with t_{nuc}.

nect tree wires are commonly used, where the metal atoms are not blocked at segment junctions as shown in Fig. 4. An interconnect tree wire is defined as continuously connected metal (copper or aluminum) within one layer of metallization. These trees terminate at diffusion barriers at vias and contacts and can have more than one terminating segment. Because of this, work has been developed that can perform analysis on multi-branch interconnects based on the solution of the Korhonen PDEs through analytical and numerical methods, giving the dynamic stress evolution of the interconnects.

2.5.1. Analytical model for multi-branch interconnects

In [43], the dynamic stress evolution is solved for several multi-branch interconnect structures. Analytical solutions are found by utilizing the Laplace Transformation method to solve the Korhonen PDEs. This work decouples each wire in the interconnect and develops the boundary conditions that govern EM flux in the wires. The paper provides demonstration of the formulation of the analytical solutions on three different structures: a single wire, straight-line three-terminal wire, T-shaped four-terminal tree, and the cross-shaped five-terminal tree.

The analytical solution to the straight-line three-terminal wire is presented as an example. The stress in each segment is written as shown in (31). From here, the Laplace transform is applied to reduce the PDE to an ODE. This ODE is then solved, the solution of which is not presented in this survey.

$$\begin{aligned}\frac{\partial\sigma_1(x,t)}{\partial t} &= \frac{\partial}{\partial x}\left[\kappa_1\left(\frac{\partial\sigma_1(x,t)}{\partial x}+G_1\right)\right], \; -L_1<x<0,\; t>0,\\ \frac{\partial\sigma_2(x,t)}{\partial t} &= \frac{\partial}{\partial x}\left[\kappa_2\left(\frac{\partial\sigma_2(x,t)}{\partial x}+G_2\right)\right], \; 0<x<L_2,\; t>0.\end{aligned} \tag{31}$$

Once a solution is found in the frequency-domain, the inverse Laplace Transform is applied to obtain the time-domain solution. This results in an analytic solution for both wire segments which are in the form of an infinite series of basis functions as shown in (32), (33)

$$\begin{aligned}\sigma_{1,I}(x,t) = &\frac{1}{2}\sum_{n=0}^{+\infty}\{2G_1g(\xi_1,t)+(G_2-G_1)g(\xi_2,t)\\ &-2G_2g(\xi_3,t)+(G_2-G_1)g(\xi_4,t)\}\\ &+\frac{1}{2}\sum_{n=0}^{+\infty}\{(G_2-G_1)g(\xi_5,t)-2G_2g(\xi_6,t)\\ &+(G_2-G_1)g(\xi_7,t)\}+2G_1g(\xi_8,t)\},\end{aligned} \tag{32}$$

$$\begin{aligned}\sigma_{2,I}(x,t) = &\frac{1}{2}\sum_{n=0}^{+\infty}\{(G_2-G_1)g(\eta_1,t)+2G_1g(\eta_2,t)\\ &+(G_2-G_1)g(\eta_3,t)-2G_2g(\eta_4,t)\}\\ &+\frac{1}{2}\sum_{n=0}^{+\infty}\{-2G_2g(\eta_5,t)+(G_2-G_1)g(\eta_6,t)\\ &+2G_1g(\eta_7,t)+(G_2-G_1)g(\eta_8,t)\}.\end{aligned} \tag{33}$$

where $g(x,t)$ is defined as

$$g(x,t) = 2\sqrt{\frac{\kappa t}{\pi}}e^{-\frac{x^2}{4\kappa t}} - x\times \mathrm{erfc}\left\{\frac{x}{2\sqrt{\kappa t}}\right\}. \tag{34}$$

and erfc(x) is the complementary error function.

Using just the first dominate term in this series shows very good agreement when compared to COMSOL finite element analysis software with less than 4% error. The same result is found for the remaining structures in the paper and solutions are also tested under a variety of current density distributions to show the effect it has on dynamic stress evolution in multi-branch interconnects.

Fig. 17 shows obtained evolution of the stress distribution along the 3-terminal interconnect tree. Analytical solution obtained with the proposed method fits well to the results of the numerical simulation at every time instance.

In addition to the structures mentioned above, [43,44] also shows the method as applied to a more complex and realistic power grid tree. In this problem, a metal 1 VDD power rail tree is segmented by many vias or voltage ports along its length. The wire is divided into segments each ending in a port or the rail end and proper boundary conditions are formulated for the tree. The Laplace transform is applied to the PDEs and results in a system of equations. Furthermore, the paper shows that this can be extended to any n-segment wire using the equations in (35).

$$\begin{aligned}\frac{\partial\sigma_1}{\partial t} &= \frac{\partial}{\partial x}\left[\kappa_1\left(\frac{\partial\sigma_1}{\partial x}+G_1\right)\right], \; 0\le x\le l_1\\ \frac{\partial\sigma_2}{\partial t} &= \frac{\partial}{\partial x}\left[\kappa_2\left(\frac{\partial\sigma_2}{\partial x}+G_2\right)\right], \; l_1\le x\le l_2,\\ &\cdots\cdots\\ \frac{\partial\sigma_{n-1}}{\partial t} &= \frac{\partial}{\partial x}\left[\kappa_{n-1}\left(\frac{\partial\sigma_{n-1}}{\partial x}+G_{n-1}\right)\right], \; l_{n-2}\le x\le l_{n-1},\\ \frac{\partial\sigma_n}{\partial t} &= \frac{\partial}{\partial x}\left[\kappa_n\left(\frac{\partial\sigma_n}{\partial x}+G_n\right)\right], \; l_{n-1}\le x\le L.\end{aligned} \tag{35}$$

Additionally, an n-segment interconnect will use the following boundary conditions in (36).

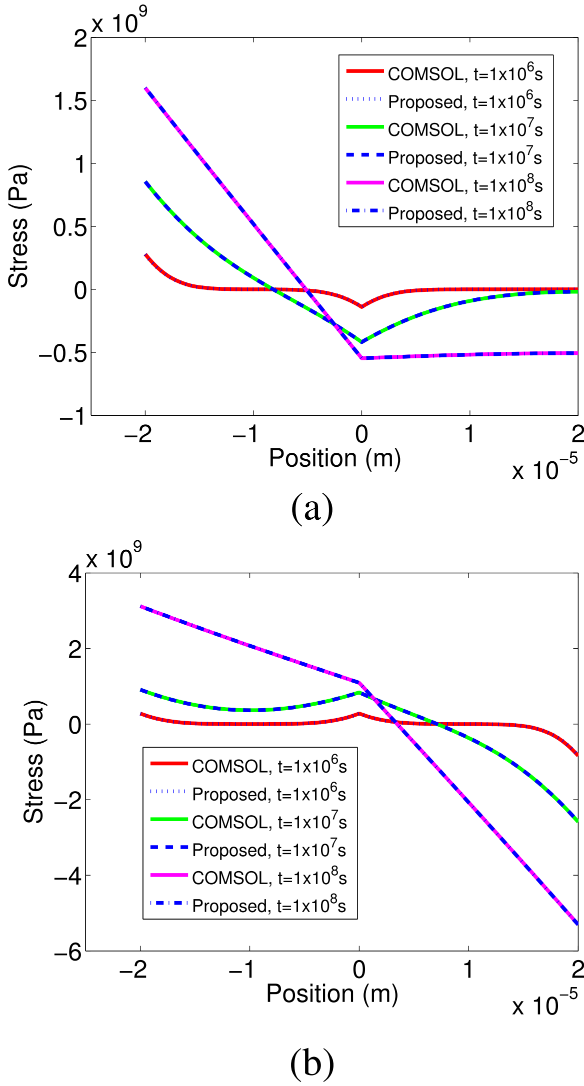

Fig. 17. The EM stress development along the lines 1 and 2 in the 3-terminal interconnect tree: (a) $j_1 = 2 \times 10^{10}$ A/m^2, $j_2 = 0$ A/m^2; (b) $j_1 = 2 \times 10^{10}$ A/m^2, $j_2 = 6 \times 10^{10}$ A/m^2.

$$
\begin{aligned}
&\kappa_1\left(\frac{\partial \sigma_1}{\partial x} + G_1\right) = 0, \ \ x = 0, \sigma_1 = \sigma_2, \ \ x = l_1,\\
&\kappa_1\left(\frac{\partial \sigma_1}{\partial x} + G_1\right) = \kappa_2\left(\frac{\partial \sigma_2}{\partial x} + G_2\right), \ \ x = l_1, \sigma_2 = \sigma_3, \ \ x = l_2,\\
&\kappa_2\left(\frac{\partial \sigma_2}{\partial x} + G_2\right) = \kappa_3\left(\frac{\partial \sigma_3}{\partial x} + G_3\right), \ \ x = l_2,\\
&\ldots\ldots\\
&\kappa_n\left(\frac{\partial \sigma_n}{\partial x} + G_n\right) = 0, \ \ x = L.
\end{aligned} \tag{36}
$$

The previously mentioned experiments and solutions were performed using equal length wire segments. However, the paper further shows that the solution method can handle variable length wires and performs analysis on the effect that length has on the stress evolution in a multi-segmented interconnect. For example, wire segments are shortened in one experiment and it is observed that this results in higher compressive stress in the shorter wire when currents in the segments flow away from the wire junctions. This shows that shorter wires in this configuration are more EM resilient than longer wires due to back-stress gradient and is shown in Fig. 18.

An extension of the work in [43] shows that an analytical solution can be found by the same technique for time-varying temperature and variable wire lengths [44]. These are important considerations for accurate EM analysis under realistic chip working conditions as temperature can vary drastically depending on workload and environmental factors. Additionally, many multi-segmented wires do not have equal segment lengths. Furthermore, analysis of the varying wire lengths shows the affect of wire topology on the dynamic stress evolution.

2.6. EM modeling for multi-segment wires by integral transformation method

Recently, another closed form analytical solution was developed for straight multi-segment wires as shown in Fig. 19 using the so-called Integral transformation method, which essentially the Green's function based method [45]. The method can compute the stress evolution over time for that kind of wires. Korhonen's Eq. (14) is discretized using this method and stress can be expressed as:

$$\sigma(x, t) = \sum_{m=1}^{\infty} \frac{\psi_m(x)}{N(\lambda_m)} \overline{\sigma}(\lambda_m, t) \tag{37}$$

where the norm of eigenfunctions $N(\lambda_m)$ is

$$N(\lambda_m) = \int_{\chi=0}^{L} [\psi_m(\chi)]^2 d\chi \tag{38}$$

and $\overline{\sigma}(\lambda_m, t)$ is transformed solution of stress which is

$$\overline{\sigma}(\lambda_m, t) = \overline{F}(\lambda_m) e^{-\kappa\lambda_m^2 t} + \frac{1}{\lambda_m^2}(1 - e^{\kappa\lambda_m^2 t}) \cdot \sum_{k=1}^{n} \Gamma_k \cdot \left(cos\frac{x_{k-1}}{L}m\pi - \cos\frac{x_k}{L}m\pi \right) \tag{39}$$

where F is

$$\overline{F}(\lambda_m) = \int_{\chi=0}^{L} \psi_m(\chi) \cdot \sigma_0(\chi) d\chi \tag{40}$$

λ_m and $\psi(x)$ are eigenvalues and eigenfunctions which are the solutions of the Sturm-Liouville problem corresponding to the diffusion Eq. (14) and the boundary conditions

$$\lambda_m = \frac{m\pi}{L}, \ \ \psi_m(x) = \cos\frac{x}{L}m\pi \tag{41}$$

where $m = 1, 2, \ldots, \infty$. Γ_k is

$$\Gamma_k = \frac{eZ\rho}{\Omega} j_k, \ k = 0, 1, \ldots, n \tag{42}$$

With (37), when the stress $\sigma(x, t)$ equals to the given critical stress σ_{crit}, then the nucleation time t_{nuc} is obtained. This method is efficient and overcomes the difficulty for numerical solution of partial differential equations. The t_{nuc} estimated using this method is very close to original Korhonen's equation. An example is shown in Fig. 20. As can be seen, the stress can be calculated correctly for multi-branch wires.

This work uses the integral transformation method to develop a closed form expression of Korhonen's equation for EM analysis. Different current densities on multi- branches can be considered and stress analyzed with this method is very accurate. However, this method is limited to one dimensional wires and cannot handle two dimensional structures such as the T-shape or cross-shape.

2.7. EM steady-state modeling and immortality check for multi-segment wires

Since traditional Black's equation and Blech product cannot handle multi-segment structure and transient EM models requires complex computation, a novel and fast EM immortality check for general multi-segment interconnect wires is proposed in [46]. This method use voltage instead of current density as the key parameter and stress on

Fig. 18. The EM stress development along the segments 1 and 2 in the three-terminal interconnect tree: (a) $L_2 = \frac{1}{6}L_1$; (b) $L_2 = \frac{2}{6}L_1$; (c) $L_2 = \frac{3}{6}L_1$; (d) $L_2 = \frac{4}{6}L_1$.

Fig. 19. Example of a multi-segment wire.

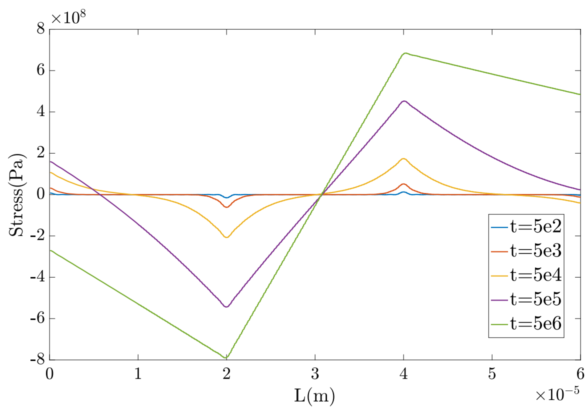

Fig. 20. Stress distribution over time on multi-segment wire calculated by integral transformation method.

the cathode at steady state (σ_{steady}) are compared with critical stress (σ_{crit}). If σ_{steady} is lower than σ_{crit}, the wire is considered as immortal.

In that model, an *EM voltage* (V_E) which is proportional to stress at ground node (σ_g) is calculated

$$V_E = \frac{1}{2A} \sum_{k \neq g} a_k V_k \tag{43}$$

where V_k is the normal nodal voltage (with respect to cathode node g) at node k of the wire. a_k is the total area of branches connected to node k. With voltage of node i (V_i), steady-state stress at that node (σ_i) can be calculated as $\sigma_i = \beta(V_E - V_i)$, where $\beta = \frac{eZ}{\Omega}$, A critical EM voltage $V_{crit,EM}$, which is voltage required for the nucleation to happen, is defined by

$$V_{crit,EM} = \frac{1}{\beta}(\sigma_{crit} - \sigma_{init}) \tag{44}$$

σ_{init} is the initial stress. In order to check whether the interconnect wire is immortality or not, we need to check the following condition:

Fig. 21. Interconnect example for EM analysis for straight 3-terminal wire.

$$V_{crit,EM} > V_E - V_i \tag{45}$$

If this condition meets for all the nodal, EM failures will not happen. Since generally cathode node has the lowest voltage among all nodes in the interconnect wire, we can just check cathode node on the interconnect tree instead of all the nodes, which means

$$V_{crit,EM} > V_E - V_{cat} \tag{46}$$

where V_{cat} is voltage at cathode. Note that (46) can be applied to both power and ground networks.

We illustrate this method by an example. Fig. 21 shows a 3-terminal wire. In this wire, node 0 is treated as the ground node. Current densities in two segments are j_a and j_b and may not the same because they will be determined by the rest of the circuit. Then, the EM stress equation becomes:

$$V_0 = 0, \quad A_0 = l_a w_a, \quad \sigma_0 = \beta V_E$$
$$V_1 = j_a l_a \rho, \quad A_1 = l_a w_a + l_b w_b, \quad \sigma_1 = \beta(V_E - V_1)$$
$$V_2 = j_b l_b \rho + j_a l_a \rho, \quad A_2 = l_b w_b, \quad \sigma_2 = \beta(V_E - V_2)$$
$$A = A_0 + A_1 + A_2$$

where

$$V_E = \frac{V_0 A_0 + V_1 A_1 + V_2 A_2}{2A} = \frac{V_1 A_1 + V_2 A_2}{2A}$$

Then we can compare V_E and V_{crit} to see if this wire is immortal.

The presented method, called *VBEM* method, provides an efficient method of checking for EM mortality in multi-segment wires. In contrast to the classical methods, consideration of multi-segmented wires provides a more complete picture of the effect that EM has on a wire as stress in neighboring wires can affect its stead-state stress. Furthermore, this closed form solution does not require the transient solution to complicated PDEs which makes it very efficient for EM mortality checking.

2.8. Finite difference analysis for EM stress evolution

Solving for the dynamic stress evolution in a general interconnect tree requires the solution of PDEs which can be difficult for complex multi-branched structures. While analytical methods can be applied to specific structures, as shown in Section 2.5, this is very difficult for large complex structures. As a solution, numerical methods are ideal for solving the PDE's for these types of problems as they can handle complex and arbitrary geometries.

The Finite Difference Method (FDM) has been proposed for solving the dynamic stress evolution PDEs for EM analysis in general interconnect trees [47]. The FDM method is ideal, and best suited, for solving this problem due to the very regular structure of the interconnect trees. While Finite Element Analysis (FEA) is also a viable method, the regularity of the structures means that the primary advantage of FEA, the ability to form a mesh for complicated and irregular domains, is lost. However, the simple grid formulated by FDM is well suited for the rectangular structures found in interconnect trees, ie, the straight-line rectangular interconnects are amenable to FDM grid formulation. Furthermore, the implementation of FDM, compared to other numerical methods, is relatively simple.

FDM is a numerical method that discretizes a problem by applying the local Taylor expansion to a PDE at grid points existing within the domain. In this case, the dynamic stress PDE and boundary condition shown in (47) are discretized for the nucleation phase.

$$PDE: \frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma}{\partial x} + G_x\right)\right]$$
$$BC: \frac{\partial \sigma}{\partial x}(x, t) = G_x, \ x = 0, L \text{ at } 0 < t < t_{nuc}$$
$$IC: \sigma(0) = [\sigma_1(0), \sigma_2(0), \ldots, \sigma_n(0)] \ at \ t = 0 \tag{47}$$

Here, $\kappa = D_a B\Omega/k_B T$ and $G = \frac{eZ\rho j}{\Omega}$, which is a function of current density j. For the Growth phase, the boundary condition shown in (48) is applied to the boundary where the void has nucleated.

$$\frac{\partial \sigma}{\partial x}(x_{nuc}, t) = \frac{\sigma(x_{nuc}, t)}{\delta}, \text{ at } t_{nuc} < t < \infty \tag{48}$$

In Eq. (48), x_{nuc} is the location of the void nucleation at a boundary and δ is size of the void interface. Once discretized, the equations form a system of equations that can be solved using backward substitution. In [47], an implicit FDM is used which employs spatial and temporal discretization, shown in (49), which yields a system of linear equations $A\sigma^{n+1} = \sigma^n$ where A is a coefficient band-matrix, σ^{n+1} is the unknown stress to be solved for, and σ^n is the currently known stress. Additionally, boundary conditions are discretized separately to handle ghost points that exist outside of the spatial domain, shown in (50). Each n timestep is then solved iteratively using the previous timestep's solution. This implicit scheme has the advantage of maintaining numerical stability with large spatial and temporal time steps but with added computational complexity compared to an explicit method which can be solved directly but with conditional stability. The system is solved for each timestep with the solution vector being used in each subsequent timestep.

$$\frac{\sigma_i^{n+1} - \sigma_i^n}{\Delta t} = \kappa \frac{\sigma_{i+1}^{n+1} - 2\sigma_i^{n+1} + \sigma_{i-1}^{n+1}}{\Delta x^2} \tag{49}$$

$$\sigma_x(0, t) = \frac{\partial \sigma_i^n}{\partial x} = \frac{\sigma_i^{n+1} - \sigma_{i-1}^{n+1}}{\Delta x} = G \tag{50}$$

Additionally, the discretization of the boundary condition for void growth is also presented in (51).

$$\sigma_x(0, t) = \frac{\partial \sigma_i^n}{\partial x} = \frac{\sigma_i^{n+1} - \sigma_{i-1}^{n+1}}{\Delta x} = \frac{\sigma_i^n}{\delta} \tag{51}$$

This boundary condition is applied, during the growth phase, to the terminal in which a void has nucleated.

In this work, the PDE for the nucleation phase is discretized and the dynamic stress evolution is obtained until steady state is reached. This will indicate if the structure is EM immortal by checking to see if stress at any boundary or junction surpasses a critical stress value that would result in void nucleation. If a critical stress is reached, the state of stress in the interconnect tree at the time of void nucleation is then saved and used as the initial condition for the growth phase. The growth phase, which uses the same PDE but uses the boundary condition in (51) at the point of void nucleation, is then solved for using the same method. The paper demonstrates the discretization and solution for a single wire and a two-segment wire. Experiments are performed using various stressing conditions. The results are then compared to COMSOL FEA software considered the gold standard in numerical solutions. Results show that the FDM used is accurate for both the void nucleation and the void growth phases when compared to the COMSOL solution. The results for the 2-segment wire void nucleation and growth phases are presented in Fig. 22.

While it can be argued that the analytical solutions should be much quicker in terms of solution time, the numerical method used in [47] presets a more general solution method that can be expanded to handle much more complex structures without the need to create a new analytical solution for every new structure while also maintaining good accuracy compared to COMSOL FEA solver. Only discretization and matrix formulation needs to be done for each new structure, which can be automated. Furthermore, the FDM is amenable to model reduction, as shown in [48], which can mitigate the performance deficiency compared to analytical solutions.

2.9. System-level dynamic reliability management and optimization

This section presents system-level dynamic reliability management (DRM) and optimization. Traditional approaches for addressing the

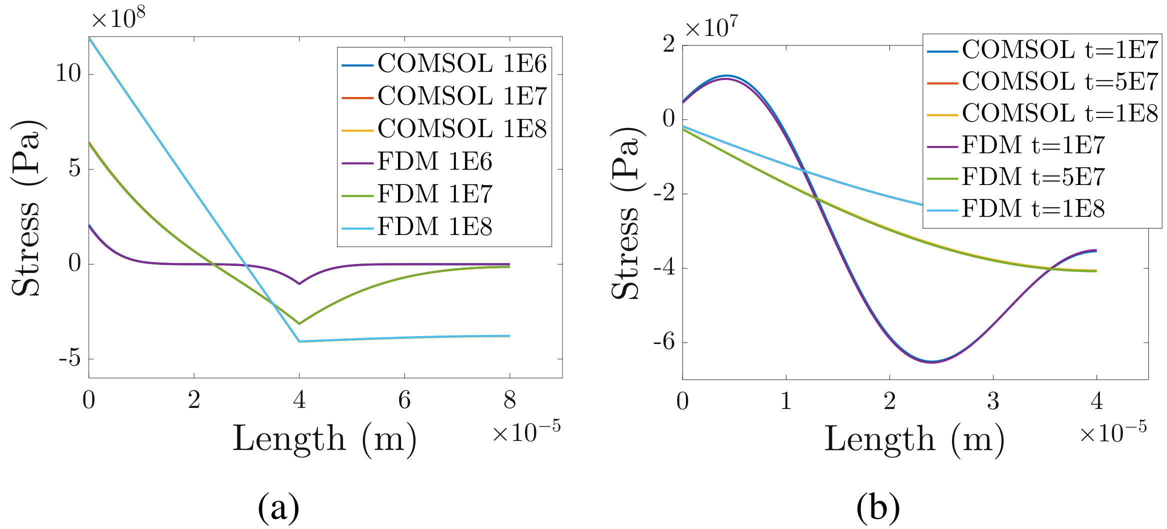

Fig. 22. 2-wire passive sink case ($j1 = 10^{10}$ A/m^2 $j2 = 0$) for (a) void nucleation and (b) void growth.

long-term reliability mainly focus on manufacture processes and circuit level techniques, those existing technologies for ensuring reliability will not be able to satisfy the competing requirements for computing and communication platforms as they typically operate in one layer due to lack of holistic modeling and analysis capability and cross-layer EDA reliability-aware design tools. This potentially leads to inefficiencies that will make these techniques impractical in future fabrication processes. This section focuses on developing system-level runtime techniques for reliability management and mitigation subject to performances, power, energy and lifetime constraints. The recently proposed two DRM techniques for different computing systems will be introduced in this section. First, a DRM technique for emerging dark silicon manycore processors will be introduced [49,50]. Second, a new approach for cross-layer electromigration (EM) induced reliability modeling and optimization at physics, system and datacenter levels will be been presented [51].

2.9.1. System-level EM-induced reliability model on multi/manycore system

An existing EM model, including the new physics-based model, can only take a constant temperature. The previous study shows that whole system time-to-failure (TTF) or lifetime under different temperature can be approximated by [52]:

$$lifetime_{i,state} = \frac{1}{\left(\sum_{k=1}^{n}\left(\Delta t_{i,k}\frac{1}{TTF_{i,k}}\right)\right)/T} \tag{52}$$

where $TTF_{i,k}$ is the actual MTTF under the k-th power and temperature settings for Δt_k period, assuming each core works through n different power and temperature settings and $T = \sum_{k=1}^{n} \Delta t_{i,k}\cdot a_{i,k}$ is core selection variable, which is zero when i-th core is dimmed at the k-th execution cycle time as dark silicon is enabled. Each $MTTF_{i,k}$ will be computed based on the recently proposed physics-based EM model and assessment techniques [22]. To explain a system-level reliability on a manycore processor, we use chip lifetime as the shortest lifetime among the cores [53,54]. Recently, one study used *performability* as the ratio of a number of non-failure cores over total number of cores [55] to explain chip multiprocessor (CMP).

2.9.2. Energy and lifetime optimizations for dark silicon manycore microprocessor considering EM effect

For new dark silicon system, a new dynamic reliability management (DRM) technique for emerging dark silicon manycore processors have been proposed [49,50]. Recently, architecture researchers predicted

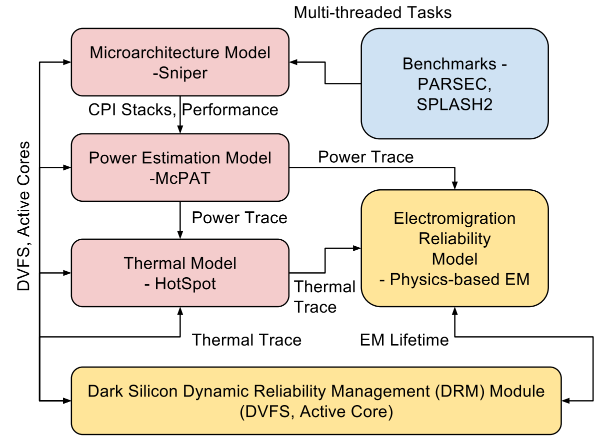

Fig. 23. The evaluation platform for dark silicon and DRM algorithms.

that future many-core (100–1000 cores) silicon dies can only be powered up partially (so-called dark silicon) as power constraints will not allow all the cores to be active at the same time. Such manycore systems pose new challenges and opportunities for power/thermal and reliability management of those chips [56].

The new approach is based on a newly proposed physics-based electromigration (EM) reliability model to predict the EM reliability of full-chip power grid networks [22,36]. The DRM problem as maximizing the (EM-induced) lifetime of dark silicon manycore processors by controlling the number of active cores and the suitable performance state (p-state) was formalized with subject to the performance and temperature constraints with dark silicon simulation framework in Fig. 23. To find maximizing lifetime/minimizing energy policy in dark silicon systems, this uses Q-learning, one of the reinforcement learning methods.

In our problem, the state (s) consists of the configurations of dynamic voltage frequency scaling (DVFS) and active core status (on/off) for each core. DVFS uses performance state (p-state) which can represent operating voltage and frequency. Action (a) is defined as a state transition from one state to the another state. Transiting an action in a state makes the agent with a reward (negative penalty) scoring that is calculated with the quantity of state-action combination (Q). Q can be defined as a set of states (S) and a set of action (A) table, $S \times A$, which is Q-table. Q-table can be updated by a Q-value function which a long-term penalty function with state and action.

Fig. 24 shows proposed Q-learning based reliability optimization framework. The environment part is dark silicon manycore processor,

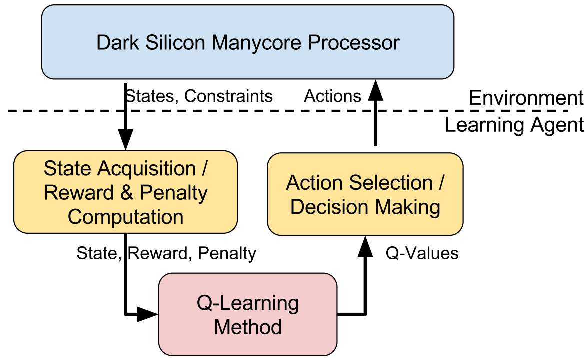

Fig. 24. Q-Learning model with reliability-aware dark silicon framework.

another is learning agent, which is Q-learning algorithm. The learning agent can obtain the environmental state, calculate penalty function, and finally, decide the next action.

A large class of multithreaded applications is used as the benchmark to validate and compare the proposed dynamic reliability management methods. Experimental results on a 64-core dark silicon chip show that the proposed DRM algorithm can effectively reduce the energy consumption of a dark silicon manycore system when the system is not tightly constrained. Fig. 25, the proposed method finds relatively high energy savings (37.5% and 18.1%) with large performance deadline (64.1 ms) than the global dynamic voltage frequency scaling (DVFS) method and core status because the more cores can be in low power mode or turned off (dark silicon) with the given power budget and performance deadline. In small performance deadline (42.7 ms), there is still a chance to highly save energy (37.5%) than global DVFS in the smaller lifetime constraint (10 yrs). However, for the higher lifetime and smaller performance constraints, energy saving will be close to global DVFS method as shown in

2.9.3. Cross-layer modeling and optimization for EM Induced reliability

For datacenter system, a new approach for cross-layer electromigration (EM) induced reliability modeling and optimization at physics, system and datacenter levels has been proposed [51]. The new approach is based on a newly proposed physics-based electromigration (EM) reliability model to predict the EM reliability of full-chip power grid networks [22,36]. This works show an example that how the new physics-based dynamic EM model at the physics level can be abstracted at the system level and even at the datacenter level. The datacenter system-level power model is based on the BigHouse simulator [57].

To speed up the online optimization for energy in a datacenter, a new combined datacenter power and reliability compact model has been proposed with using a learning based approach in which a feed-forward neural network (FNN) is trained to predict energy and long term reliability for each processor under datacenter scheduling and workloads. As shown in Fig. 26, the feed-forward neural network (FNN) can be constructed to predict energy and long-term reliability for each processor under datacenter scheduling and workloads. We separately construct and train networks for each individual workloads. The inputs to the neural networks are average load rate, power mode (quantified), and number of servers in the datacenter. With these inputs, the neural networks can estimate average cluster power, average processor temperature, tail latency, and average socket MTTF. To train the neural networks more efficiently with less numerical stability issues, the scaling of the inputs is required. Otherwise, it can have a large effect on the quality of final solution. As shown in Fig. 26, the number of servers is normalized. The average load rate can be used without scaling since it already has a good distribution. In the same way, the output data set can be scaled and converted into logarithmic scale since they are served as a part of the training input set in the back-propagation algorithm [58]. We use three hidden layers with sigmoid activation functions, with all layers having 15 nodes respectively. The input and output layer sizes are 3 and 5 respectively.

To optimize the energy and reliability of a datacenter, we apply the efficient adaptive Q-learning based reinforcement learning method. Fig. 27 shows cross-layer framework for datacenter system. Experimental results show that the proposed compact models for the datacenter system trained with different workloads under different cluster power modes and scheduling policies are able to build accurate energy and lifetime as seen in Table 2. Moreover, the proposed optimization method effectively manages and optimizes datacenter energy subject to reliability, given power budget and performance.

As shown in Table 3, energy savings for the different constraints (case 1, 2 and 3) have been evaluated. WWW workload with tight MTTF constraints (case 1) and loose MTTF constraints (case 3). In Table 3, our method finds relatively high energy savings for each case.

3. Aging effects from the physical to system level

The International Technology Roadmap for Semiconductors (ITRS) states that upcoming technology nodes introduce reliability challenges at an increased pace compared to the last decade [59] because devices below 45 nm are increasingly susceptible to multiple aging mechanisms. This is primarily due to the higher vertical/horizontal electric fields within scaled MOSFETs along with the employment of the new high-K material in forming the transistor's dielectric. In fact, shrinking feature sizes leads to higher electric field strengths, as well as higher current densities, which both accelerate device aging and thus increase degradation of transistor electrical characteristics which can ultimately turn into failures. Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI) and Hot Carrier Induced Degradation (HCID) have become the most prominent aging mechanisms impeding reliable MOSFET transistors. While understanding the physical processes of aging mechanisms is not entirely

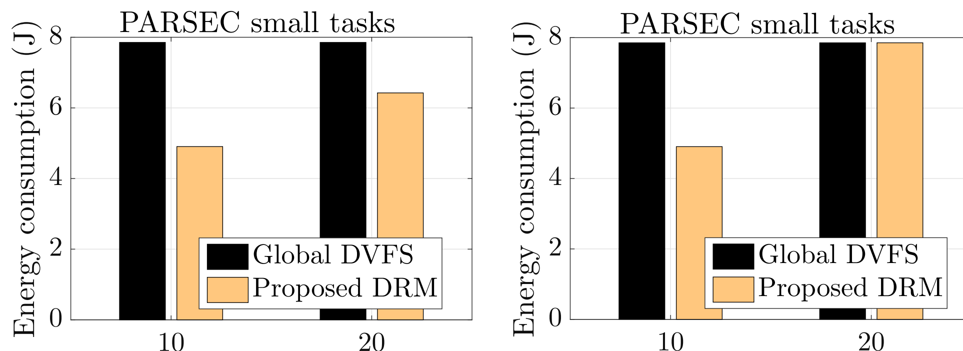

Fig. 25. Energy optimization with global DVFS (all cores are in the same p-state) and our proposed DRM on PARSEC small task set – different performance deadline and EM lifetime constraints).

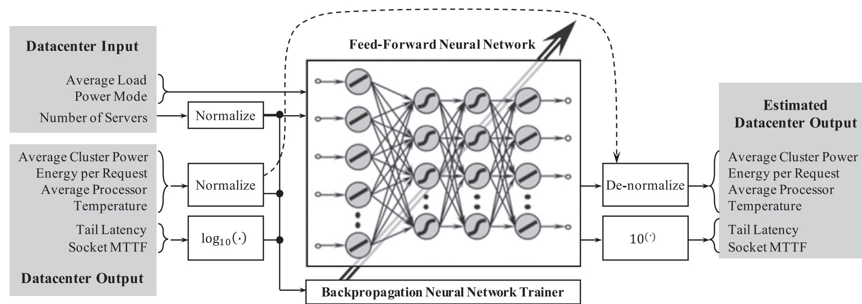

Fig. 26. Feed-forward neural network structure and data configuration.

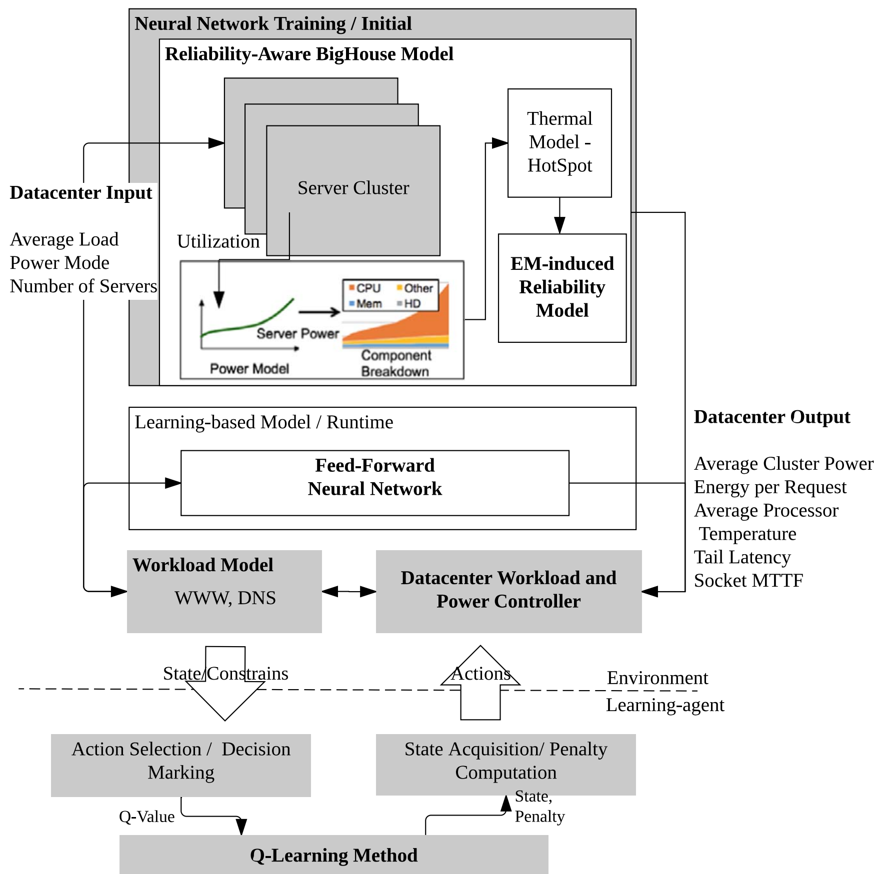

Fig. 27. The evaluation platform for datacenter and energy and reliability management algorithms.

Table 2
Accuracy analysis (RMSE) of the feed-forward neural network (FNN) model for WWW service in datacenter systems.

	Training error	Validation error
Tail latency	6.53%	9.37%
Avg. cluster power	2.45%	3.50%
Avg. proc. temp.	2.91%	2.92%
Avg. proc. MTTF	6.78%	7.40%
Energy per request	0.738%	1.20%

required at the system level, there is still a substantial need to model the different induced degradations by aging (originated at the physical level) towards grasping and investigating how they propagate all the way up to the system level where their deleterious effects finally take place.

Download software: Our developed aging models, degradation-aware cell libraries, reliability framework, etc. are publicly available at [60]. They are ready to be directly used with existing EDA tool flows like Synopsys without requiring any modifications.

3.1. Aging effects at the physical and device levels

BTI is mainly caused by continuous trap generation in the Si-SiO_2 interface of a transistor, whereas HCID is caused by *hot carriers*. Note that *Hot* does not relate to transistor's temperature but to the ability of carriers to tunnel through the semiconductor material. Such *hot* carriers are caused by the strong electric field across the transistor's channel causing kinetic energies sufficient to form electron-hole pairs through impact of ionization, which may be injected in undesirable areas.

In the following, we consider a PMOS transistor as an example for the sake of explication. However, defects in NMOS transistors are analogously induced but with the corresponding opposite charges.

Interface traps: These are caused by dissociating the Si–H bonds in the Si-SiO_2 interface due to the non-epitaxial structure of amorphous SiO_2 on the crystalline silicon. Further details can be found in [61].

Table 3
Energy optimization for datacenter.

	Energy per request (J)	Energy savings (%)
Max State (WWW)	23.71	
Case 1 (WWW)	8.44	64.37
Case 2 (WWW)	8.44	64.37
Case 3 (WWW)	12.25	49.30

When an electric field between gate and source is applied, holes can be captured by an Si–H bond and combined with one of the two available electrons there resulting in weakening the bond. This can activate the hydrogen to break the bond and diffuses away. Overall, the rates of dissociation/healing Si–H bonds and diffusion of molecular hydrogen mainly determine the total number of unsatisfied silicon atoms (i.e. interface traps N_{IT}) over time. BTI is responsible for one physical Si-H dissociation mechanism. Additionally, the Si–H bonds can also be dissociated because of accelerated carriers in the MOSFET channel when an electric field between the drain and source is applied. The *hot carriers* lose their energy due to Coulomb scattering leading to dissociating Si–H bonds. Therefore, HCID is responsible for the additional *interface trap* defects.

Self-healing and recovery of Si–H bonds: Healing the dissociated Si–H bonds is the opposite process to its dissociating. Actually, the dissociated bonds may almost be recovered if a sufficient relaxation time is given. However, a full recovery is impossible because the H_2 may leave the gate dielectric after reaching the metal gate. In such a case, the corresponding dissociated Si–H bond may not be healed anymore as it will lack for a bonding atomic H. Generally, the majority of dissociated Si–H bonds (i.e. due to BTI and/or HCID phenomenon) may immediately after heal because its H partners are still available beside the unsatisfied silicon atoms Si^+. It is noteworthy that the ratio between bond dissociating and bond healing, (i.e. $\frac{k_f}{k_r}$), ultimately determines the generation of N_{IT}. Further details about the aforementioned processes of dissociating and healing Si–H bonds are explained in [61].

Impact of interface traps on the MOSFET characteristics:

1. *Threshold voltage increase*: Since the *interface traps* are, at the end, unsatisfied silicon atoms Si^+, they, indeed, lead to undesired positive charges that may be accumulated under the SiO_2-Si interface. The latter results in less and less attracted carries during the formulation of the conducting channel of MOSFET because of the weakener electric field. This, in turn, manifests itself as a shift in the MOSFET threshold voltage (V_{th}) because the required voltage, to make the transistor "ON", becomes higher in order to provide the same electric field that was originally (i.e. before the generation of aging-induced defects) necessary to form the MOSFET channel.
2. *Carrier mobility degradation*: Additionally, the accumulated aging-induced charges at the SiO_2-Si interface also result in a reduction in the carrier mobility (μ) across the MOSFET channel. This is because that the channel is formed from holes and therefore the positive induced defects/charges and the holes within the channel will scatter each other. This makes the channel has more scattering making the carriers within the channel be obstructed during their movement. Note that this is valid for the case of PMOS transistors which we employ as an example during our explanation of the *interface traps* generation. However, for NMOS transistors, the channel consists of electrons, instead of holes, and defects will be analogously induced but with the corresponding opposite charges.
3. *Sub-threshold degradation*: Analogous to μ, interface traps (N_{IT}) contributes to sub-threshold (*SS*) degradation. Note that PBTI and other NBTI defects (e.g, hole traps) have a negligible contribution to *SS* degradation. This is because traps, which are not close to the interface (as in hole trapping component for NBTI and traps generation in PBTI), are inside the interfacial layer (IL)/High-k (HK) bulk and therefore they have a negligible contribution to *SS* degradation. Hence, only the N_{IT} related fraction of the total ΔV_{th} must be modeled for *SS* degradation. In practice, N_{IT} are donor type traps at the Si/IL interface which are positively charged when empty of electrons (or filled with holes) and neutral when filled with electrons. This nature of the traps being filled or emptied in response to the gate voltage gives rise to an interface trap capacitance (C_{IT}) which comes in parallel with the depletion capacitance and hence it contributes to *SS* degradation. Further discussion and details can be found in [62].
4. *Drain current degradation*: Finally, both degradations in V_{th} and μ lead to other degradations in the MOSFET electrical characteristics such as the drain current (I_D) and transconductance (g_m due to the interdependencies of them. As a matter of fact, the formation of the channel of a MOSFET transistor beneath the gate dielectric entirely depends on both V_{th} and μ. Thus, higher aging-induced degradations in both of them due to elevated temperatures result in degrading the transistor's drain current I_D as well, which is considered the key electrical characteristic in MOSFETs. This can be also observed from the following simplified equation that approximately models the drain current I_D in MOSFET [63]:

$$I_D = \mu \cdot \frac{C_{ox} \cdot W}{2 \cdot L}(V_{GS} - V_{th})^2 \cdot (1 + \Phi V_{ds}) \tag{53}$$

Where, W is the gate width, L is the gate length, C_{ox} is the gate oxide capacitance per unit area and Φ is the channel-length modulation parameter. Furthermore, according to the previous equation, the MOSFET g_m, which represents how easy the drain current to flow, can be expressed (during the saturation mode of MOSFET) as follows [63]:

$$\begin{aligned} g_m &= \frac{2I_D}{V_{gs} - V_{th}} \\ &= \mu \cdot C_{ox} \cdot \frac{W}{L}(V_{gs} - V_{th}) \cdot (1 + \Phi V_{ds}) \end{aligned} \tag{54}$$

Oxide traps: These are partially because of *Pre-Existing* defects in the amorphous SiO_2 of the gate dielectric material during manufacturing. Such defects are unsatisfied bonds due to oxide vacancies, which are not electrically active due to their neutral atoms. However, these act as N_{HT} and, thus, are positively charged if a hole is trapped. Due their spatial absence from the channel, they do not affect the transistor carrier mobility like *interface traps*. Importantly, the number of hole traps is limited to the number of the unsatisfied bonds (from manufacturing) contrary to *interface traps* which are continuously generated over time due to abundance of the Si–H bonds that can be

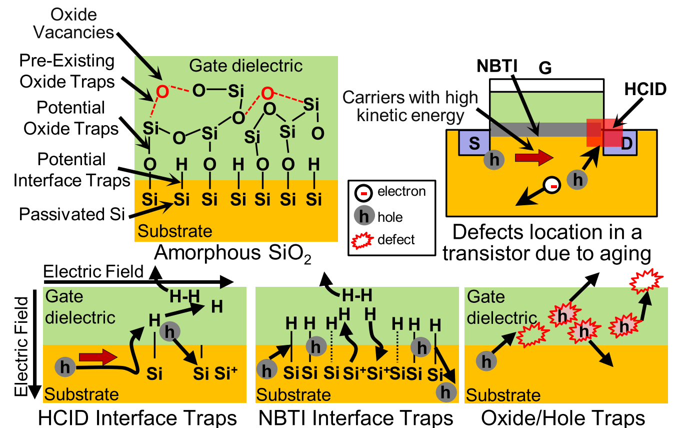

Fig. 28. Key aging defects in a PMOS transistor.

dissociated. Beside the *Pre-Existing oxide traps*, other N_{OT} can also be induced over time due to the slow and irreversible dissociation of Si–H bonds [64] which are stronger than Si–H bonds. This increases the number of available *oxide traps* resulting in increasing the saturation point of hole traps within the transistor. Despite the experimental measurements observing *oxide traps* when HCID is analyzed, it has been proven that these traps are only induced by BTI which simultaneously occurs [65]. The defects caused by NBTI and HCID are shown in Fig. 28.

Impact of oxide traps on the MOSFET characteristics: Activated *oxide traps* also result in undesired positive charges within the gate dielectric. Importantly, these charges, contrary to the *interface traps*, are not accumulated near to the SiO_2-Si interface but, instead, deep within the gate dielectric. Therefore, the deleterious impact of *oxide traps* on the transistor mobility is neglected because they cannot interact with the carriers within the MOSFET channel, unlike *interface traps*. However, *oxide traps* still can weaken the electric field over the gate dielectric due to their positive charges. This again manifests itself as an increase in the MOSFET threshold voltage (V_{th}).

It is worthy to note that as more *oxide traps* are generated over time the probability to have a conducting path between the two sides of the gate dielectric becomes higher. This results in a gate-leakage current which may burn the transistor up if it is sufficiently high due to breaking the gate dielectric down. In such a case, we say that the TDDB phenomenon has occurred. However, with the employment of the high-k material *oxide traps* are barely generated. The latter along with the increase in the thickness of the dielectric (compared to the technology before the high-K material) makes having the deleterious impact of TDDB is seldom. The probability of to have a breakdown due to TDDB in the current technology node of 22 nm is smaller than 10^{-11} [66]. Thus, the TDDB phenomenon is not within the focus of this thesis.

Interdependencies between BTI and HCID phenomena: As earlier mentioned, the BTI phenomenon consists of two kinds of traps, i.e. *interface traps* and *oxide traps*. In practice, the first kind (i.e. *interface traps*) is shared with the HCID phenomenon. This creates interdependencies between both phenomena [67,68] as Fig. 29 demonstrates.

3.2. Aging effects at the gate and circuits levels

To translate the resulting degradation due to aging in terms of threshold voltage, carrier mobility and sub-threshold slope (i.e. ΔV_{th}, μ and SS, respectively) towards the corresponding delay increase in logic gates (i.e. combinational and sequential gates), we characterize the open-source 45 nm cell library from "NanGate" [69]. To achieve that, we employ HSPICE simulations to measure the new delay and leakage/dynamic power information for every cell/gate within the cell library under aging-induced degradations. In our work, we target during simulations varied (7 × 7) input signal slew and output load capacitance cases, which is analogous to the majority of existing standard cell libraries. Then, we store all gates/cells information using the "liberty" standard format which makes our so-called "*degradation-aware*" cell library is compatible with existing EDA commercial tool flows like Synopsys. In other words, we can use it directly within standard flow tools like logic synthesis, static timing analysis (STA), power analysis, etc. without requiring any modifications. This enables designers to perform *degradation-aware logic synthesis*, *degradation-aware* timing analysis and *degradation-aware power analysis* for their designs and circuits regardless their complexity [70,62]. This is because designers will be able to employ the available mature algorithms within commercial tool flows, evolved in more than two decades, in order to perform the required analysis.

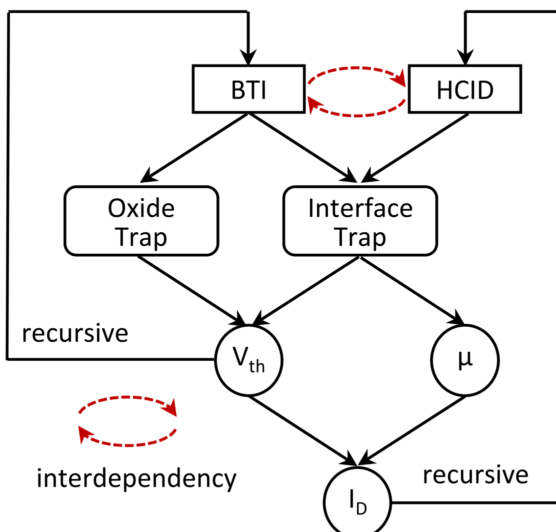

Fig. 29. The shared interface traps between BTI and HCID creates an interdependencies between both phenomena over time [67,68].

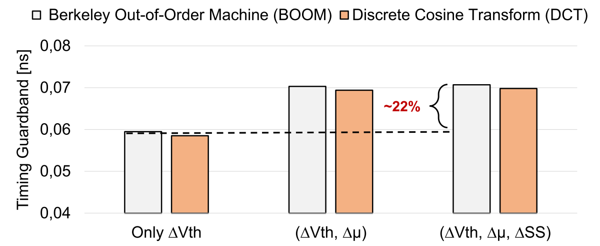

Fig. 30. Impact of BTI effects on circuits' delay. Note that considering the impact of BTI on ΔV_{th} solely is insufficient. Considering the impact of BTI on μ beside V_{th} demonstrates the need for a 22% larger guardband. Hence, ΔV_{th} alone provides a guardband that is unable to sustain reliability during lifetime.

Degradation-aware delay and power analysis: In this work, we studied the Berkeley Out-of-Order Machine (BOOM) [71] which is an open-source industry-competitive superscalar processor recently designed to serve for future microarchitectural studies for use in research and industry. In addition, we also study the Discrete cosine transform (DCT) circuit, which is typically used for image encoding [70]. By studying the BOOM and DCT designs, we show the impact of aging on the delay and power in two different circuits that have very size.

In Fig. 30, we demonstrate the total delay increase due to aging under different degradation effects. As it can be noticed, considering only ΔV_{th} as typically done in state of the art (e.g., [72]) is not sufficient and it leads to estimating a wrong timing guardband. In practice, such a wrongly-estimated guardband will be insufficient and hence reliability would not be sustained later during the projected lifetime (which is 10 in this analysis). Note that this is mainly due to neglecting the impact of aging on carrier mobility (μ) as the latter plays a major role in the I_{ON} of transistor and hence in the delay of gates/cells.

In Fig. 31, we additionally demonstrate the impact of aging on the total static power consumption of the BOOM processor. As it can be

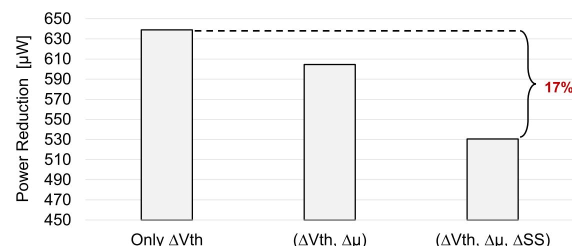

Fig. 31. Impact of BTI effects on the static power of the BOOM processor. Note that considering the impact of BTI on ΔV_{th} solely is insufficient. Considering the impact of BTI on μ and SS beside V_{th} demonstrates how the power reduction will be diminished by 17%.

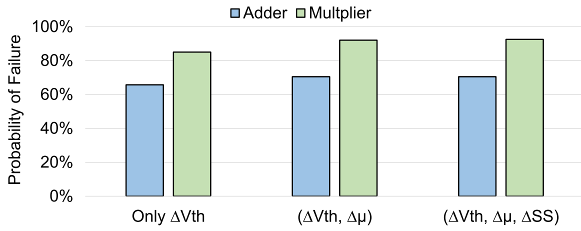

Fig. 32. The impact of aging-induced degradation of the correctness of 32 × 32 Adder and Multiplier circuits under different scenarios showing how considering ΔV_{th} alone is insufficient to estimate the correct probability of failure.

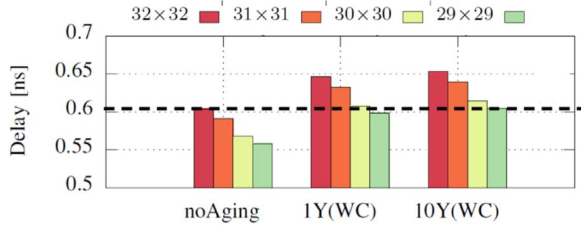

Fig. 33. Converting the required guardband into a precision reduction for the case of 32 × 32 Multiplier circuit [75]. WC refers to estimating aging-induced degradation under the worst case of aging stress. 1Y and 10Y refer to the lifetime of 1 year and 10 years of operation respectively.

noticed again, considering only ΔV_{th} will again leads to a wrong estimation. In practice, the predicted reduction in power due to aging will be overestimated. Note that this mainly due to neglecting the important role that aging-induced SS degradation has on static power estimation.

In fact, this might lead to a misleading conclusion that aging may significantly reduce the power of circuits [72–74]. Further details on explaining the impact of ΔV_{th}, $\Delta\mu$ and ΔSS on estimating delay and power of circuits along with the corresponding impact of every individual degradation can be found in [62].

3.3. Aging effects at system level

In the following we investigate the ultimate impact of aging-induced degradations on the probability of failure of computational units. In fact, this is necessary to answer the key question "whether we need to include a guardband or not assuming the circuits can tolerate errors like in image processing circuits". To achieve that, we study 32-bit Adder and Multiplier circuits. Both have been synthesized using the original (i.e. aging-unaware) cell library. Then, we perform our degradation-aware timing analysis as explained in the previous section. This provides us with the delay information of circuits, i.e. the static delay format (.sdf) files, under aging effects. We studied here different scenarios in which we show the impact of considering ΔV_{th} *solely* and considering ΔV_{th}, $\Delta\mu$ and ΔSS *jointly*. Afterwards, we run gate-level simulations in which we simulate the Adder and Multiplier circuits functionality under 10 K of random input data. This allows us to calculate the probability of failure in the studied circuits due to aging effects. In this analysis, the Synopsys tool flows have been employed to perform the required logic synthesis as well as the static timing analysis. In addition, the Modelsim simulator from Mentor Graphics has been used to perform the required gate-level simulations.

Fig. 32 summarizes our results. As it can be seen, aging effects results in a considerable probability of failure. This demonstrates the necessity of including guardbands. Note that neglecting the impact of aging on degrading μ and SS leads to underestimating the resulting probability of failure in both studied circuits (i.e. Adder and Multiplier).

Finally, we additionally studied the impact of aging effects on the DCT-IDCT chain circuit which is typically used to decode and encode

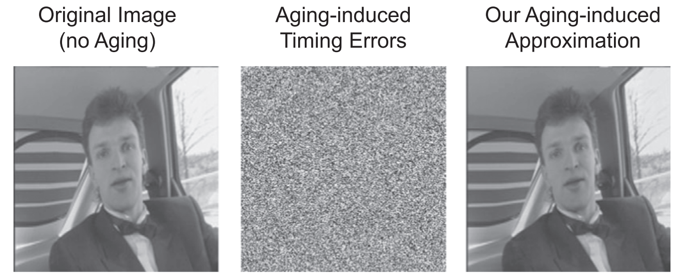

Fig. 34. Analyzing the impact of aging effects in DCT-IDCT circuits, which are used for encoding decoding images. As shown, aging-induced timing errors destroys the image quality completely. However, employing our aging-induced approximation method results in converting the stochastic timing errors into controlled approximations [75] and hence the quality of image remains high for a lifetime of 10 years despite aging effects.

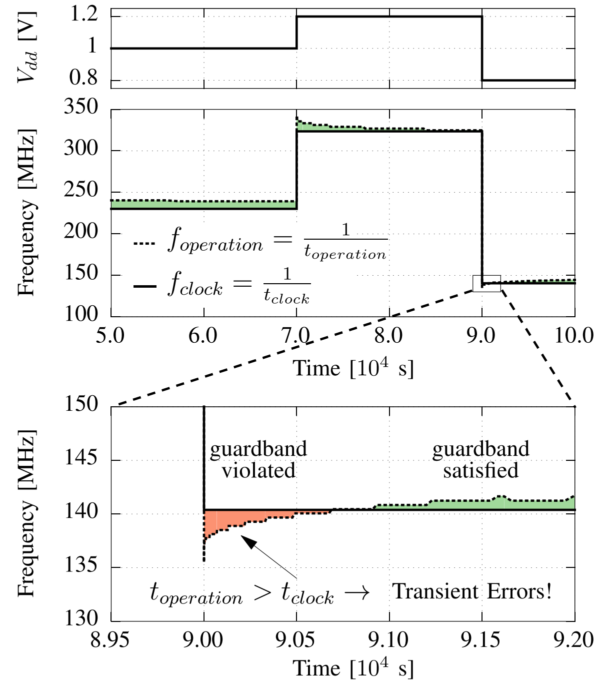

Fig. 35. Aging-induced degradations in conjunction with ultra-fast voltage switching leads to the so-called "**short-term effects of aging**" which are transient errors due to the temporary violation of guardband [77].

images. In Fig. 34 we show the impact of aging on the output image. As shown the image is totally corrupted and the Peak Signal to Noise Ratio (PSNR) is below 10db. *This again demonstrates the necessity of including guardbands even in error-tolerant circuits.*

Aging-induced approximation: In order to translate nondeterministic aging-induced timing errors into deterministic and controlled approximations instead, we presented in [75] how the required guardband can be converted into an equivalent reduction in precision. Fig. 33 demonstrates how reducing the precision of Multiplier from 32 bits to 29 bits is sufficient to compensate the aging-induced delay increase. Hence, by cutting the 3 LSBs (least significant bits) from the multiplier we guarantee that aging will never result in any timing errors even for a lifetime of 10 years under the worst case aging stress (i.e. continuous aging stress without any recovery). To demonstrate the impact of such precision reduction on the quality of images, we show in Fig. 34 the resulting image after reducing the precision by 3 bits. As shown, the image's quality is very similar to the original quality (i.e. before aging effects). In order words, aging-induced approximation allows us to convert the stochastic/nondeterministic timing errors induced by aging into deterministic and controlled approximations. *Hence, guardbands can be safely removed without jeopardizing the quality of circuits.*

3.4. Emerging aging effects: a paradigm shift form long-term to short-term reliability degradation

In recent technology, aging effects have become a subject to voltage switching due to the introduction of ultra-fast on-chip voltage regulators which are able to scale the voltage within a μs. As a matter of fact, aging-induced degradations get accelerated at higher V_{dd} (due to the higher applied electric fields) and vice versa [76]. At lower voltages, partial recovery of aging degradations which have been induced at the higher voltage start to occurs. However, switching V_{dd} in an ultra-fast manner may trigger *transient errors*, as the V_{dd} will be dropped significantly much faster (order of a 1 μs) than the speed of aging recovery [77]. Hence, transient errors temporally occur due to timing violations. After a short period of time, such transient timing errors stop as the lower voltage will recover the aging degradations. To demonstrate such "**short-term aging effects**", we show in Fig. 35 [77] how $t_{operation}$ temporarily grows larger than t_{clock} after switching to a lower V_{dd} level. This is because of the high aging-induced degradations (e.g., ΔV_{th}), originating from the high V_{dd} along with the negligible recovery within a very small transition time of <1 μs.

4. Conclusion

In this article, we have presented the latest development and advances for modeling and analysis of two most important failure mechanisms for nanometer VLSI systems: the electromigration for the interconnect wires and bias temperature instability (BTI) effects for CMOS devices.

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