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Electromigration assessment for power grid networks considering temperature and thermal stress effects ☆

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ABSTRACT

With technology scaling, reliability has emerged as a major design constraint for very-large-scale integrated circuits. Many prior works have investigated electromigration (EM) on full-chip power grid interconnects. However, most of the published results were obtained under the assumption of uniformly distributed temperature and/or residual stress across interconnects. In this paper, we demonstrate the implementation of novel methodology and flow for full-chip EM assessment on the multi-layered power grid networks of a 32 nm test-chip and investigate the impacts of the within-die temperature and thermal stress variations on the failure rate. The proposed approach is based on recently developed physics-based EM models and the EM-induced IR-drop degradation criterion that replaces the traditional conservative weakest segment method. The cross-layout temperature distribution caused by power dissipations in devices and by interconnect Joule heating has been characterized and taken into account in the full-chip EM assessment methodology. Results of the simulations performed on the analyzed multi-layered power/ground nets show that traditional assumption of the uniform average temperature leads to inaccurate predictions of the time-to-failure. Furthermore, the consideration of thermal stress variation results in a retarded EM induced degradation.

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1. Introduction

Electromigration (EM) is a physical phenomenon of the oriented migration of metal atoms along a direction of applied electrical field due to the momentum exchange between atoms and the conducting electrons. Migration of atoms results in metal density depletion or accumulation, which leads to built-up of hydrostatic stresses across conductor. The continuous shrinking of features sizes in modern integrated circuits has aggregated the EM-induced reliability treats. The chip interconnect is either used for the connection of different parts of design for a signal propagating, or used for voltage delivery. EM can degrade both these functions by degrading the conductivity of the individual segments of the interconnect circuits. The power delivery networks are more susceptible to EM effects than the signal lines as they carry large unidirectional currents, and thus can fail in much shorter times due to continuous stress buildup under EM action. The signal lines mainly carry bidirectional or pulsed currents. It results in a much longer EM-induced failure time caused by repetitive increase and decrease of the mechanical stress at the line ends, due to the excessive atom accumulation and depletion governed by the electron wind force and stress gradient. Recently, a number of works have been proposed to employ the EM-induced IR-drop degradation analysis as an EM assessment for power grid networks. This analysis considers the inherent redundancy of mesh-structured networks and power-delivery functionality of the grid [1–4], which replaced the traditional conservative weakest segment criterion. Currently employed Blech limit [5] (for the out filtration of immortal segments) and Black's equation [6]

$$MTTF = Aj^{-n}\exp\{E_a/k_BT\} \quad (1)$$

(for calculating mean-time-to-failure (MTTFs) for segments characterized by known current densities and temperatures) are subjects for the hard criticism [7–10]. Here, j is the current density, k_B is the Boltzmann's constant; T is the absolute temperature; E_a is the EM activation energy; the symbol A is a constant. Cross-die variation of residual stress makes the Blech's "critical product" to

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be layout dependent variables rather than experimentally determined constants.

The widely accepted methodology of calculating the MTTF at use condition, represented by chip operation current density and temperature, is using n and E_a determined at the stressed (accelerated) condition, which is characterized by high current densities and elevated temperatures. However, the interdependency of the Black's activation energy (E_a) and current density exponent (n) on the current density and temperature [8,9,7], makes this method rather controversial. The recently proposed new physics-based EM model for void initiation and evolution responsible for a time-dependent resistance degradation of the power/ground (P/G) nets can overcome all the flaws related to the Black–Blech formulation [10,3,4].

EM effect on a metal wire is governed by a combination effect of current density, local temperature and residual stress, as shown in [10,11,3,12]. The rapid increase in chip power dissipation and power density results in thermal hot spots and temperature gradients on the die. Thermal stress is a major source of the residual stress, which is mainly due to the significant mismatch in the coefficients of thermal expansion of the metal and the silicon surrounding it. Therefore in order to accurately estimate the risk of EM induced failure, the full-chip EM assessment methodology should not only account for the current densities but also consider the temperatures and residual stresses in different interconnect segments for different workloads. There have been many prior works focusing on EM analysis techniques under various scenarios. However, unfortunately, most of the published results were obtained under the assumption of uniformly distributed temperature and/or uniformly distributed residual stress across the chip [1–3,13]. These results will be not accurate enough to characterize the kinetics of void nucleation and void volume evolution responsible for EM-induced degradation and, hence, result in ineffective reliability optimization techniques.

This paper describes the implementation of novel methodology and flow for full-chip EM assessment for multi-layered power grids, considering the impacts of the cross-layout temperature and thermal stress variations on the failure rate. The proposed approach is based on recently developed physics-based EM models and the EM-induced IR-drop degradation criterion that replaced the traditional conservative weakest segment method. We conduct the experiments on a real 32 nm test-chip. The new approach consists of the following contributions: (i) characterization of power dissipation in devices and Joule heating in the interconnects, and the estimation of full chip temperature and thermal stress distribution by compact modeling; (ii) the implementation of the novel methodology and flow of EM-reliability assessment of the power grids, accounting the within-die temperature and thermal stress variations.

The paper is organized as follows: Section 2 reviews the physics of electromigration and the physics-based models for void nucleation and growth. Sections 3 and 4 present the proposed new power grid reliability analysis method considering the with-in die temperature and thermal stress distributions based on the physics-based EM models. The experimental results are discussed in Section 5. Section 6 concludes the paper.

2. Electromigration modeling review

In this section, we review the physics-based modeling of EM phenomena in on-chip interconnects. EM effect on metal wires results in metal density depletion or accumulation, which is accompanied by development of the corresponding tensile or compressive hydrostatic stresses at the locations characterized by the atomic flux divergences, for example at the ends of the metal lines embedded in inter-layer/inter-metal dielectrics (ILD/IMD). Over time, the lasting unidirectional electrical load increases these stresses, as well as the stress gradient along the metal line. In some cases, usually when a line is long, this stress can reach critical levels, resulting in a void nucleation at the cathode and/or hillock formation at the anode end of line, Fig. 1. The recently proposed physics-based EM models for void initiation and evolution that cause a time-dependent degradation of the segment electrical characteristics allow accurate prediction of interconnect failure rate caused by impacts of current density, temperature and residual stress to be made [10,3,4]. From the view of EM-induced degradation the modern power grid networks consist of a set of interconnect elemental reliability units, also known as interconnect trees [14], representing continuously connected, highly conductive metal lines within one layer of metallization, terminated by diffusion barriers, Fig. 2. The absence of blocking boundaries at one or both ends of the branches allows atoms to transfer between connected limbs in a tree preventing them from accumulation/depletion, and hence, eliminates related stress buildup at the branch connections. Thus the traditional immortality assessment and the time-to-failure (TTF) calculation methods, which are based on a single interconnect line confined by IMD/ILD dielectric, is not applicable for the power grid analysis. Instead, we should perform tree-based analysis, which deals with the grid structure and takes into account the stress redistribution between the connected branches in a tree.

The EM process can be characterized as a sequence of two events: *void nucleation* and a sub-sequencing *void growth*. Void

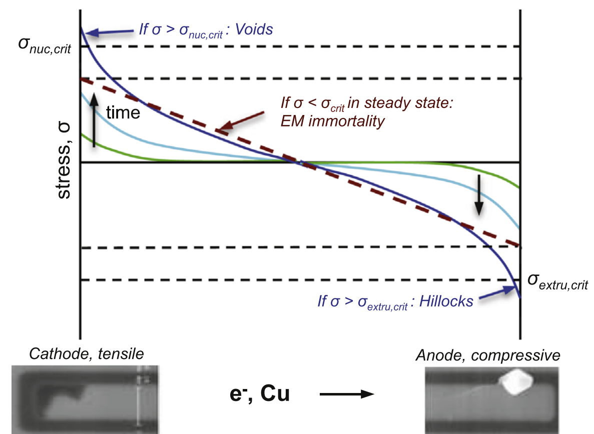


Fig. 1. The stress development and distribution in EM [15].

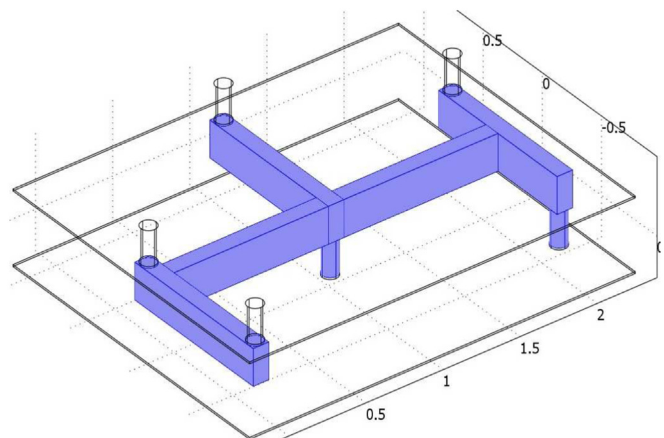


Fig. 2. Interconnect tree confined by diffusion barriers/liners.

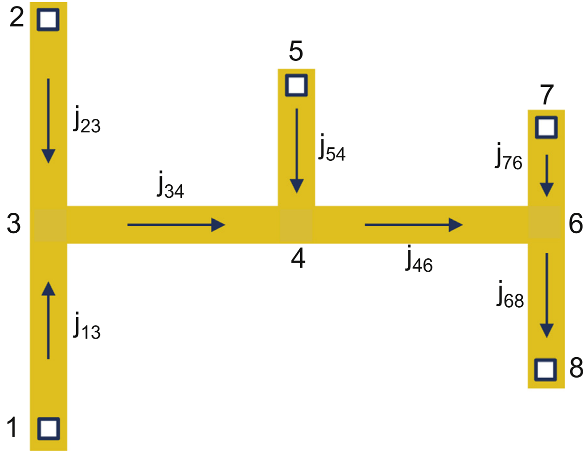


Fig. 3. Example of an interconnect tree.

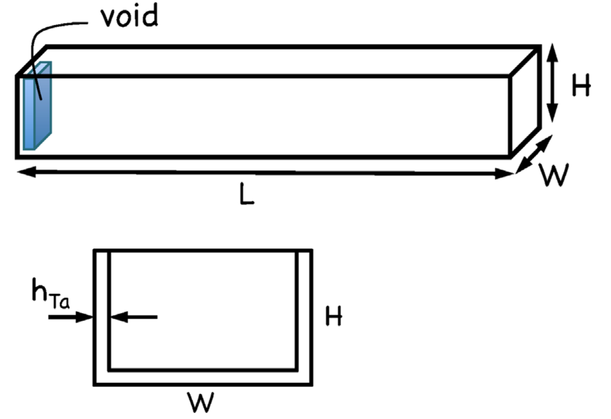


Fig. 4. Schematics of the line geometry.

nucleation kinetics in the interconnect segment can be derived from the solution of kinetics equation describing the time evolution of stress in the interconnect segment [11,16–18]. Void nucleation time (t_{nuc}) is determined as an instant in time when stress at the cathode end of the line, characterized by the biggest tensile stress, reaches the critical stress (σ_{crit}) and can be calculated as [3]:

$$t_{\text{nuc}} \approx \frac{L^2}{2D_0}\frac{k_B T}{\Omega B}\exp\left\{\frac{E_V + E_D - \Omega^* \sigma_{\text{crit}}}{k_B T}\right\} \cdot \ln\left\{\frac{\sigma_{\text{EM}}}{\sigma_T + \sigma_{\text{EM}} - \sigma_{\text{crit}}}\right\} \quad (2)$$

where the steady state EM stress at cathode end of a wire σ_{EM} is a function of current density j and wire length L, and $\sigma_{\text{EM}} = \frac{eZ\rho jL}{2\Omega}$ for a 1D confined line. Here, E_V and E_D are the activation energy of vacancy formation and diffusion, eZ is the effective charge of migrating atoms, ρ is the metal resistivity, k_B is the Boltzmann constant, T is the temperature, Ω is the atomic lattice volume, activation volume $\Omega^* \approx 0.95\Omega$ is the combination of the vacancy formation and the migration volumes [19], σ_T is the thermal stress developed in the metal line confined in the ILD/IMD environment during cooling from the zero stress temperature T_{zs} down to the temperature of use condition T, B is the bulk modulus [10,3]. For an interconnect tree, Fig. 3, the hydrostatic stress (including EM stress and residual stress) at the at all nodes of the tree should be obtained based on Eqs. (3) and (4), under a void-less steady state assumption, [3]:

$$\sigma_i^c - \sigma_j^a = {}^{\triangle}\sigma_{ij} = -\frac{eZ\rho j_{ij} L_{ij}}{\Omega} \quad (3)$$

$$\sum_{i=1}^{k}\left(\sigma_i - \left[\sigma_T + \frac{eZ\rho j_{ij} L_{ij}}{2\Omega}\right]\right) L_{ij} = 0 \quad (4)$$

where σ_i^c and σ_j^a are the hydrostatic stresses at the cathode and anode ends of the ij-branch.

Critical void formed at t_{nuc} grows its volume above critical one at $t > t_{\text{nuc}}$. The kinetics of the void volume evolution governs the evolution of the segment electrical resistance. In the growth phase, the resistance of a void containing branch increases over time. As a result, the P/G network becomes a time-varying network and its IR drops will keep changing over time. The kinetics of line resistance change can be approximately described as [3,4]:

$$\Delta R(t) = \vartheta \cdot (t - t_{\text{nuc}}) \cdot \left[\frac{\rho_{\text{Ta}}}{h_{\text{Ta}}(2H + W)} - \frac{\rho_{\text{Cu}}}{HW}\right] \quad (5)$$

where $\vartheta = \frac{D_a eZ\rho_{\text{Cu}} j}{k_B T}$ is the void edge drift velocity, D_a is the effective atomic diffusivity. Here, as schematically shown in Fig. 4, ρ_{Ta} and ρ_{Cu} are the resistivities of the barrier material (T_a/T_aN) and copper,

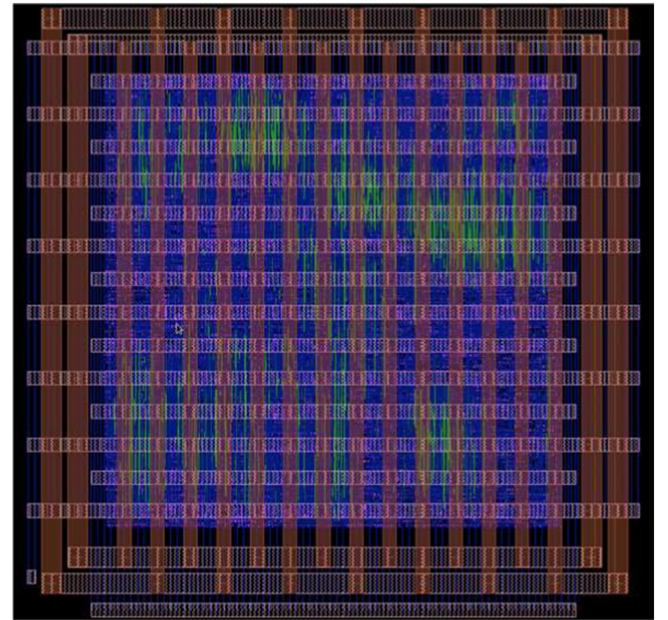


Fig. 5. Layout of 32 nm test-chip.

W is the line width, H is the copper thickness, and h_{Ta} is the barrier layer thickness.

The void saturated volume develops when growing void consumes all volumetric deformation generated by thermal stress and by redistribution of atoms removed from the space occupied by growing void. Once the void volume becomes saturated, the further resistance change is stopped until the current density will be changed due to other voids developed somewhere inside same interconnect tree or in other trees. If the wire is stressed under constant current density, the saturated void volume can be calculated as $V_{\text{SS}}^{\text{volm}} = V_{\text{line}}^{\text{volm}}(\sigma_T + \sigma_{\text{EM}})/\Omega$, where $V_{\text{line}}^{\text{volm}}$ is the volume of the metal line [20].

3. Cross-layout temperature and thermal stress characterization

This section describes the estimation of within-die temperature and thermal stress distribution. We demonstrate the characterization of power dissipation in the devices and the Joule heating in interconnects, then, we detail the temperature simulation methodology, which builds a thermal netlist with the effective thermal properties. Further, the thermal stress variation across the layout will be obtained

based on the temperature distribution. A 32 nm test-chip is used as the case example to present the flow. Standard-cells are used in this design along with 7 metal (copper) layers. Fig. 5 shows the layout of this design with dimension 184 μm × 184 μm. There are 16 layers in total (the Si-layer is divided into a thin Si-device layer that includes power dissipation and a thick Si-substrate layer for thermal analysis purpose). The BEOL (Back-End-of-Line) geometry information is described in Table 1.

3.1. Full-chip power characterization

Power estimation is a challenging task since the result is highly dependent on the workload or typical usage of a chip. We consider both the power dissipation in the devices and Joule heating in interconnects. The chip power consists of static and dynamic components. Eq. (6) is the power model for each individual primitive block, where a block is considered to be a primitive if it cannot be further decomposed into smaller blocks based on an user settings. The dynamic power comes from the gate switching, in which the block dissipates power by charging the load capacitances of wires and gates and dissipates power during a very short period of time when a conduction path exists between the power and ground voltage connections. Thus, more active block is characterized by the higher dynamic power. In contrast, the static power is due to static current, including the leakage current and presents regardless of a block's activity level.

$$P_{block} = P_{static} + \alpha_{switching} \times P_{dynamic} \quad (6)$$

Here, P_{static} and $P_{dynamic}$ are the static and dynamic powers of a block, $\alpha_{switching}$ is the switching estimate for signals that describes the switching activity of the block.

For time varying currents, the time scale is on the order of picosecond, which is too fine for the thermal time scale. As a result, power averaging is further applied to obtain the power consumption in the device layer. The current flowing through interconnects generates Joule heating. Similar to Eq. (6), we estimate the Joule heating in a wire by evaluating both static and dynamic components of generated heat. Fig. 6a is the power map for the device layer. We selectively show the Joule heating in M1, M3 and M6 layers in Fig. 6b–d.

3.2. Thermal simulation methodology

Since the temperature affects atom diffusivity, the EM assessment requires accurate local temperature estimation at each interconnect layer in order to adequately account for the

Table 1
Geometry of > power grid interconnects (μm).

Layer	Contact	M1	V1	M2	V2	M3	V3	M4	V4	M5	V5	M6	V6	M7
Layer number	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Width	–	0.066	–	0.066	–	0.2	–	0.2	–	0.36	–	6	–	6
Thickness	0.2	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.6	0.9	0.9	0.9

Layer1: Si-substrate; Layer2: device layer.

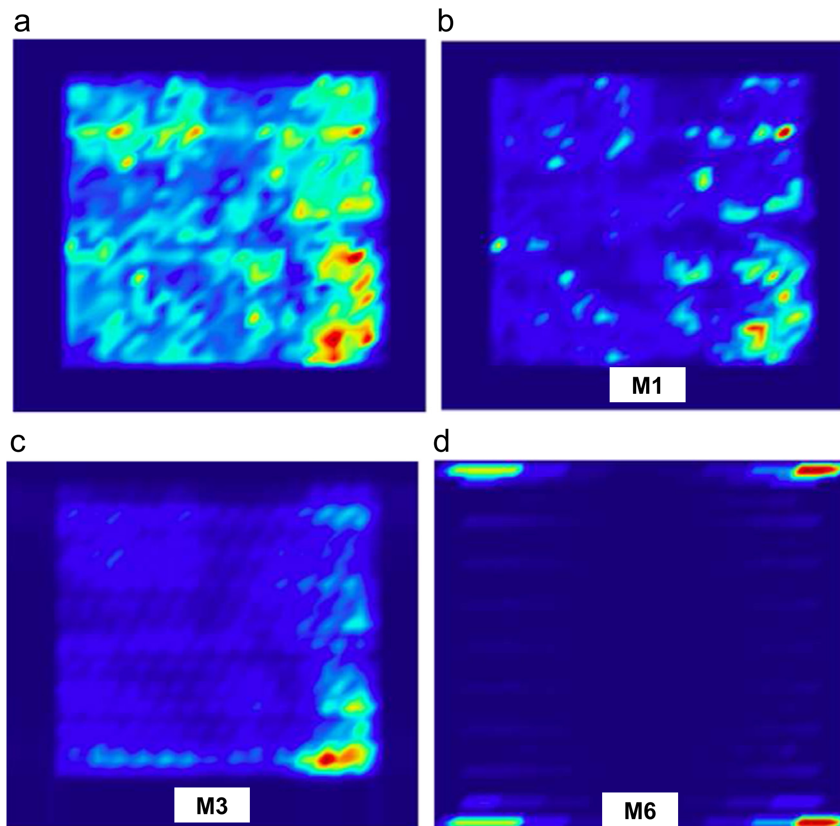


Fig. 6. Power consumption in device layer (0–6.91 mW), (a), and Joule in M1 (0–0.06 mW), (b), M3 (0–0.33 mW), (c), and M6 (0–4.53 mW), (d), layers.

temperature-sensitive void nucleation and growth kinetics. In this section, we describe a thermal analysis flow that efficiently estimates the cross-die temperature variation by employing a compact thermal model that represents a die as arrays of cuboidal thermal cells with effective local thermal properties. The methodology includes three steps: (i) extract effective thermal properties of a thermal cell in a layer, (ii) generate thermal netlist of the whole chip, and (iii) calculate temperature at each thermal node by a circuit solver, see for example [21,22]. As shown in Fig. 7, all considered composite layers are divided into a set of thermal cells defined by a layer thickness and a square window of size L which is chosen based on the simulation accuracy: the finer partitioning provides more accurate results at the expense of the run time. Each cell contains 6 thermal resistors representing heat propagation in the lateral and vertical directions; a thermal capacitance can be included for transient thermal analysis.

The effective thermal conductivities are functions of metal density and routing direction of wires in each metal layer based on the theory of effective thermal properties of anisotropic composite materials [23]. Based on the standard procedure [21,22], with the extracted thermal resistances e.g. Fig. 8, estimated power sources, as well as the thermal boundary conditions, the chip can be represented as a thermal netlist, in which the nodal temperatures correspond to the nodal voltages and the powers corresponds to the currents. The electric circuit solver can then obtain temperature for each thermal node. In the thermal simulation, performed in the analyzed design, a window size $L=5\ \mu m$ was chosen for computational efficiency while keeping reasonable temperature resolution. The top surface of the die was kept at $T=330$ K, while all other sides were insulated. As shown in Fig. 9, the temperature varies across different layers. The temperature distribution in M1 interconnects is shown in Fig. 10.

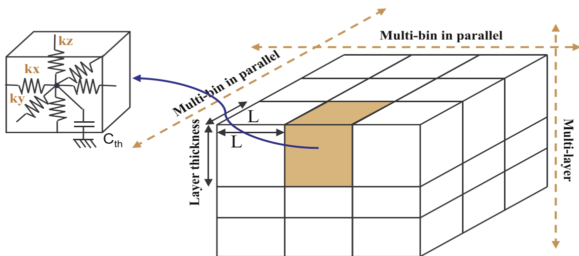


Fig. 7. The die is divided into arrays of thermal cells with 6 thermal resistances in each cell (bin).

3.3. Thermal stress estimation

Since the residual stress existing in each metal line before the electrical load is applied is responsible for both void nucleation and growth, its distribution should be considered for accurate chip-scale EM assessment. This work focuses on the thermal stress, which is a major source of the residual stress. In the case of metal line embedded into the rigid confinement, which, in the analyzed case of the on-chip interconnect, is comprised by refractive metal and dielectric diffusion barriers and ILD/IMD dielectrics, the initial stress is generated during the system cooling from the stress-free annealing temperature T_{ZS} down to the use temperature T. A primary source of this thermal stress is the difference in the coefficients of thermal expansion of the metal α_M and confinement α_{conf}, which is mainly determined by the silicon substrate:

$$\sigma_T = B(\alpha_M - \alpha_{conf})(T_{ZS} - T) \quad (7)$$

The thermal stress distribution in the M1 layer is demonstrated in Fig. 11. Since a lower thermal stress corresponds to a higher layout temperature due to the smaller temperature gap $\Delta T = T_{ZS} - T$, the regions with the highest T, Fig. 10, are characterized by the smallest σ_T, Fig. 11. Note that more accurate thermal stress estimation

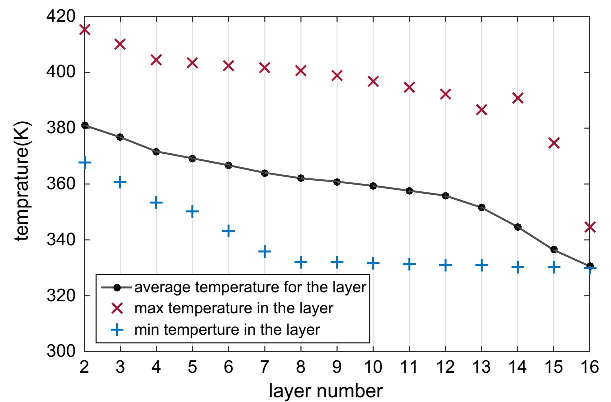


Fig. 9. Temperature (K) variation across different layers.

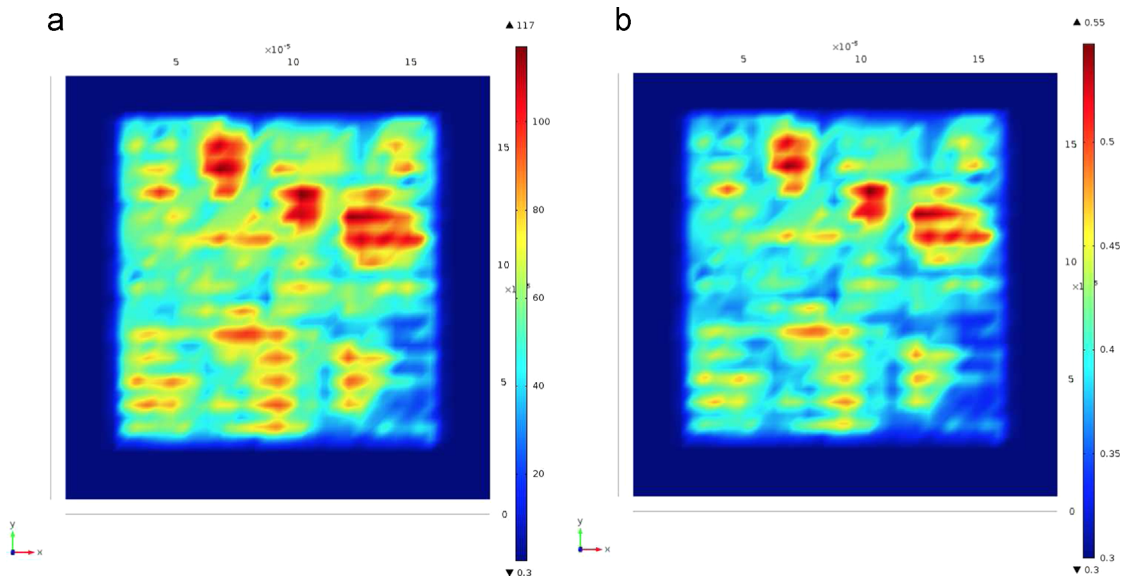


Fig. 8. Effective thermal resistance of M2 layer in (a) x direction and (b) y direction.

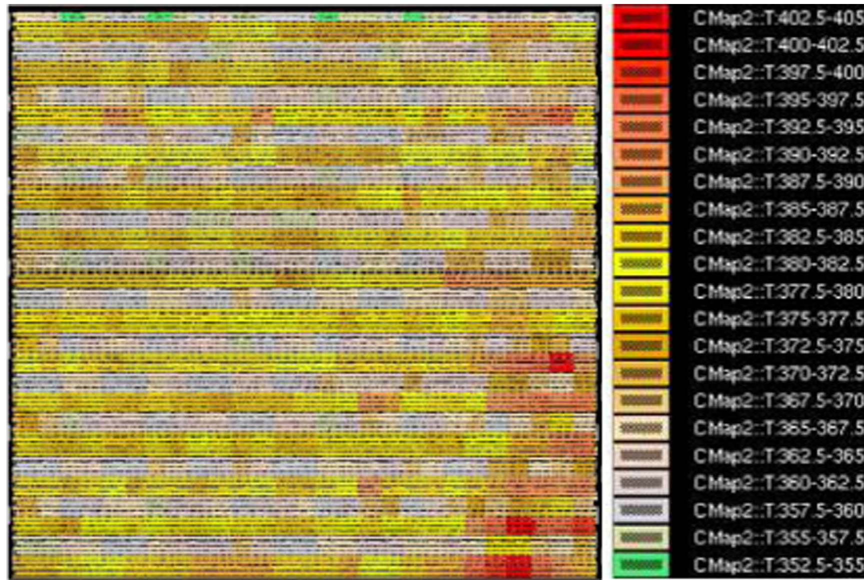


Fig. 10. Temperature (K) distribution in M1 layer.

should consider the elastic portion of the stress generated by interaction with confinement. This is reserved for the future analysis. Nevertheless, the calculated inelastic fraction of the thermal stress demonstrates well the trend caused by the thermal stress variation and its relation to the temperature distribution.

4. Full-chip EM analysis flow

Now we present the new EM-induced reliability analysis algorithm and flow for P/G networks of the 32 nm test-chip, which accounts for the impacts of within-die temperature and thermal stress variations. As stated in Algorithm 1, the EM assessment is achieved through the following steps:

- *IP block modeling and power grid network extraction*: Model IP block's interaction with the P/G nets through pre-defined connections (pin locations) under various conditions (e.g. input slew and output loading capacitance): run circuit simulations of the transistor netlist annotated with the layout parasitic information; estimate block's activity based on realistic circuit behaviors, such as the percentage of design switching within a clock cycle. Assuming that each standard cell used in this design has a power (V_{DD}) pin and a ground (V_{SS}) pin associated with the power grids, we extract the P/G networks as parasitic circuits with each P/G pin modeled as a DC current source: $I_{DC} = I_{leakage} + \alpha_{switching} I_{ON}$.
- *Cross-layout temperature and thermal stress characterization*: First, we characterize power dissipation in devices and Joule heating in interconnects by Eq. (6). Then, upon dividing each layer into multi thermal cells the local effective thermal properties are computed. The die is further modeled as an equivalent thermal circuit, where the power is represented as current and the temperature is denoted by voltage. We solve the thermal net and get the temperature distribution across the die. Further, the thermal stress distribution can be obtained based on Eq. (7). Finally, we map the temperatures and the thermal stresses into the layout.
- *Full-chip EM analysis considering within-die temperature and thermal stress distributions*: Each of the interconnect branches is now assigned a local temperature and a local thermal stress, replacing the average values used in the traditional EM analysis. In the formulation of the dynamic P/G networks, the hydrostatic stress is analyzed in interconnect trees; the wire resistance begins to change (increase) starting with the nucleation time (t_{nuc}), calculated by Eq. (2), and later their resistance changes are estimated by Eq. (5). The generation of void saturated volume should be checked before updating the resistance. As indicated in step7 in Algorithm 1, the P/G network starts to degrade after the first void have nucleated at $t = \min\{t^i_{nuc}\}$, which is characterized by both hydrostatic stress and temperature. Then at each instant in time $t{:=}t+\Delta t$, we update resistance of all branches with non-saturated voids; recalculate current density and hydrostatic stress; and check if there are any new voids nucleated during the previous time increment Δt. The chosen time-step Δt should be small enough to detect approximately an instant in time when the critical stress is developed in any branch of any tree. We continue the process until the IR drops at one or more nodes reaches the given threshold, for example, $10\% V_{DD}$ or when the time instant has reached the required lifetime (LT_{REQ}).

Algorithm 1. New power grid EM-induced reliability analysis algorithm considering cross-layout temperature and thermal stress variations.

Require: Layout design files, required chip LT (LT_{REQ}), chip failure criteria, time step (Δt)
Ensure: TTF and failed segment (if $TTF < LT_{REQ}$), largest IR drop, void locations
1: IP block power modeling and P/G network extraction.
2: Chip power consumption and interconnect Joule heating estimation.
3: Thermal analysis: obtain within-die temperature and thermal stress distribution. Apply results in following full-chip EM assessment.
4: Divide the P/G nets into a set of interconnect trees.
5: Calculate the initial effective EM current density for each branch and compute the steady state distributions of hydrostatic stress inside each interconnect tree.
6: Find all suspicious branches with the tensile stress larger than the critical value. Find nucleation time for the first void ($t_0 = \min\{t^i_{nuc}\}$).
7: Start the analysis from time $t = t_0$. Branch with the first nucleated void enters the growth phase.
8: **while** the largest IR drop $\leq$ threshold or $t < LT_{REQ}$ **do**

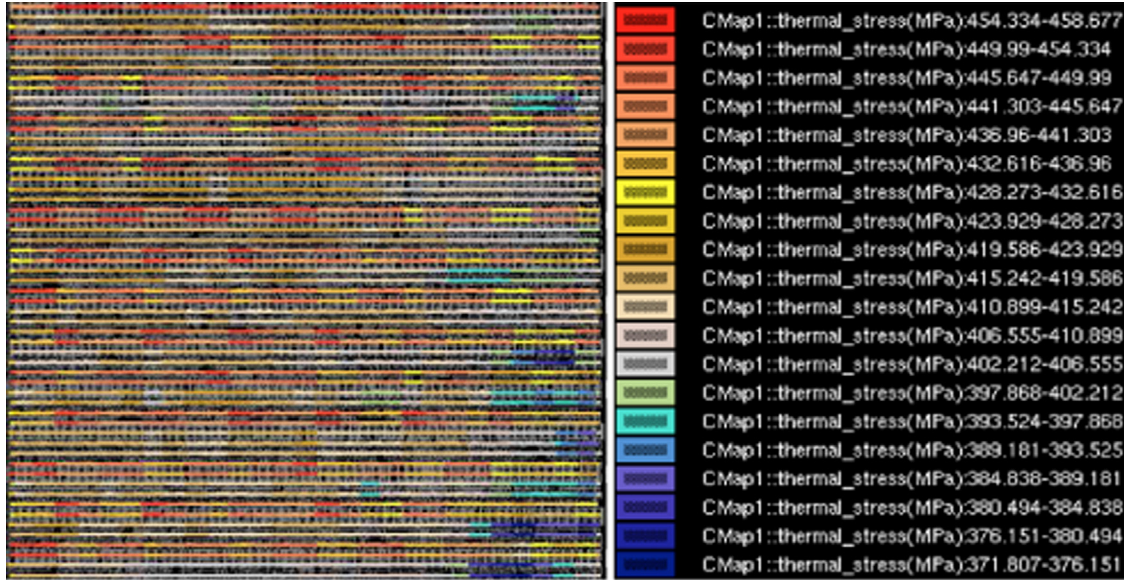


Fig. 11. Thermal stress (MPa) distribution in M1 layer.

Table 2
Parameters used in EM model.

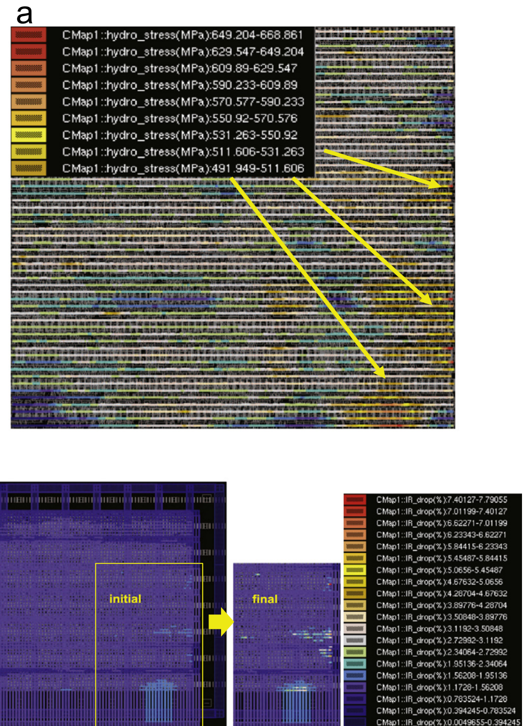
Parameter	Value	Parameter	Value
E_V	0.73 eV	Z	10
E_D	0.53 eV	σ_{crit}	500 MPa
Z	10	T_{ZS}	623 K
B	1×10^{11} Pa	D_0	7.56×10^{-3} m^2/s

9: Move to next instant in time $t := t + \Delta t$: For branches in the growth phase, update resistance for branches with non-saturated voids.
10: Perform the DC analysis of the P/G nets. Re-compute the hydrostatic stress distribution inside each tree.
11: For each tree, find the minimum void nucleation time ($\min\{t^i_{nuc}$) for all suspicious branches in the nucleation phase. If $\min\{t^i_{nuc}\} \le t$, the corresponding branches steps into the growth phase.
12: **end while**
13: Output t, IR drop map and locations of voids

5. Experimental results and discussion

The proposed full-chip thermal variation aware-EM assessment method is implemented by C++ code on a 2.4 GHz Linux server and tested on the 32 nm standard-cell IC design. We use Calibre tools for layout extraction and circuit analysis. The EM analysis results can be mapped into the BEOL layout and displayed in Calibre RVE tool. The power net and ground net are symmetrical and independent on each other since the standard cells are modeled as effective DC current sources. In this work, the thermal analysis targets the whole chip and the EM analysis focuses on the power net. We assume the chip fails when the maximum IR drop exceeds $10\% V_{DD}$. Parameters used in EM model are listed in Table 2.

Fig. 12(a) demonstrates the EM-induced IR drop increase in the power net. The results show that the most significant IR drop change happens in the M1 layer, which is the closest layer to devices. Comparing it with the initial steady state hydrostatic stress shown in Fig. 12(b), which includes the thermal stress and



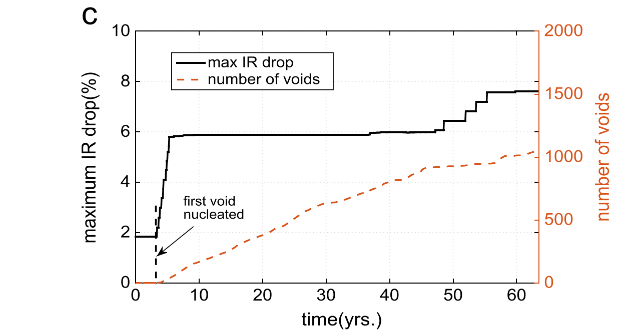


Fig. 12. (a) Steady state hydrostatic stress map of M1 layer predicted by initial current densities (the distribution of thermal stress is taken into account), (b) EM-induced IR drops change in the power net, and (c) the increase of the maximum IR drop and number of nucleated voids over time.

the steady state EM stress computed by the initial current densities, and with the temperature distribution shown in Fig. 10, we can get the conclusion that the EM induced IR drop degradation is more likely to happen at the locations with both high hydrostatic stress and high local temperature. Fig. 12(c) plots the change of the largest IR drop in the power net over time, caused by the increasing number of nucleated voids. It shows that the worst IR drop is smaller than $10\%V_{DD}(V_{DD} = 1.1\text{ V})$ when the simulation stops, which means this chip has a longer lifetime than the requirement.

5.1. Effect of cross-layout temperature variation

To evaluate the impact of within-die temperature variation, we performed EM assessment under assumption of uniform temperature (T=367.4 K, averaged temperature across the chip) and with the calculated non-uniform temperature distribution. Uniform average thermal stress $\sigma_T = 434.55$ MPa was assumed in both cases. The evolution of IR drop degradation and the locations of branches with voids when the simulation stops, are shown in Figs. 13 and 14 respectively.

We have several interesting observations: first, the accelerated voltage degradation caused by high local temperatures at lower layers was observed in the case of non-uniform temperature distribution during the earlier time. Second, as time goes by, the drastic IR drop increase is found under the average temperature assumption. At this time these two assumptions result in totally different analysis results (the average temperature case causes a false-alarm chip failure). This is mainly due to the incorrect prediction of voids nucleated in the top layers where the actual local temperature is much lower than the average value, which can be viewed by comparing Fig. 14(a) and (b).

5.2. Effect of spatial thermal stress variation

Next, we have investigated the impact of thermal stress on EM effects by comparing the IR drop evolution in two cases characterized by non-uniform and uniform ($\sigma_T = 434.55$ MPa) thermal stress distributions. Fig. 15 shows the IR drop evolution taking place in these two cases. Contrary to the impacts of spatial temperature variation, the retarded voltage degradation has been observed when the thermal stress variation was taken into account. The failure prefers to happen at places where both the hydrostatic stress and local temperature are high. Since a higher temperature corresponds to a lower thermal stress, when spatial

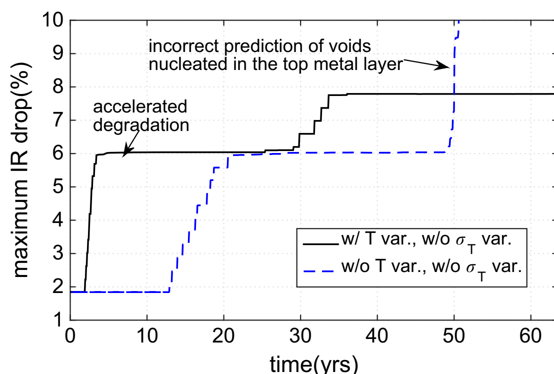


Fig. 13. Comparison of predicted maximum IR drop increase between w/o and w/ temperature variation conditions. Uniformly distributed thermal stress is considered in both cases.

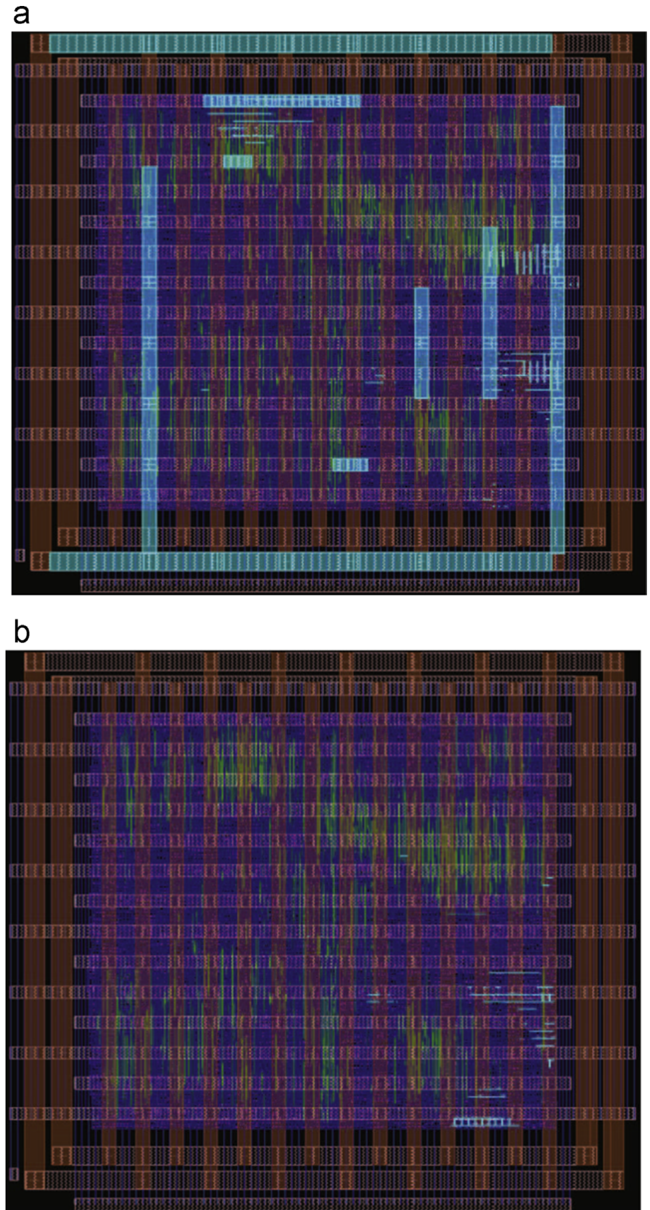


Fig. 14. The branches with voids (blue color) at the time when simulation stops in two cases: (a) uniform averaged temperature, and (b) with temperature variation. Uniform thermal stress distribution is considered in both cases. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

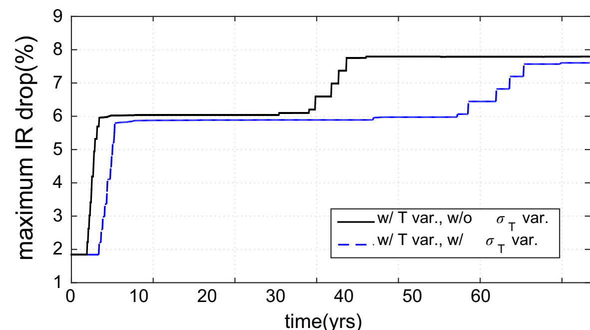


Fig. 15. Comparison of the IR drop evolutions calculated w/o and w/thermal variation assessments. Temperature variation is considered in both cases.

thermal stress variation is considered, the branches with the high temperature have smaller initial stresses compared with the average value, thus a longer evolution time is needed for stress to reach the critical value required for void nucleation.

6. Conclusion

In this work, we have proposed and implemented a new EM assessment method for the multi-layered power grid networks of a 32 nm test-chip, based on recently proposed physics-based EM models and the EM-induced IR drop degradation criterion. The proposed method characterizes the within-die temperature variation caused by power dissipation in devices and by Joule heating in interconnects, and investigates its impacts on failure rate of power grid networks. It also accounts the across chip thermal stress variation. The experimental results show that the EM-induced degradation is a combined effect of temperature and hydrostatic stress. Employing traditional uniform average temperature assumption leads to inaccurate predictions of the TTF. It also reveals that the consideration of thermal stress variation results in a retarded voltage degradation.

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