UiMOR – UC Riverside Model Order Reduction Tool for Post-Layout Wideband Interconnect Modeling [*]

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ABSTRACT

In this paper, we introduce a new model order reduction tool, *UiMOR* – UC Riverside Model Order Reduction Tool. UiMOR fills the gap between parasitic extraction and post-layout simulation to improve the efficiency of VLSI circuit validation. UiMOR is a stand-alone circuit complexity reduction tool. It can perform accurate reduction for wideband frequency range with negligible loss of accuracy and is well suited for analog/mixed-signal/memory designs. It also works well for traditional delay and noise calculations in digital circuits. It works seamlessly with the existing digital and analog design tools that use the standard SPICE format interface. We then present some numerical comparison results with an existing industry tool, Ultrasim. *UiMOR* is now available for free download from UC Riverside

1. INTRODUCTION

Complexity reduction (also called model order reduction) is to reduce the interconnect circuit model complexity while preserving accuracy of the original circuit model to boost the verification process at the post-layout stage. It fills the emerging gap between the parasitic extraction and post-layout simulation as an increasing number of parasitic components (resistance, capacitance, self and mutual inductance) are required to model the physical reality of circuit interconnects, substrates, packages.

Circuit complexity reduction becomes indispensable as the complexity of nanometer integrated circuits, especially the unavoidable interconnect parasitics grow very rapidly (almost exponentially). This is driven by requirements of observing the finer levels of physical effects for accurate verification of increasing design concerns like noise, signal integrity, cross coupling, and even quantum effects as technologies advance below 100nm. The massive extracted parasitics can significantly degrade performance of today's SPICE-level commercial simulation tools. Excessive simulation time leads to long design time and large simulation tool budgets.

The reduction techniques for linear interconnect circuits have been studied intensively in the past and many techniques have been proposed [18]. The dominating methods are still based on subspace projection. In terms of projection subspace, these approaches are divided into two broad categories: moment-matching based methods (Krylov subspace methods) [14, 4, 16, 11, 15, 5, 17, 7] and balanced truncation based methods[9, 8, 12, 21, 19, 22, 13, 23, 6, 24, 20]. In the former case, the system is projected onto a subspace to match dominant moments of transfer functions, while in the latter case the system is projected onto a subspace that is both easily controllable and easily observable. A more detailed survey of model order reduction techniques can be found [18, 3].

Existing techniques such as moment-matching based methods are mainly used for computing the interconnect delays and coupling noises in digital circuits. Those techniques lack the accuracy for the wide frequency ranges required for modeling analog mixed-signal and RF/MM circuits. Also the reduced models in the circuit matrix formats can not be easily transformed back into the circuit-level format compatible with the general circuit-level SPICE format. Those reduction methods have been integrated with the existing timing analysis tools to only compute the delay and noise of interconnects. As of now, the major EDA companies do not offer the stand-alone reduction tools, although there are startup efforts going on now to address this emerging requirement.

UiMOR is a new circuit complexity reduction tool developed by MSLAB at UC Riverside. It combines many advanced reduction techniques developed in the Mixed-Signal Nanometer VLSI Research Lab (MSLAB) at UC Riverside in the past decade [18]. UiMOR is a stand-alone circuit complexity reduction tool. It can perform accurate reduction for wideband frequency range with negligible loss of accuracy and is well suited for analog, mixed-signal, RF and memory designs. It also works well for traditional delay and noise calculations in digital circuits and consists of all the mainstream reduction methods such as moment matching and fast balanced truncated realization.

UiMOR aims at reducing the amount of data in the netlist; reducing the memory footprint. As a result, it can speed up simulation without degrading simulation accuracy. UiMOR can read in the interconnect circuits modeled as RC/RLC circuits and produce the reduced RC/RLC circuits in SPICE format. Designers can specify the intended frequency range in which the reduced models will be accurate in its analog model reduction (more on this in the next section). UiMOR offers three algorithms to perform model reduction including the moment-matching (Krylov-subspace) method, sampling based method, and an adaptive sampling method. As a result, UiMOR offers users the freedom to choose the one most suitable for their own problems. UiMOR has several features and advantages over the existing reduction techniques:

1. True SPICE compatibility: SPICE-in, SPICE-out reduction technique.
2. Fits seamlessly with the existing post-layout verification flow.
3. First wide-band reduction technique for digital, analog/mixed-signal/RF circuits designs.
4. Extremely efficient for RC circuits with very little accuracy loss. Can achieve 10-100× reduction ratio.
5. Very scalable and efficient for reducing interconnect circuits with millions of nodes.

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[*] This work is supported in part by NSF grant under No. CCF-0448534, in part by National Natural Science Foundation of China (NSFC) grant under No. 60828008.

978-1-4244-5800-4/10/$26.00 ©2010 IEEE

The reduction techniques developed in UiMOR have the potential to bring immediate impacts on the VLSI chip design community as it can reduce the verification time of VLSI chip design, especially for the analog, mixed-signal and RF circuits, in the post-layout stages. The reduced simulation time can directly translate to improved efficiency and the saving in the simulation tool budgets and total design costs as few licenses are required and more simulation runs can be carried out for each design. UiMOR Version 1.0 now is available and can be downloaded from MSLAB website [2].

This paper is organized as the following: Section 2 introduces some basic features in UiMOR. Section 3 gives the algorithm flow of UiMOR. Some numerical results are given in Section 4 and Section 5

2. THE CAPABILITIES AND IMPORTANT FEATURES OF UIMOR

2.1 Interface for UiMOR

UiMOR takes a SPICE compatible netlist as input and then generates the internal matrices for the reduction process. After the reduction, it will create a SPICE compatible netlist frmo the reduced matrices.

Internally, UiMOR still represents the interconnect systems in terms of Modified Nodal Analysis (MNA) matrices. Specifically, for a system with n states and p ports, its MNA is expressed as

$$\begin{aligned} Gx(s) + sCx(s) &= Bu(s), \\ y(s) &= B^T x(s), \end{aligned} \tag{1}$$

where $G \in \mathbb{R}^{n\times n}$, $C \in \mathbb{R}^{n\times n}$, $B \in \mathbb{R}^{n\times p}$. We call G, C, B the system matrices. UiMOR reads in the SPICE compatible netlist directly and automatically generates the system matrices G, C, B through its built-in parser.

After reduction, the reduced system has an MNA formulation

$$\begin{aligned} \hat{G}\hat{x}(s) + s\hat{C}\hat{x}(s) &= \hat{B}u(s), \\ y(s) &= \hat{B}^T \hat{x}(s). \end{aligned} \tag{2}$$

where $\hat{G} \in \mathbb{R}^{q\times q}$, $\hat{C} \in \mathbb{R}^{q\times q}$, $\hat{B} \in \mathbb{R}^{q\times p}$. q is the reduced system order which is defined by the user or determined automatically by UiMOR (in the adaptive algorithm).

In the end, UiMOR will realize the reduced system matrices $\hat{G}$, $\hat{C}$ and $\hat{B}$ into a practical circuit and write it into a SPICE netlist as output.

2.2 Reduction algorithms used in UiMOR

To make UiMOR more versatile and adaptive for different applications, we have implemented several reduction algorithms in UiMOR and users can select the most suitable one for their applications. UiMOR offers three main algorithms for reduction: the Krylov-subspace based method for fast delay and noise calculations, the sampling based TBR method for better accuracy control, and the adaptive sampling based method for the most accurate requirments such as those for interconnect circuits of analog, memory, RF, and mixed-signal circuits.

The first one is a Krylov-subspace or moment-matching based method. The main advantage of this algorithm is its efficiency and simplicity of use. It is the fastest among the three algorithms but it is also the least accurate method. The user only needs to provide one parameter: the order of the reduced system. Although with local accuracy (set to be accurate at DC in UiMOR), the Krylov-subspace based method can still find a good reduced model for RC circuits whose frequency responses are usually simple with a few dominant poles. In UiMOR, the ”-m *delay*” parameter is used to select the reduction mode. The value of is used to indicate this reduction algorithm option.

Table 1: Comparison of three algorithms used in UiMOR.

Algorithm	Speed	Accuracy	Parameters
Krylov-subspace	fast	low	order
Sampling-based	balanced	balanced	order, freq range, sample #
Adaptive-based	slow	high	freq range, max error

Another choice in UiMOR is the sampling based method. It tries to find a balance between accuracy and speed. In addition to providing the reduction order, the user also needs to specify the frequency range (the minimum and maximum frequencies) and number of sample points to be used. The frequency range should cover the frequencies required by the user and number of sample points should be large enough to achieve the desired accuracy. Typically, more sampling points means more accurate results but at higher computing cost and larger model sizes. In UiMOR, the ”-m *analog*” parameter along with the ”--alg *by_order*” option is used to select the sampling-based method algorithm.

Sometimes even the sampling based method can not achieve a satisfactory accuracy or the user does not know whether the reduced system is accurate enough or not. In these cases, UiMOR provides the accuracy guaranteed algorithm: the adaptive sampling -based method (the adaptive method for short). The user only needs to provide the frequency range and the allowed maximum error (usually the default value of 0.1 is satisfactory, which means 10% relative error for the entire specified frequency range). Then, the number of sample points, the positions of sample points, and the order of the reduced system are determined by UiMOR automatically. The ”-m *analog*” option along with ”--alg *adaptive*” is used to indicate the adaptive algorithm. Although this option is the most time consuming and requires the most memory, model reduction only needs to be done once so it is still acceptable for demanding applications.

Table 1 summarizes the properties of the three algorithms.

2.3 Structure-preserving reduction

The original structures of the circuit matrices contain much important information such as passivity, reciprocal, sparsity, etc. Projection based reduction may destroy the structure related properties of the circuit matrices therefore it is important to keep the structure and structure related properties for projection based reduction algorithms. Preserving structure also helps realize the reduced circuits back into topology-based circuit netlists. In UiMOR, we implement the structure preserving reduction techniques developed in MSLAB [10, 25, 18].

2.4 Reduced system optimization

The reduced system matrices are generally dense, which makes the simulation of the reduced systems less desirable even though the order of the system has been reduced. A dense $\hat{G}$ matrix means each node of the reduced circuit has a resistive coupling between any two nodes. The same thing is true of the $\hat{C}$ matrix. If we realize this dense reduced system into a SPICE netlist, we may only observe limited simulation speedup compared with the original sparse system. In order to solve this problem, UiMOR further optimizes the reduced dense matrices into sparse ones and generates a sparse reduced circuit without accuracy loss.

3. THE MAJOR STEPS IN UIMOR

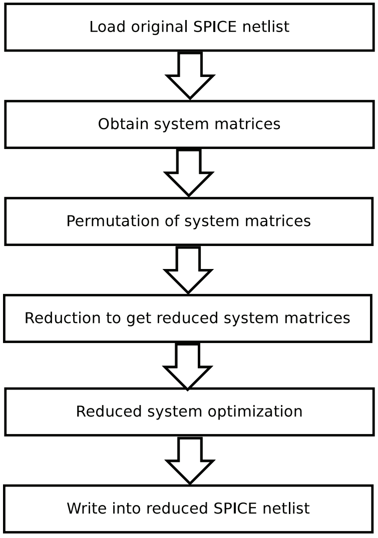

Figure 1: The flow of UiMOR

The main computing steps of UiMOR are summarized in Figure 1. First, the SPICE compatible circuit netlist is read in and the system matrices (G, C, B) are obtained. Next, row and column permutations of the system matrices are performed in order to preserve the matrix structure after reduction. Then, UiMOR reduces the permuted system into the structure-preserving reduced system. Several reduction algorithms are provided such as the the Krylov-subspace method, a sampling based method, and an adaptive sampling method. Users can choose one of these algorithms to trade-off accuracy and speed. Finally, the structure-preserved reduced system is further optimized and realized into a SPICE netlist.

During the reduction, all the ports driven by independent current and voltage sources will be automatically preserved and reproduced in the realized circuit for easy integration of the reduced models into the whole circuit system.

Also since we apply the structure-preserved reduction, the stability and passivity of the reduced system is preserved. Sometime numerical errors may still cause stability and passivity issues. Our model optimization techniques will further enhance and enforce the stability and passibility of the reduced models.

4. EXPERIMENTAL RESULTS

In the section, we present some numerical comparison results of UiMOR to show advantage of UiMOR over an existing commercial tool. Both RC and RLC circuits are used for the test. We use commercial tool Cadence UltraSim (version 7.0.0.073, 2007) [1] for the comparison as UltraSim has some built-in reduction capability. Hspice simulation results of the original systems are used as the golden standard for accuracy.

We first demonstrate the performance of UiMOR on a RC circuit which has 278801 elements and 119605 nodes. Table 2 shows the simulation time and memory cost for both UiMOR and UltraSim. For UiMOR, we use the simplest Krylov-subspace algorithm and a very low order 6 is set. The reduced circuit has 32 nodes (versus 11906 nodes in the original circuit). Compared to the two settings of UltraSim, UiMOR is better for both simulation time and memory cost.

Table 2: Simulation time and memory comparison for the RC circuit case.

Tool	Setting	Elem #	Time (s)	Memory (Mb)
UiMOR	Krylov,order=6	153	1.15	15.1
UltraSim	postl=1	70872	27.8	73.7
UltraSim	postl=2	4861	12.9	73.7

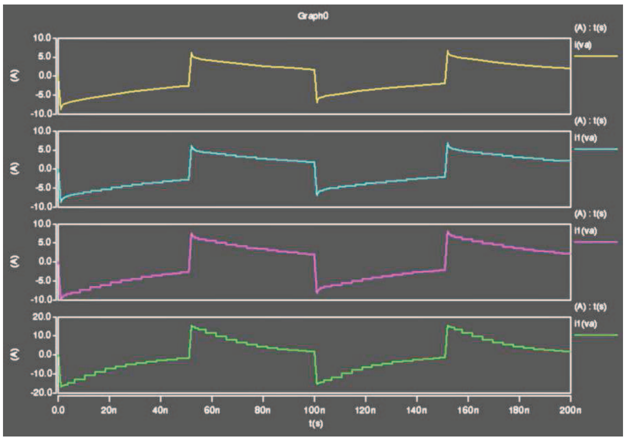

Figure 2: Comparison with UltraSim on a RC circuit. From up to down, there are Hspice, UiMOR, UltraSim postl=1, UltraSim postl=2.

Figure 2 shows the accuracy performance. A periodic square wave is used as the input signal and Hspice simulation result of the original circuit is used as the standard. With order 6, UiMOR has exactly the same result as Hspice. UltraSim postl=1 has a little difference with the standard while UltraSim postl=2, which means more aggressive reduction, generates relatively large error.

The next example is a RLC circuit with 89201 elements and 69404 nodes. Table 3 shows the simulation time and memory cost. The reduced circuit has 416 nodes. Compared to RC circuits, RLC circuits usually have spiky frequency responses and are harder to be reduced. As a result, sampling based algorithm, which has better global accuracy is used. For this RLC example, UiMOR with the order of 200 is still faster and more memory efficient than UltraSim. It is noted that UltraSim fails if postl=1 was set. The accuracy performance is shown in Figure 3. In this case, both UiMOR and UltraSim have similar results and match standard Hspice simulation result very well.

5. CONCLUSION

In this paper, we have introduced a new circuit complexity reduction tool – *UiMOR*. UiMOR is a stand-alone reduction tool and fits seamlessly with the existing post-layout verification flows in VLSI circuit and system design. UiMOR accepts standard SPICE netlists and produces reduced circuits also in standard SPICE format for easy integration with other tools. It offers wide-band reduction for both digital circuits and analog/mixed-signal/RF circuits. It is extremely efficient for RC circuits and can achieve 10-100× reduction ratio with very little accuracy loss. UiMOR is very scalable and efficient for reducing massive parasitic interconnect circuits and compare very favorably with the reduction function in commercial simulation tool.

6. REFERENCES

Table 3: Simulation time and memory comparison for the RLC circuit case.

Tool	Setting	Element #	Time (s)	Memory (Mb)
UiMOR	Sampling TBR, order=200	42840	9.63	32.7
UltraSim	postl=0	89201	21.2	92.0
UltraSim	postl=1	N/A	N/A	N/A

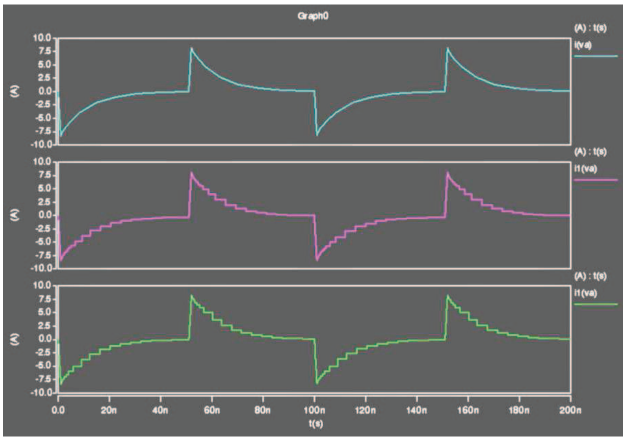

Figure 3: Comparison with UltraSim on a RLC circuit. From up to down, there are Hspice, UiMOR, UltraSim postl=0.

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