Mesh optimization Methodology for the Early-stage Design of On-chip Power/Ground (P/G) Networks

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Abstract— *Owing to roaring current density, the worst-case IR drop of on-chip P/G grids becomes another style of the power constraint on floor-planning. Thus, it is very important to efficiently minimize the worst-case IR drop with the definite percentage of routing resource in early-stage P/G network design. In this paper, we propose a practical optimization method that uses ICCG algorithm to obtain the exact optimal solution for P/G meshes. In order to replace time-consuming ICCG algorithm for shortening optimization process, we give out a novel approach, named as ACD, to efficiently analyze P/G networks and certainly to speedup the optimization. Last, we present a theoretic method to directly calculate the optimal solution for fastest optimization. Shown with experimental data, the optimization methods construct single-peak solution spaces and the peaks are close so that designers can efficiently obtain the practical optimal solution based on the theoretic counterpart.*

1. Introduction

With technology scaling into nano-regime, power becomes one important design constraint as well as performance and area [1-2]. In many scenarios such as mobile applications, power is the first design constraint. Therefore, any solution of floor- planning should satisfy the power constraint [3]. Additionally, there are two indirect constraints both linked to the power consumption. One is thermal constraint [3] and another is the worst-case IR droop constraint of On-die P/G networks.

Because P/G network, clock network and general signal network compete each other in the distribution of chip routing resource [2-6], designers usually assign definite percentages of whole chip routing resource among them in floor-planning. Although there are some constraints, the main object of floor-planning is still the minimum die area [3]. In the optimization process of floor-planning, the area-saving solution increases the current density and decreases the routing resource for On-die P/G networks. As the result, the IR droop of the P/G network keeps in monotonic increase during floor-planning.

In order to guarantee the work voltage of transistors, V_{wst}, the worst-case IR droop of On-die P/G network, should be kept in a limitation with the definite percentage of chip routing resource. Thus, it is imperative for us to minimize V_{wst} of early-stage P/G network subject to the definite percentage of chip routing resource. Since floor-planning process produces much more solutions for choosing the optimal and each solution has its own P/G network as well as its own die area and current density, it is very important to find an efficient optimization algorithm for the early-stage On-die P/G network design.

Up to now, many scholars propose some methods [4-10] to optimize On-die P/G networks. Among them, [4-6] propose approaches to optimize DC P/G networks through wire sizing, [7-8] give out approaches to optimize transient P/G networks with decap budgeting, and [9] presents an unique approach to optimize transient P/G networks through simultaneous wire sizing and decap budgeting. Methods [4-8] are feasible to optimize P/G networks at routing stage while some work need be done to put the approach [9] into use. But these methods [4-9] are infeasible to optimize early-stage P/G networks because floor-planning need further more efficient optimization algorithms. Recently, paper [10] proposes a theoretical method to efficient optimize double-mesh based P/G networks at floor-planning stage. Unfortunately, it is infeasible due to an assumption that all lines in a same mesh are of equal width. Paper [11] shows that all lines linked to PADs or vias are wider than other lines.

In this paper, we propose a novel method to efficiently optimize early-stage P/G networks supplied by C4-PAD array [11] through sizing the width ratio between lines linked to PADs and other lines. For modern chips, On-die P/G networks are composed of two layer networks, upper layer networks are pure meshes and lower layer ones are of different topologies including tree[4], chain[7-8] and mesh [9-10]. Thus, in this paper, we only focus our research on single P/G meshes and in future, we will expend our research to double-layer P/G networks. First, we uses ICCG algorithm [6] to optimize P/G networks for exact optimal solutions S-ICCG though it is inefficient owing to more time consuming. Then, we propose a novel simulation algorithm, approximate currents distribution (ACD) algorithm to efficiently obtain the approximate optimal solutions S-ACD with slight accuracy loss. Last, based on ACD algorithm, we find a theoretical method to directly calculate the approximate optimal solutions S-THR. Experiments demonstrate that triple solutions obtained by above methods are very close while S-ICCG and S-ACD searching spaces are single-peak. At the same time, we can fast obtain S-ICCG and S-ACD from S-THR so that our methodology is very suitable to efficiently optimize early-stage P/G grids as well as to fast check whether a floor-planning solution breaks the IR droop constraint.

This paper is organized as follows. We first formulate the optimization problem in section 2. Then, section 3 presents the method to use ICCG to get S-ICCG. And section 4 proposes the ACD simulation algorithm and the method to obtain S-ACD. The method to compute S-THR is described in section 5. Section 6 concludes the paper.

2. Problem Formulation

In the floor-planning stage, the k^{th} floor-planning solution for a chip of total current I_0 is of area A^k, which means the current density is I_0 / A^k because current uniform distribution is also one constraint of floor-planning [3]. As for early-stage P/G networks supplied by PAD array, because total current I_0 is the definite value, N_{PAD}, the number of PADs, can be computed with the maximum assigned current I_{pmax} of one PAD.

$$N_{PAD} = ceiling(I_0 \div I_{p\max}) \qquad (1)$$

where the *ceiling* function is to assign the integer more than the viable.

Assume the chip is square. Then, N_2, the number of PADs in a row or column, can be computed as following:

$$N_2 = ceiling\left((N_{PAD})^{0.5}\right) \quad (2)$$

Assume the minimum Pitch is l_{pt}. Then, N_{line}, the number of rows or columns for k^{th} floor-planning solution, can be computed as follows:

$$N_{line} = bound\left\{\left(A^k\right)^{0.5} \div l_{pt}\right\} \quad (3)$$

where the *bound* function is to assign the integer less than the viable. Then, N_1, the number of lines between two adjacent PADs (includes two lines linked to two PADs), can be computed as follows:

$$N_1 = bound\{N_{line} \div (N_2 - 1) + 1\} \quad (4)$$

Assume all currents are connected to the cross nodes of P/G networks. As the result, we can compute I_{node}, the current absorbed from one cross node of uniform-current-distribution P/G networks, as

$$I_{node} = I_0 \div \{(N_2 - 1) \times (N_1 - 1) + 1\} \quad (5)$$

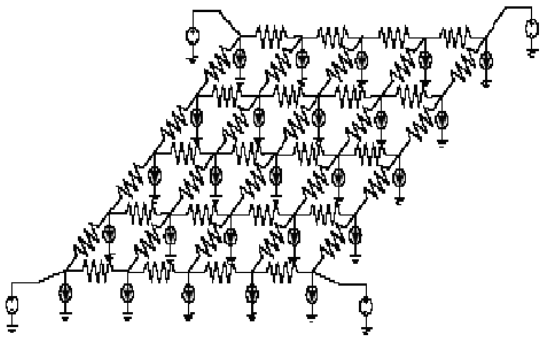


Figure 1: Circuit model for the single-level power mesh.

As for the k^{th} floor-planning solution, its total routing resource is $R_{rt} \times A^k$ where R_{rt} is the definite ratio between routing resource and die area. And the routing area of the P/G grid is $R_{pg} \times R_{rt} \times A^k$ where R_{pg} is the definite percentage of the total routing resource. With the routing area of $R_{pg} \times R_{rt} \times A^k$, we can design an initial P/G network whose lines are of the same width. Based on the initial P/G network, we minimize the worst-case IR drop through sizing α, the width ratio between lines linked to PADs and other lines unlinked. Thus, we formulate the early-stage P/G network optimization as follows:

$$\min\{V_{wst} = f(\alpha)\},$$
$$\{(N_2 - 1)(N_1 - 1) + 1 - N_2\} \times w + N_2 \times \alpha \times w = 0.5 R_{pg} \times R_{rt} \times A^k \quad (6)$$

where w is the width of lines unlinked to PADs.

3. Using ICCG to get S-ICCG

In this section, we use ICCG algorithm to find the optimal ratio α_{opt} between lines linked to PADs and other lines unlinked for a given routing area. Among simulation approaches [4][6][12-15], ICCG algorithm is more efficient for accurately calculating currents and voltages in VLSI power supply networks. For each ratio, we can calculate V_{wst} and then we can pursue the minimum. Experiments demonstrate that V_{wst} is a single peak function about the ratio α. Therefore, we can use 1-dimension searching method such as the Golden-Section-Search method to get the optimal solution α_{opt}.

In the following parts, we induce another parameter to replace α for simplicity. For a P/G grid, the number of nodes in the typical area surrounded by four power PADs is $N_1 \times N_1$, and the number of the C4 power PADs is $N_2 \times N_2$. The voltage of the C4 power pad is V_{dd}, the total current drained from each PAD is $I_{pad} = I_0 \div (N_2)^2$.

We first consider the situation when all wires are of the same width w_0. The resistance between two neighbor nodes is R_0 for all segments. As we change α, the width of the coarser wire becomes $\beta \times w_0$, and the width of the fine wire is $\gamma \times w_0$. In order to keep the total routing area the same, β and γ should satisfy this relation:

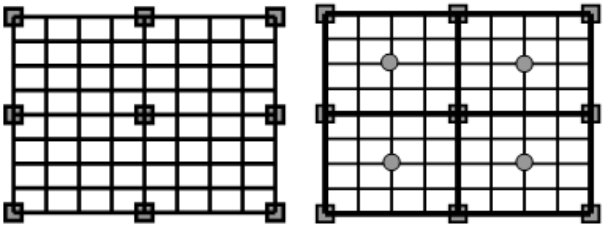
$$N_1 - 1 = \beta + \gamma(N_1 - 2)$$

or
$$\gamma = \frac{N_1 - 1 - \beta}{N_1 - 2} \quad (7)$$

and $\alpha = \beta \div \gamma = \beta \times (N_1\text{-}2) \div (N_1\text{-}1\text{-}\beta)$. (8)

The resistances of the coarse segment and the fine segment change to $R_0 \div \beta$ and $R_0 \div \gamma$, respectively. And with EQ(8), the formulation about the early-stage P/G network optimization can be transformed from EQ(6) to EQ(9), which means that β replaces α as the optimization variable.

$$\min\{V = f(\beta)\},$$
$$\{(N_2 - 1)(N_1 - 1) + 1 - N_2\} \times \beta + N_2 \times \frac{N_1 - 1 - \beta}{N_1 - 2} = 0.5 R_{pg} \times R_{rt} \times A^k \div w_0 \quad (9)$$



(*a*) All wires are the same. (*b*)Wires between pads are coarser.

Figure 2: An example of changing width. N_1=5, N_2=3. The circular nodes in (*b*) are the worst-case IR-drop nodes.

Because early-stage P/G networks are linear R-only circuits, we can easily prove that the optimal solution β_{opt} is independent on V_{dd}, I_{node}, R_0. So in following experiments, similar to [10], we assign that V_{dd} = 2.0V, I_{pad} = 1.0A, and R_0 = 1.0Ω.

3.1 Optimal results with different N_2

As N_2 becomes large, the mesh can be considered as an infinite resistive plain, and the optimal ratio β_{opt} will come to a definite value. We let N_1=10, and change N_2. From table.1, we can see results agree to the above analysis. In the following experiment, we let N_2=20.

Table 1: The optimal ratio of coarser and finer wires with different N_2

N_2	β_{opt}
5	4.141845
6	4.171778
7	4.174862
10	4.177498
15	4.177571
20	4.177556

3.2 S-ICCG with different N_1

When N_1 changes, we first get initial worst-case IR-drop when all the segments have the same width using ICCG algorithm. Then we change the width of segments, get the optimal solution S-ICCG including the worst-case IR-drop and ratio β_{opt}. Table 2 gives the results as N_1 changes while N_2=20.

Shown in table 2, as N_1 increases, the optimal V_{wst} changes small around a value but the initial V_{wst} increases rapidly. The optimal V_{wst} is much better than the initial one, which means the approach in [10] is

infeasible because it assumes that all wire in the same layer mesh are of the same width. Another interesting thing is that the optimal V_{wst} becomes slightly smaller as N_1 is even than as N_1 is odd. Because V_{wst} occurs at the central of four C4 power pad, as N_1 is even, there is no central node but a central square. The optimal β_{opt} increases as N_1 increases. We fit the data with least square method and get correlation coefficient r=0.999799. It is so close to 1 that β_{opt} is linear to N_1.

Table 2: The initial and optimal worst-case IR-drop, β_{opt}, and the time consuming by ICCG algorithm.

$N1$	Initial V_{wst} (mV)	Optimal V_{wst} (mV)	Error (mV)	β_{opt}	Time Consuming (s)
5	333.30	240.40	92.9	2.107	10.344
6	359.93	233.00	126.93	2.564	23.454
7	392.75	241.74	151.01	2.931	57.473
8	413.51	237.80	175.71	3.371	84.371
9	436.79	242.23	194.56	3.747	133.752
10	453.44	239.80	213.64	4.177	177.836
11	471.73	242.46	229.27	4.558	259.513

4 Optimize with ACD simulation algorithm

ICCG algorithm can get exact optimization solutions because it can accurately calculate the voltages of all nodes. But as the scale of the mesh increases, the run-time increased rapidly. Thus, it is too slow to optimize early-stage P/G networks of large scale for so much floor-planning solutions. Thus, we need a far more effective algorithm. In this paper, we propose the approximate current distribution (ACD) algorithm for efficient analysis and optimization of early-stage P/G networks.

ACD algorithm does not calculate the voltages directly. It first gets an estimation of current distribution and then, uses the current distribution to directly calculate the worst-case IR-drop. Thanks the current uniform distribution of ear-stage P/G networks, the ACD is accurate enough to obtain the S-ACD nearly around S-ICCG as shown in following parts.

4.1 ACD simulation algorithm

In ACD algorithm, we assume that the mesh is an infinite resistive grid and estimate the current distribution in a typical square area surrounded by four C4 PADs. The square can be divided to four sub-squares. According to symmetry, we only need to consider a sub-square.

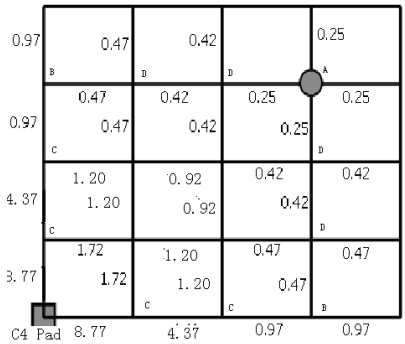


Figure 3: An example for simple estimation for a sub-square. A, B, C, D are typical nodes on the border lines.

Now, we describe how to distribute all currents in the square. Because PADs are the only current providers to the P/G network of the uniform absorption-current distribution, currents always flow from nodes near to PADs to the far-away neighbors in each sub-square. But for border nodes of sub-square, there are following special regulations on how to supply current. Figure 3 shows the detail current distribution in a sub-square of current-even-distribution P/G grids.

A. The node that is the center of four C4 PADs, gets current evenly from four neighbors.
B. The node that is the center of vertical or horizontal lines linking two C4 pads, currents evenly flow in from two neighbors on the line linking two C4 pads and then, evenly flow out to other two neighbors.
C. The nodes locating on border lines of squares, except in B cases, currents flow into the nodes from the neighbor near to a C4 pad and then, flow out to other three neighbors.
D. The nodes locating on border lines of sub-squares, except nodes in A and B case, currents flow into the nodes from three neighbors near to the C4 pads of two sub-squares and then, flow out to the far-end neighbors.

With the current distribution, we can calculate the worst-case IR-drop quickly. But another question arises because we can get different IR-drop from different ways. So we calculate V_{diag}, the IR-drop along the diagonal line, which is smallest while V_{bord}, the IR-drop along borders, which is largest. Then, we regard the average value as the worst-case IR-drop.

$$V_{wst}= (V_{diag}+V_{bord})\div 2. \qquad (10)$$

As β changes, we do not change the current distribution and only change the resistances of the mesh. Thus, we can directly calculate the V_{wst} according to the resistances of the mesh.

4.2 S-ACD with different N_1

With the ACD simulation algorithm, the only parameter we need to consider is N_1, the number of nodes between two neighbor PADs. We change N_1 to get the optimal solution S-ACD including V_{wst} and β_{opt}. Then, we compare S-ACD with S-ICCG (listed in Table.2) gotten with ICCG algorithm.

Table 3: the optimal solutions S-ACD obtained with ACD algorithm

$N1$	V_{wst} (mV)	V_{wst} Error (mV)	β_{opt}	β_{opt} error (%)
5	236.26	-4.14	2.109801	0.002532
7	234.98	-6.76	2.845255	-0.085893
9	233.91	-8.32	3.538974	-0.207645
11	233.15	-9.31	4.208975	-0.348752
13	232.63	-9.96	4.863712	-0.502465
15	232.29	-10.39	5.507664	-0.665295

The error of V_{wst} is less than 5% while the error of β_{opt} is less than 12%. Shown in Fig.4 in next page, V_{wst} of S-ICCG changes slow around the β_{opt} of S-ICCG. Thus, V_{wst} of S-ACD is very close to the exact one though β_{opt} of S-ACD is not good enough. But the ACD simulation algorithm is much faster than ICCG algorithm. In fact, we can first use the ACD algorithm to get an approximation β_{opt} of S-ACD, then use ICCG algorithm to get the accurate value.

4.3 S-THR Based on ACD algorithm

For the ACD algorithm, the current distribution does not change while the ways we choose to calculate V_{wst} do not change, too. So the sums of currents on coarser and finer wires also do not change. We indicate them as I_c and I_f. According to EQ(10), we get the following equation.

$$V_{wst} = \left(\frac{I_c}{\beta} + \frac{I_f}{\gamma}\right) \times R_0 = \left(\frac{I_c}{\beta} + \frac{I_f (N_1 - 2)}{N_1 - 1 - \beta}\right) \times R_0 \qquad (11)$$

We set the derivation of V_{wst} to zero:

$$\frac{\partial V_{wst}}{\partial \beta} = \left(-\frac{I_c}{\beta^2} + \frac{I_f (N_1 - 2)}{(N_1 - 1 - \beta)^2}\right) \times R_0 = 0 \qquad (12)$$

Then we get the optimal ratio β_{opt}:

$$\beta_{opt} = \frac{N_1 - 1}{\sqrt{\frac{I_f (N_1 - 2)}{I_c}}} \qquad (13)$$

Once we get the current distribution, we do not need to search for the optimal solution S-ACD including β_{opt}, but can directly calculate it named as S-THR. Table 4 shows that S-THR is so closed to S-ACD that we can directly regard S-THR as S-ACD.

Table 4: The calculated S-THR compared with S-ACD.

N1	β_{opt} calculated	error
5	2.11022	0.0004
7	2.84566	0.0004
9	3.53921	0.0002
11	4.20930	0.0003
13	4.86411	0.0004
15	5.50813	0.0005

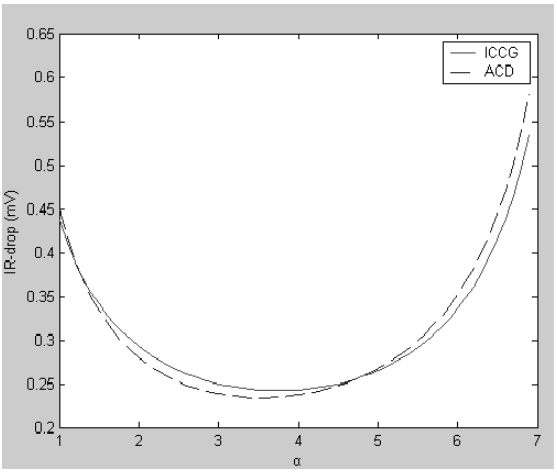


Figure 4: The image of function V(β) using ICCG algorithm and ACD algorithm when N_1=9, N_2=20.

4.4 Usage of Our Method in Floor-planning

Because the uniform power distribution is the constraint of floor-planning, the current distribution of early-stage P/G network is regarded as totally uniform. For each solution of floor-planning, out method can efficiently calculate the V_{wst} of the S-THR and fast check if the solution breaks the constraint of the worst-case IR droop.

Furthermore, for huge P/G networks of nearly uniform current distribution, our ACM algorithm can fast calculate the worst-case IR droop.

5.Conclusion and Future Work

In this paper, we have discussed worst-case IR-drops on single uniform-current-distribution meshes. We use the ICCG algorithm to optimize the widths of the mesh and propose a new algorithm to improve the efficiency. By these algorithms, we can optimize a single mesh quickly and get the worst-case IR-drop. It is suitable to check whether a floor-planning solution breaks the IR droop constraint.

Further research directions may include: (1) Optimizing early-stage P/G networks of two layers. (2) Optimizing P/G networks of nearly uniform current distribution.

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