

# EQUADI: A Linear Complexity Algorithm on

## Transient Power/Ground(P/G) Network Analysis for ASICs

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**Abstract**— *This paper presents a hybrid algorithm on P/G networks of Mesh+Tree topology for ASICs. Based on existing algorithms, equivalent circuit method and TLM-ADI method, our algorithm is of linear complexity to solve P/G networks of Mesh+Tree topology. First, it uses equivalent circuit approach to compress the Mesh+Tree P/G circuit into the circuit only of Mesh topology, which is a linear complexity and error-free process. Then, it uses the TLM-ADI approach to linearly solve the reduction circuit of Mesh topology. Last, once the reduction circuit is solved, it can back-solve all leaves nodes from the base nodes of trees, which is linear complexity. Experiments show that our method is indeed linear complexity to analyze P/G networks of Mesh+Tree topology for ASICs while it speeds up two magnitudes over HSPICE.*

### 1. Introduction

As technology scales into nanometer regime [1], accompanying with soaring frequency and power consumption, IC chips need large and complex power/ground grids, which makes design and verification of P/G networks become challenging [2]. Driven by marketing strategy, most of chips are ASICs that usually utilize Mesh+Tree topology for their P/G grids due to the reliability as well as the flexibility. This kind of P/G networks utilizes mesh topology of the coarse grid on upper levels for the reliability while the tree topology of the fine grid on lower levels for the flexibility. So it is imperative to find the algorithm that can efficiently analyze huge P/G networks of Mesh+Tree topology [14][15].

As P/G grids of Mesh+Tree topology experience the huge current flows in high-end ASIC chips, they are more susceptible to current-induced reliability and functional failures due to excessive IR drops,  $Ldi/dt$  noise, electro-migration and resonance effects. Increasing parasitics due to rising frequency and continuing pushing for more device integrations lead to exponential complexity growth of pos-layout P/G networks. As a result, very scalable transient analysis techniques of P/G grids are required to capture the increasing dynamic voltage fluctuations for guiding the design of robust P/G grids. But the traditional circuit simulators methods like SPICE are no longer able to meet the formidable tasks of analyzing P/G circuits with millions of extracted RLCK elements in a timely manner.

Driven by the increasing importance of P/G integrity, many efficient linear circuit simulation techniques have been proposed for fast P/G grid analysis in the past. Those methods include the model reduction based method [3][5][15], the hierarchical and macro-modeling based method [4][5], subspace projection based approach [6], iterative approaches such as preconditioned conjugate gradient method (PCG)[7], multi-grid methods [8][9], the transmission-line-modeling alternating-direction-implicit method (TLM-ADI)[10], the random walk method [11], and node-reduction

based approaches [12][13][14][15].

Paper [15] is the first try to efficiently solve P/G networks of Mesh+Tree topology. But it uses such the complicated PRIME algorithm to compact trees that it becomes inefficient. As the result, it only speed up 10-20X times over HSPICE [15]. Paper [14] uses one efficient and error-free method, the equivalent circuit method, to compress trees and then to solve the reduction mesh circuit with the PCG algorithm. But the reduction mesh circuits of huge P/G grids are still so large that the method [14] becomes inefficient.

In order to find an efficient algorithm of linear complexity for huge P/G networks of Mesh+Tree topology, we induce the TLM-ADI method to deal with the reduction mesh circuits since the method is the algorithm of linear complexity [10]. In this paper, we do much more works to combine two methods from [14][15] into a more practical method, EQUADI, to solve huge P/G networks of Mesh+Tree topology in linear complexity. Experiments demonstrate that the EQUADI method solves the test cases indeed in  $O(N)$  complexity so that it can deal with huge P/G grids.

The remainder of the paper is organized as follows. Section 2 describes the Mesh+Tree topology for P/G grids of ASICs. In section 3, the approximate modeling is introduced to transform RLC circuits to R-only circuits for the static analysis. Section 4 presents the EQUADI method and its algorithm analysis. Experimental results are collected to validate the method in section 5. And section 6 concludes the paper.

### 2. P/G grids of the Mesh+Tree topology

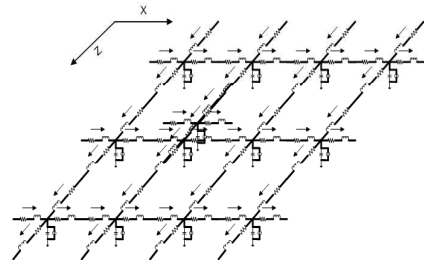


Figure.1 Mesh topology for coarse grids on upper levels

Shown in Fig.1, the mesh topology provides 4 connection degrees for each node so that it can guarantee the reliability for power delivery. As the coarse network on upper levels delivers larger and larger currents from PADs to the fine network, designers must consider the electro-migration (EM) effect of copper caused by the large current density. Thus, they choose the mesh topology to ensure the reliability of the coarse network on upper levels.

On the other hand, the fine network on lower levels experiences the little current density, which in turn, decreases the EM effect. Therefore, designers choose the tree topology for the fine network on lower levels in order to shorten the ASIC design cycle since the tree

topology is the most flexible among all candidates.

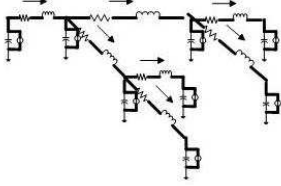


Figure.2 Tree topology for fine grids on lower levels

### 3. Approximate Modeling for Static Circuit Analysis

It is difficult to directly simulate RLC circuit because it may induce additional nodes as [10] and can't compress trees as [14]. In order to transform RLC circuits into R-only circuits for the static circuit analysis, we must use the trapezoid approximation method and the Norton equivalent theory to simplify P/G circuits as follows.

Let  $h$  be the time step used at simulation step  $k+1$ . For the capacitors and inductors, trapezoidal companion models of Norton's form are used. In this way, we will not introduce any extra nodes. Specifically, the current across a capacitor at step  $k+1$  is:

$$I_{c,k+1} = \frac{2C}{h}V_{c,k+1} - \left(\frac{2C}{h}V_{c,k} + I_{c,k}\right), \quad (1)$$

where  $V_{c,k}$ ,  $I_{c,k}$ ,  $V_{c,k+1}$ ,  $I_{c,k+1}$  denote, respectively, the branch voltages and branch currents of the capacitor at step  $k$  and step  $k+1$  respectively and  $C$  is the value of the capacitor. Similarly the current through an inductor at step  $k+1$  is:

$$I_{L,k+1} = \frac{h}{2L}V_{L,k+1} + \left(\frac{h}{2L}V_{L,k} + I_{L,k}\right), \quad (2)$$

where  $V_{L,k}$ ,  $I_{L,k}$ ,  $V_{L,k+1}$ ,  $I_{L,k+1}$  denote, respectively, the branch voltages and branch currents of the inductor at step  $k$  and step  $k+1$  and  $L$  is the value of the inductor.

Because a segment of P/G grid includes a resistor and an inductor, there are two floating resistors and one floating current source in the segment after the trapezoidal transformation for an inductor. Thus, we merge two floating resistors for each RLC section as shown in Fig. 3 using Norton theory. Then we have:

$$R_i^* = 2L_i/h + R_i, \quad (3)$$

$$e_{l_{i,k+1}} = \left(\frac{h}{2L_i}V_{L_{i,k}} + I_{L_{i,k}}\right) \cdot \frac{2L_i/h}{2L_i/h + R_i}, \quad (4)$$

where  $V_{L_{i,k}}$  and  $I_{L_{i,k}}$  are the branch voltage and branch current of  $L_i$  at step  $k$ . They can be represented with node voltages and branch currents.

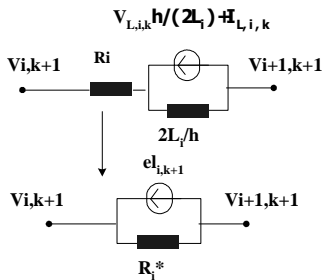


Figure 3. Merge two resistors in a RLC section.

We then combine two grounded current sources, one is coming from the independent current source and another is coming from capacitor's companion model, into one current source  $ec_{i,k+1}$  for each RLC section:

$$ec_{i,k+1} = e_{i,k+1} - \left(\frac{2C_i}{h}V_{i,k} + I_{i,k}\right), \quad (5)$$

and rename the equivalent resistor from  $C_i$ 's companion model as  $r_i = h/2C_i$ . As a result, RLC circuits in Fig. 1 and Fig. 2 can be simplified to the resistor-only circuits for the static analysis.

In rest of the paper, the symbol  $\left|^{k+1}\right.$  is used to mark variables at  $k+1$  step. For instance,  $V_{i,j}^{k+1}$ ,  $e_{i,j}^{k+1}$  mean the voltage of node  $(i,j)$  and the absorbing current source connected to  $(i,j)$  at the  $k+1$ th step.

### 4. The EQUADI method

In this section, we describe equivalent circuit method and TLM-ADI method for tree compression and mesh analysis in two sub-sections. And then, the algorithm is presented.

#### 4.1 Equivalent Circuit Model for Tree Simulation

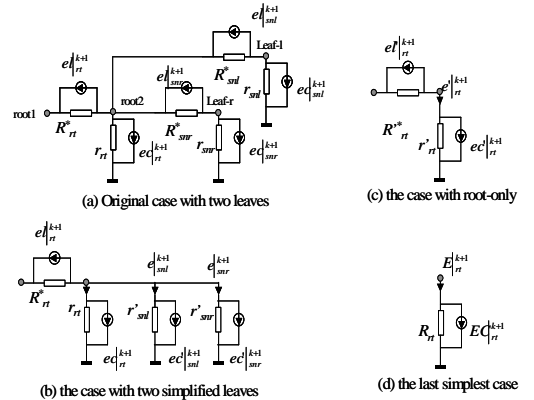


Figure.4 Tree Compression Procedure

After the approximation process described in above section, RLC trees can be transformed into the R-only trees shown in Fig.4(a). The approach in [14] uses Norton theory to error-free compress trees into only base nodes remained as shown in Fig.4. And the P/G circuit of Mesh+Tree topology is compressed into the small circuit of pure mesh topology shown in Fig.5. Once the reduction circuit is solved, the counter-procedure of Fig.4 is operated to back-solve leaves' voltage from the base nodes.

The approach in [14] uses PCG algorithm to solve the remainder mesh circuit. If the mesh circuit is large enough, the inefficiency of PCG algorithm may cause the inefficiency of the approach, which means the approach can't deal with huge P/G circuits for high-end ASIC application. In the following subsection, we propose a novel ADI method to efficiently solve the R-only meshes shown in Fig.5.

#### 4.2 ADI Method for Mesh Simulation

The TLM-ADI approach [10] can directly deal with RLC meshes but can't solve the static meshes obtained in above subsection. In

following, we propose a novel digital ADI method based on the basic TLM-ADI theory. Our digital ADI method consists of two steps: the horizontal implication operation at the  $k+0.5^{th}$  step and the vertical implication operation at the  $k+1.5^{th}$  step.

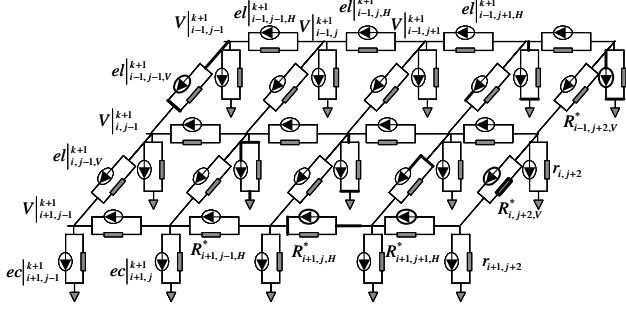


Figure.5 Static Mesh Circuit for ADI Method

Shown in Fig.5,  $r_{i,j}, R_{i,j,H}^*, R_{i-1,j,H}^*, el_{i,j,V}^{k+1}, el_{i,j,H}^{k+1}, ec_{i,j}^{k+1}$  are the

known equivalent values for the reduction circuit of pure mesh.

For the static mesh circuit, the horizontal implication operation at the  $k+0.5^{th}$  step uses  $k+1^{th}$  currents for horizontal branches and  $k^{th}$  currents for vertical branches to formulate the following equation according to KCL law.

$$V_{i,j}^{k+0.5} \div r_{i,j} + ec_{i,j}^{k+0.5} = \delta_H |_{i,j}^{k+1} + \delta_V |_{i,j}^k \quad (6)$$

where  $V_{i,j}^{k+0.5}, ec_{i,j}^{k+0.5}$  are the voltage of node  $(i,j)$  and the equivalent

current linked to the node at  $k+0.5^{th}$  step. Meanwhile  $\delta_H |_{i,j}^{k+1}, \delta_V |_{i,j}^k$

are two current differences between two branches in horizontal direction at the  $k+1^{th}$  step and between two branches in vertical direction at the  $k^{th}$  step.

As the values at the  $k^{th}$  step are known, we only need to compute the values at the  $k+0.5^{th}$  step and the  $k+1^{th}$  step as follows.

$$\begin{aligned} V_{i,j}^{k+0.5} \div r_{i,j} + ec_{i,j}^{k+0.5} &= 0.5V_{i,j}^{k+1} \div r_{i,j} + 0.5V_{i,j}^k \div r_{i,j} + 0.5(ec_{i,j}^k + ec_{i,j}^{k+1}) \\ &= 0.5g_{i,j}V_{i,j}^{k+1} + 0.5(g_{i,j}V_{i,j}^k + ec_{i,j}^k + ec_{i,j}^{k+1}) \end{aligned} \quad (7)$$

$$\begin{aligned} \delta_H |_{i,j}^{k+1} &= I_H |_{i,j}^{k+1} - I_H |_{i-1,j}^{k+1} \\ &= \left[ (V_{i,j}^{k+1} - V_{i,j}^{k+1}) \div R_{i,j,H}^* + el_{i,j,H}^{k+1} \right] - \left[ (V_{i,j}^{k+1} - V_{i-1,j}^{k+1}) \div R_{i-1,j,H}^* + el_{i-1,j,H}^{k+1} \right] \\ &= G_{i,j,H}^* V_{i+1,j}^{k+1} - (G_{i,j,H}^* + G_{i-1,j,H}^*) V_{i,j}^{k+1} + G_{i-1,j,H}^* V_{i-1,j}^{k+1} + (el_{i,j,H}^{k+1} - el_{i-1,j,H}^{k+1}) \end{aligned} \quad (8)$$

where  $g_{i,j}, G_{i,j,H}^*, G_{i-1,j,H}^*$  are the conductance corresponding to the resistors  $r_{i,j}, R_{i,j,H}^*, R_{i-1,j,H}^*$  shown in Fig.5.

With EQ(7) and EQ(8), EQ(6) can be transformed into EQ(9).

$$\begin{aligned} 0.5g_{i,j}V_{i,j}^{k+1} + 0.5(g_{i,j}V_{i,j}^k + ec_{i,j}^k + ec_{i,j}^{k+1}) &= \delta_V |_{i,j}^k + \\ G_{i,j,H}^* V_{i+1,j}^{k+1} - (G_{i,j,H}^* + G_{i-1,j,H}^*) V_{i,j}^{k+1} &+ G_{i-1,j,H}^* V_{i-1,j}^{k+1} + (el_{i,j,H}^{k+1} - el_{i-1,j,H}^{k+1}) \end{aligned} \quad (9)$$

Then, EQ(9) can be simplified into the following equation.

$$\begin{aligned} -G_{i-1,j,H}^* V_{i-1,j}^{k+1} + (G_{i,j,H}^* + G_{i-1,j,H}^* + 0.5g_{i,j}) V_{i,j}^{k+1} - G_{i,j,H}^* V_{i+1,j}^{k+1} \\ = \delta_V |_{i,j}^k + (el_{i,j,H}^{k+1} - el_{i-1,j,H}^{k+1}) - 0.5(g_{i,j}V_{i,j}^k + ec_{i,j}^k + ec_{i,j}^{k+1}) \end{aligned} \quad (10)$$

The right term of EQ(10) is the known current while three left terms are unknown. With EQ(10), all nodes of each row compose of a tri-diagonal matrix that can be solved in linear complexity.

Then at the  $k+1.5^{th}$  step, the vertical implication operation can also be formulated into the following equation according to KCL law.

$$V_{i,j}^{k+1.5} \div r_{i,j} + ec_{i,j}^{k+1.5} = \delta_H |_{i,j}^{k+1} + \delta_V |_{i,j}^{k+2} \quad (11)$$

Similarly, EQ(11) can be transformed into the following equation. And all nodes of each column also compose of a tri-diagonal matrix so that they can be solved in linear complexity.

$$\begin{aligned} -G_{i,j-1,H}^* V_{i,j-1}^{k+2} + (G_{i,j,V}^* + G_{i,j-1,V}^* + 0.5g_{i,j}) V_{i,j}^{k+2} - G_{i,j,V}^* V_{i,j+1}^{k+2} \\ = \delta_H |_{i,j}^{k+1} + (el_{i,j,V}^{k+2} - el_{i,j-1,V}^{k+2}) - 0.5(g_{i,j}V_{i,j}^{k+1} + ec_{i,j}^{k+1} + ec_{i,j}^{k+2}) \end{aligned} \quad (12)$$

With EQ(10) and EQ(12), we propose the digital ADI method of the linear complexity to statically simulate the remained circuit of pure mesh topology shown in Fig.5.

### 4.3 The EQUADI Algorithm

Based on the above analyses, we propose the EQUADI algorithm to efficiently solve huge P/G networks of the Mesh+Tree topology for high-end ASIC applications in this subsection. The procedure of EQUADI is described as follows.

- 1) Equivalent parameters should be refreshed as described in section.3.
- 2) Equivalent circuit method is used to compress the Mesh+Tree circuit into the reduction circuit of the pure mesh topology as shown in subsection 4.1.
- 3) The digital ADI method in described subsection 4.2 is used to solve the reduction circuit in linear complexity.
- 4) Equivalent circuit method is used to back-solve all leaves of trees from base nodes planted on the mesh circuit as shown in subsection 4.1.

Because the complexities of all four steps are linear, the EQUADI algorithm is linear, too, which means the algorithm can deal huge P/G networks for high-end ASIC applications.

Paper [10] proves that ADI method is unconditionally stable. And we can easily prove that the trapezoidal approximation is unconditionally stable, too. Thus, EQUADI is also unconditionally stable.

Although the trapezoidal approximation is of the  $O(h^2)$  accuracy, the ADI method is only of the  $O(h)$  accuracy. Therefore, our method is also of the  $O(h)$  accuracy, which means we only shorten the time step  $h$  to increase the accuracy.

## 5. Experimental Results

The proposed simulation algorithm has been implemented in C++. All the experimental results are collected on a SUN V880 workstation with 750MHz Ultra Sparc CPU and 2GB memory. The number of time steps is assigned 120 for one clock cycle and VDD is 2.5V.

From above analyses, the EQUADI algorithm is of the linear complexity while it is unconditionally stable and  $O(h)$  accuracy. The following four figures are drawn to show the superiority of the

EQUADI algorithm from the viewpoint of experiment.

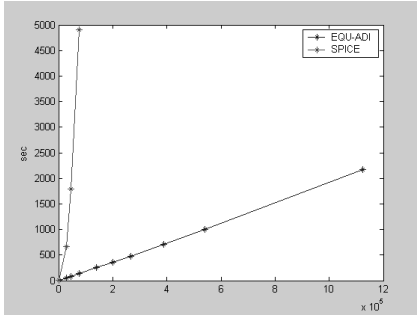


Figure.6 Time Complexity Comparison

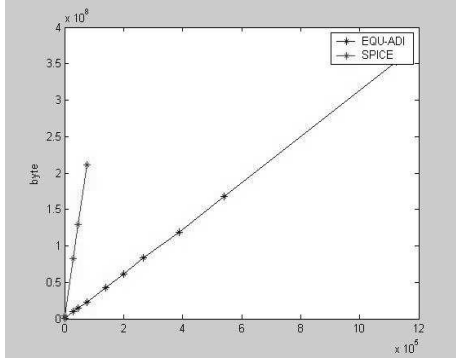


Figure.7 Memory Complexity Comparison

With comparisons with HSPICE in Fig.6 and Fig.7, we can see EQUADI is really a fast, efficient algorithm. And we can see the time and space complexity of the EQUADI algorithm are both  $O(n)$ .

With the DC transient response of EDU-ADI with different time steps in Figure.8, we can conclude the EQU-ADI algorithm is unconditional stable.

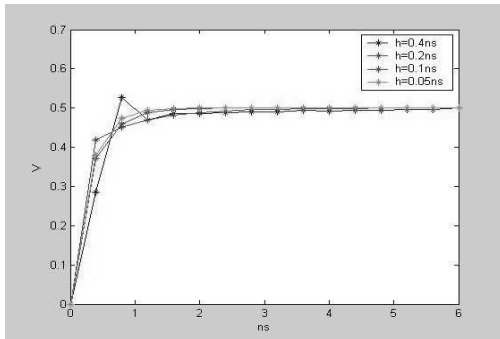


Figure.8 DC transient response of EDU-ADI with different time steps

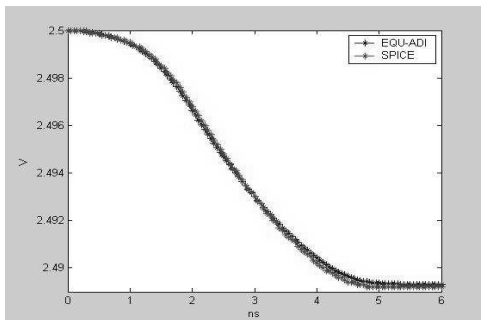


Figure.9 Accuracy Comparison with HSPICE

Figure 9 shows the waveform of the random selected cell's voltage.

We can see the error is small enough. In fact, we can shorten the time step  $h$  for obtaining high accuracy due to the  $O(h)$  accuracy of the EQUADI algorithm.

## 6. Conclusion and Future Work

This paper proposes the EQUADI algorithm to efficiently solve the transient P/G networks of the Mesh+Tree topology for high-end ASIC applications. Besides the unconditional stability and linear accuracy, the algorithm shows its superiority in the linear complexity of both run-time and memory. Thus, the algorithm can efficiently solve huge P/G networks of millions of nodes.

In future, we will polish the algorithm for efficiently solving huge P/G networks that include coarse meshes on upper layers and complex grids of different topologies in different areas on lower layers.

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