Symbolic Formulation Method for Mixed-Mode Analog Circuits using Nullors

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Abstract

A formulation method is introduced for the symbolic analysis of mixed-mode analog circuits consisting of opamps, current conveyors and/or current-feedback opamps. We show that by modeling all active devices using only nullors and grounded resistors, a reduced system of nodal equations can be formulated and solved by determinant decision diagrams. The nullor equivalents allow including parasitic elements as demonstrated in designing a universal filter.

1. Introduction

Analog signal processing applications require the use of different kinds of active elements. For instance, paper [1] lists the different kinds of active devices in the current state-of-the-art. The behavior of these devices can be modeled using nullors, for example, the nullor-based models of the different kinds of current conveyors and current feedback opamp (CFOA) are presented in [2]. As already shown in [3], the main advantage of transforming an analog circuit to a nullor-based equivalent is to use Nodal Analysis (NA) to formulate the system of equations. This paper introduces a new formulation method at the circuit level, whose solution can be performed by determinant decision diagrams [4],[5]. For large circuits, however, the solution can be performed by applying Boolean logic operations [6].

Section 2 will present the nullor equivalents of some active devices. Section 3 will describe the proposed formulation method. An opamp based circuit [7], and a current conveyor based simulated inductance [8], will be used to highlight the advantages of the method. Section 4 will present an illustrative example by including some parasitic of current conveyors in the design of a universal filter [9]. Finally, section 5 concludes this paper.

2. Modeling active devices using nullors

This section shows the nullor equivalents of the opamp and current conveyors. The CFOA can be modeled by a positive-type second generation current conveyor (CCII+) in a cascade connection with a voltage follower as shown in [2]. The nullor equivalents of other active devices, as the ones listed in [1], can be generated in a similar way. For instance, Fig. 1(a) shows the most compact model for current conveyors, it is the one associated with the negative-type current conveyor (CCII-) and includes its parasitic resistance at port X. As one sees, the CCII+ shown in Fig. 1(b) embeds the CCII- and adds two resistors and one nullor to invert the sign of the current. The dual-output CCII shown in Fig. 1(c) also embeds the CCII- between Y-X ports, the current from port X is converted to voltage through the 1Ω resistor. Then, in the upper part is the topology of the CCII+ to generate the port Z+, while to generate the port Z-, three resistors and two nullors are added in the lower part to invert the sign of the current.

As shown in the following section, the nullor equivalents include only grounded resistances because they have only one entry in the NA formulation [2], while floating ones have four entries requiring more computational work. The proposed formulation method is very suitable for opamp [7], current conveyors [2], CFOA [10], and in general for mixed-mode circuits at the integrated circuit level [11]. Moreover, the nullor also is quite useful in the synthesis of analog circuits [12], where the non-ideal performance analysis including the parasitic elements can be done by applying the proposed NA-formulation method.

3. Nodal analysis of nullor circuits

When the nullor is used to model the behavior of all active devices and to transform all non-NA compatible elements to be NA compatible ones, a

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symbolic-NA-formulation method (***i*=*Yv***) can be performed in three main steps:

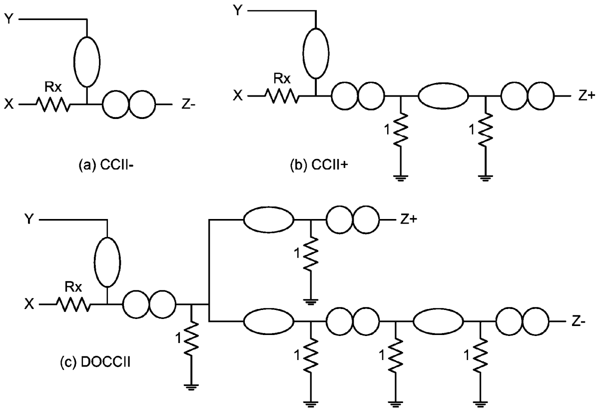

Figure 1. Modeling CCIIs using nullors and grounded resistances, and including the parasitic resistance Rx.

Step 1: Create three data structures to describe the interconnection relationships (IRs) of:

a. Norators: Generate a table to include the nodes (m,n) of each norator P_k .

b. Nullators: Generate a table to include the nodes (m,n) of each nullator O_k .

c. Admittances: Generate a table to include the name and nodes (m,n) of each admittance.

Step 2: Calculate the indexes associated to rows and columns by manipulation of the IRs calculated in step 1, and group grounded and floating admittances:

a. Set ROW: It contains all nodes (ordered) calculated by using the IRs and properties of the norator, whose nodes (m,n) are virtually short-circuited. These indexes are associated to rows and are used to fill vector ***i*** and the admittance matrix ***Y***.

b. Set COL: It contains all nodes (ordered) calculated by using the IRs and properties of the nullator, whose nodes (m,n) are virtually short-circuited. These indexes are associated to columns and are used to fill vector ***v*** and the admittance matrix ***Y***.

c. Grouping Admittances: They are structured into two tables: Table A consists of all nodes (ordered), and in each node is the sum of all admittances connected to it. Table B consists of all floating admittances and its nodes (m,n).

Step 3: Use sets ROW and COL to fill vector ***i*** and ***v***, respectively. To fill the admittance matrix ***Y***: if in Table A, a node is included in sets ROW and COL (Cartesian product described in [3]), introduce that admittance(s) in ***Y*** with the corresponding row (from ROW index) and column (from COL index). For each floating admittance connected between nodes (m,n) in Table B, search node m in set ROW and node n in set COL (do the same but now search n in ROW and m in COL), if both nodes exist that admittance is introduced in ***Y*** with the corresponding row (from ROW index) and column (from COL index), and it is negative.

Let's consider the simulated inductor taken from [8] and shown in Fig. 2. Using the nullor equivalents from Fig. 1, the resulting nullor circuit is shown in Fig. 3. The impedance Zin is calculated by adding an independent current source and by computing the voltage at node 1, so that Zin=(Vin/Iin).

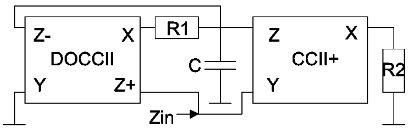

Figure 2. Lossless grounded simulated inductance.

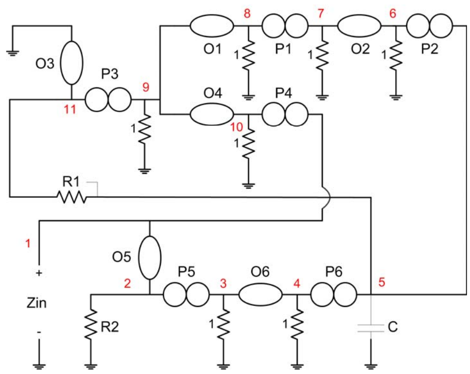

Figure 3. Nullor equivalent of Fig. 2.

From Fig. 3, the NA-formulation is done as follows:

Step 1: This step is performed as it is done in [3].

Step 2: This step is improved with respect to the one already presented in [3]. The set ROW={(1,10), (2,3), (4,5,6), (7,8), (9,11)}, the set COL={(1,2), (3,4), (5), (6,7), (8,9,10)} . The admittances are listed in Table I.

Table I. Generating Table A and Table B

Table A

Nodes	Admittances
1	0
2	g2
3..4	1
5	sC+g1
6..10	1
11	g1

Table B

Floating admittance	Nodes
g1	(5,11)

Step 3: This step is also improved with respect to [3]. The evaluation of the Cartesian product between ROW×COL leads us to the formulation given by (1). For example: since g1 is floating, the Cartesian product

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between ROW[5]×COL[3] leads us to the combination (11,5), so -g1 is added into the admittance matrix in the position (5,3) in (1). Finally, the solution is given by (2), where the parasitic resistance at terminal X of each current conveyor has been added, since it is in series connection with R1 and R2.

$$\begin{bmatrix} i_{in} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ g_2 & 1 & 0 & 0 & 0 \\ 0 & 1 & sC+g_1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & -g_1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_{3,4} \\ v_5 \\ v_{6,7} \\ v_{8,9,10} \end{bmatrix} \quad (1)$$

$$Z_{in}(s) = sC(R_x + R_1)(R_x + R_2) \quad (2)$$

As one can infer, the order of the system of equations is equal to the number of nodes minus the number of nullors (O-P pairs). This advantage of using nullors can be better appreciated in opamp based circuits. Let's consider the circuit shown in Fig. 4, where each opamp has been modeled with the nullor, and the voltage source has been transformed to current source. By applying traditional Modified Nodal Analysis, the system of equations has an order equal to the number of nodes plus the number of stamps, i.e. the order is 15 (11 nodes + 4 stamps).

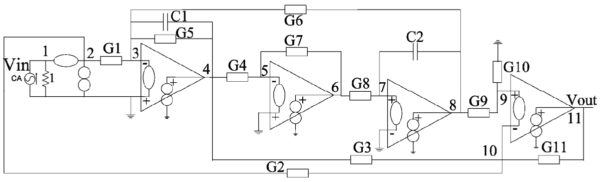

Figure 4. Opamp based RC filter taken from [7].

By applying the proposed NA-formulation method, the order is reduced to 6! (11 nodes – 5 nullors), the system is given by (3), and the solution is given by (4).

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ -G_1 & -G_5 - sC_1 & 0 & -G_6 & 0 & 0 \\ 0 & -G_4 & -G_7 & 0 & 0 & 0 \\ 0 & 0 & -G_8 & -sC_2 & 0 & 0 \\ 0 & 0 & 0 & -G_9 & G_9 + G_{10} & 0 \\ -G_2 & -G_3 & 0 & 0 & G_2 + G_3 + G_{11} & -G_{11} \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_4 \\ v_6 \\ v_8 \\ v_{9,10} \\ v_{11} \end{bmatrix} \quad (3)$$

$$\frac{v_{out}}{v_{in}} = \frac{-(G_9+G_{10})G_2G_7C_1C_2s^2 + \left((G_1G_3 - G_2G_5)(G_9+G_{10})\right)G_7C_2s - G_4G_8\left(G_1G_9(G_2+G_3+G_{11}) + G_2G_6(G_9+G_{10})\right)}{G_{11}(G_9+G_{10})\left(G_4G_6G_8 + sC_2G_5G_7 + s^2C_1C_2G_7\right)} \quad (4)$$

4. NA-formulation including parasitic

Lets us consider now the voltage-mode universal filter shown in Fig. 5, which consists of only CCII+s and whose nullor equivalent includes its parasitic resistance Rx, as shown by Fig. 1(b). The order of the system of equations by applying our proposed NA-formulation method is 12. The solution generates the exact transfer functions of the low-pass (LP), band-pass (BP) and high-pass (HP) filter responses given by (5), (6) and (7), respectively, where *D(s)* is given by (8).

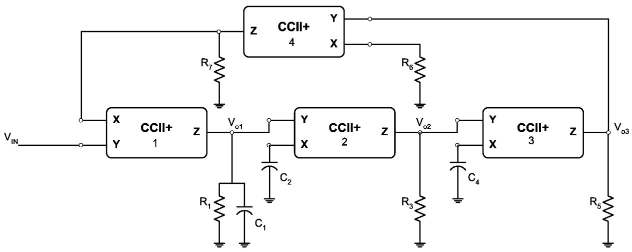

Figure 5. Voltage-mode universal filter taken from [9].

$$TF_{LP} = \frac{s^2\left[C_2C_4R_1R_{x2}R_{x3}(R_6+R_{x4})\right] + sR_1\left[C_4(R_6R_{x3}+R_{x3}R_{x4}) + C_2(R_6R_{x2}+R_{x2}R_{x4})\right] + R_1(R_6+R_{x4})}{D(s)} \quad (5)$$

$$TF_{BP} = \frac{s^2\left[C_2C_4R_1R_3R_{x3}(R_6+R_{x4})\right] + s\left[C_2R_2R_3(R_6+R_{x4})\right]}{D(s)} \quad (6)$$

$$TF_{HP} = \frac{s^2\left[C_2C_4R_1R_3R_5(R_6+R_{x4})\right]}{D(s)} \quad (7)$$

$$\begin{aligned} D(s) = {} & s^3[C_1C_2C_4R_1R_{x2}R_{x3}(R_7R_{x4}+R_6R_{x1}+R_6R_7+R_{x1}R_{x2})] + s^2[C_1C_4R_1R_{x3}(R_6R_7+R_7R_{x4}+R_6R_{x1}+R_{x1}R_{x4}) + \\ & C_1C_2R_1R_{x2}(R_6R_{x1}+R_{x1}R_{x4}+R_7R_{x4}+R_6R_7) + C_2C_4(R_6R_{x1}R_{x2}R_{x3}+R_{x1}R_{x2}R_{x3}R_{x4}+R_7R_{x2}R_{x3}R_{x4}+R_1R_3R_5R_7 + \\ & R_6R_7R_{x2}R_{x3})] + s[C_1R_1(R_6R_{x1}+R_7R_{x4}+R_6R_7+R_{x1}R_{x4}) + C_2R_{x2}(R_6R_{x1}+R_{x1}R_{x4}+R_7R_{x4}+R_6R_7) + \\ & C_4R_{x3}(R_7R_{x4}+R_{x1}R_{x4}+R_6R_7+R_6R_{x1})] + R_6R_{x1}+R_6R_7+R_{x1}R_{x4}+R_7R_{x4} \end{aligned} \quad (8)$$

By setting $R_1=R_3=R_5=R_6=R_7=R$, $C_1=C_2=C_4=C$, and by assuming that all CCII+s have the same Rx: $Rx_1=Rx_2=Rx_3=Rx_4=Rx$, then the LP, BP and HP filter responses are give in (9), (10) and (11), and *D(s)* is written in (12). The cut-off (LP and HP) or center frequency (BP) is approximated by (13).

$$TF_{LP} = \frac{s^2\left[C^2RR_x^2(R+R_x)\right] + s\left[2CRR_x(R+R_x)\right] + R(R+R_x)}{D(s)} \quad (9)$$

$$TF_{BP} = \frac{s^2\left[C^2R^2R_x(R+R_x)\right] + s\left[CR^2(R+R_x)\right]}{D(s)} \quad (10)$$

$$TF_{HP} = \frac{s^2C^2R^3(R+R_x)}{D(s)} \quad (11)$$

$$\begin{aligned} D(s) = {} & s^3[C^3RR_x^2(R^2+2RR_x+R_x^2)] + s^2\left[C^2(R^4+2R^3R_x+5R^2R_x^2+4RR_x^3+R_x^4)\right] + \\ & s\left[C(R^3+4R^2R_x+5RR_x^2+2R_x^3)\right] + R_x(2R+R_x) + R^2 \end{aligned} \quad (12)$$

$$\omega_0 = \sqrt{\frac{R^2+2RR_x+R_x^2}{C^2R_x(5R^2R_x+4RR_x^2+2R^3+R_x^3)+C^2R^4}} \quad (13)$$

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If Rx=2KΩ, R=7.75KΩ, and C= 10pF, the frequency of the filter is 1.86MHz, as shown in Fig. 6. In this case, the response is affected at high frequencies by the parasitic Rx. It requires a design centering [13]. Furthermore, in the ideal case when Rx=0Ω, the filter responses are shown in Fig. 7 for a frequency of 2MHz.

From this example, one can appreciate the usefulness of evaluating analytical expressions to gain insight on the behavior of the circuit. As a result, the proposed NA-formulation method is very suitable for analyzing mixed-mode circuits, while it can be used to generate symbolic behavioral models [14].

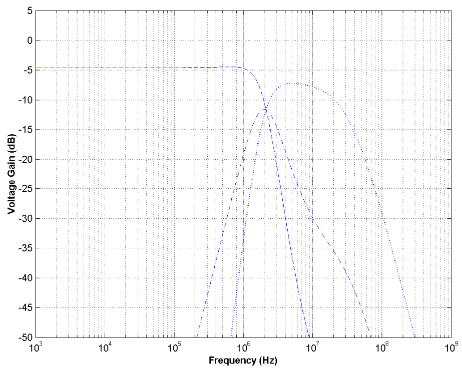

Figure 6. Responses with Rx=2KΩ: LP is in dashed-line, BP in dot-dashed line and HP in dot line.

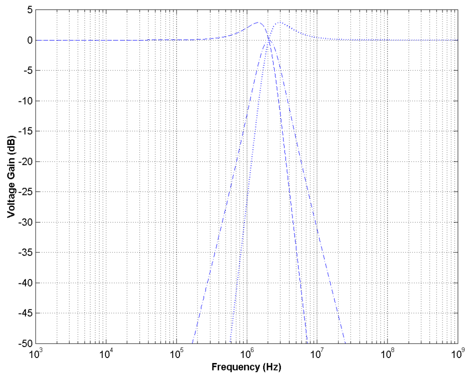

Figure 7. Responses for Rx=0Ω: LP is in dashed-line, BP in dot-dashed line and HP in dot line.

5. Conclusion

This paper has shown the usefulness of modeling active devices using nullors to formulate a reduced system of equations to compute exact analytical expressions of mixed-mode circuits consisting of opamps, current conveyors and CFOAs. The nullor equivalents allow to include parasitic elements and the formulation is performed by applying only NA. Finally, experimental examples on a universal filter demonstrate the suitability of the proposed method to gain insight into the behavior of a circuit.

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