Symbolic DDD-based Tool for the Computation of Noise in CMOS Analog Circuits

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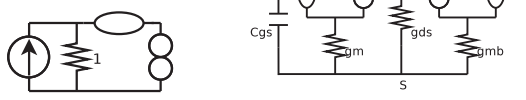
***Abstract*—In this paper we present a tool based on determinant decision diagrams (DDDs) for the automatic generation of exact fully-symbolic noise expressions of analog integrated circuits containing MOSFETs. The formulation of the circuit equations is performed through modeling all MOSFETs with their nullor equivalents and by applying symbolic nodal analysis. The derived exact fully-symbolic noise expressions are evaluated from HSPICE^{TM} simulations using the related noise equations for NLEV 0, 1 and 2. We show the good agreement between the derived symbolic-expressions and HSPICE^{TM}. Another advantage of our proposed DDD-based tool relies on its capability to compute the voltage noise generated at each circuit node, and in a simple post-processing step it can compute the current noise at each circuit branch.**

I. Introduction

It is of great concern for the integrated circuit (IC) designer to effectively face the challenges of increasing performance for analog signal processing applications [1]. In todays pervasive low voltage and low power analog IC applications, designing for low noise and low distortion is sought more actively [2]. The advantages of designing such applications using numerical and symbolic approaches has already been presented in [1], [3], [4]. It can be readily noticed that the use of nullor equivalents allows us to implement the computer algorithm using only symbolic nodal analysis formulation [5], [6]. Additionally, the small signal model for the MOSFET stamp can be increased in complexity as desired [3], [4], [6]. For instance, in this investigation only Cgs, Cgd, Gds, Gm, and Gmb are included into the nullor equivalent of each MOSFET.



(a) Nullor equivalent of an independent voltage source.

(b) Nullor equivalent of the four terminals MOSFET.

Fig. 1. Nullor equivalents.

The goal of this investigation is to show the usefulness of the nullor equivalents to formulate a small system of equations, i.e. an small admittance matrix [1], [3], [4], [6]. The resulting symbolic equations are solved to obtain a transfer function or behavioral characteristics of the analog IC under analysis. It can be performed by applying Cramer's rule, but it has been demonstrated that determinant decision diagrams (DDDs) are quite adequate in solving symbolic systems of equations [1], [3], [7]–[10]. In this manner, our proposed procedure based on DDDs is described in the following sections. First, the symbolic nodal analysis formulation by using nullor equivalents and/or pathological elements, is briefly explained in Section II, and three different kinds of noise equations are presented. The noise expressions are related to HSPICE^{TM} models known as NLEV = 0, 1, and 2. In section III, the workings of the developed DDD-based tool are explained. In section IV several amplifiers are analyzed and the resulting exact fully-symbolic expressions for noise are presented. The computed symbolic noise expressions are evaluated by using the numerical results from HSPICE^{TM} simulations. The comparisons between the evaluated symbolic noise expressions and HSPICE^{TM} simulations are plotted. Finally, the conclusions are given in section V.

II. Matrix equations formulation and solution

The symbolic nodal analysis and our proposed DDD-based procedure are described in detail in [1], [3], [7]–[10], and they are reproduced here in a short form for convenience.

A. Symbolic Nodal Analysis Formulation in Short

From a nullor equivalent circuit, two sets of pairs of nodes are formed, one for ROWs and one for COLs [5], [6]. These two sets are then used to form the admittance matrix by performing the Cartesian product of every subset [1].

In the ROW group a subset is formed for every node with no Norator connected to it, and a different subset for every group of nodes connected by floating Norators.

In the COL group a subset is formed for every node with no Nullator connected to it, and a different subset for every group of nodes connected by floating Nullators.

Two groups of admittances are formed [5]: the first (group A) containing a subset for every node listing all the admittances connected to it, the other (group B) listing floating admittances with the corresponding pair of nodes.

If a node is present in a subset in ROWs and a subset in COLs then the corresponding subset of admittances (from group A) is summed at the matrix position (ROW index,

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COL index). If a pair of nodes is present, one in a subset of ROWs and the other in a subset of COLs, the corresponding admittance (from group B) is summed with negative sign at the matrix position (ROW index, COL index).

B. Noise Sources and Symbolic Noise Analysis

To perform symbolic noise analysis, each MOSFET should be replaced with their nullor equivalent including noise sources. For instance, a thermal noise current source is attached in parallel to every resistance (capacitors and inductors are considered noiseless) and a noise current source accounting for both thermal and flicker noise is connected between drain and source for every MOSFET. Each of these noise sources has a value represented by a symbol, which is substituted by the corresponding symbolic noise equation shown by Table I, just after the transfer function is formulated.

TABLE I
NOISE EQUATIONS FOR THE MOSFET.

NOISE MODEL	THERMAL NOISE CURRENT SOURCE	FLICKER NOISE CURRENT SOURCE
NLEV 0	$\frac{8}{3}kT(G_M + G_{DS} + G_{MB})$	$\frac{KF \cdot ID^{AF}}{(COX \cdot Leff^2 f)}$
NLEV 1	$\frac{8}{3}kT(G_M + G_{DS} + G_{MB})$	$\frac{KF \cdot ID^{AF}}{(COX \cdot Leff^2 \cdot Weff^2 f)}$
NLEV 2	$\frac{8}{3}kT(G_M + G_{DS} + G_{MB})$	$\frac{KF \cdot GM^2}{(COX \cdot Leff^2 \cdot Weff^2 \cdot f^{AF})}$

In order to solve the system of noise equations for a given node considered to be the output, at least two determinants should be computed: one for the original admittance matrix in order to obtain the denominator and the other for the admittance matrix with the independent sources vector substituting the column of the desired output node to obtain the numerator (Cramer's rule). Additional determinants for the denominator must be computed if superposition of independent sources has to be performed. Symbolic determinants are formulated by using DDD structures [1], [7]–[10], where a symbol is generated for every element of the Nullor equivalent circuit which conveniently contains only Norators, Nullators, impedances and current sources.

III. DDD-BASED TOOL

A. Matrix Formulation from HSPICE^{TM} Netlist

The HSPICE^{TM} netlist is read as input, from which sets for impedances, nullators, norators and independent sources are formed. Transistors and independent voltage sources are replaced by their nullor equivalents from Fig. 1, which are quite suitable for symbolic nodal analysis. If symbolic noise analysis is to be performed, independent sources are removed, the corresponding nodes are grounded and the noise current sources are inserted in place in the circuit.

The admittance matrix is then formulated as explained in the previous section by performing simple row and column operations over the adjacency matrix of the nullor equivalent circuit. The entries of this admittance matrix consist of a sum of elements which are encoded as an index reference and a 1 or a -1 to account for the sign of the element in the matrix [1]. This index refers to a new structure which stores signature information pertaining to every element of the nullor equivalent circuit [3]. This information consists of the symbol for the element stored as a string, a numerical value if available and the position and sign of every occurrence of this symbol in the admittance matrix. This last information is useful if the need to perform the first derivative of a symbol arises.

Numeric values are automatically read from the HSPICE^{TM} netlist file, the operating point and the transistor model reported in the HSPICE^{TM} output listing while physical constants are hardcoded [4].

Rows and columns of the admittance matrix are represented by the sets of nodes grouped according to the procedure described in the previous section [1], so the available outputs are given by the COLs group of node sets. To generate the transfer function or a behavioral symbolic expression, at least two different determinants must be computed. This procedure is done by using DDD structures and applying superposition of non-correlated independent sources [6].

B. DDD Implementation

The DDD structure implemented in this tool is a tree in which the arithmetic operations are encoded in the depth of the tree node, that is, different depth implies multiplication while equal depth implies addition. Every element of the DDD structure corresponds to a position of the admittance matrix. The structure is built recursively in a depth-first fashion [7], [8], [10], and provisions are made in order to stop the recursion and send a prune signal if a zero is encountered in a given path. This prune signal is propagated all the way up until a summing point is reached so the whole branch does not form part of the final structure and the path is terminated to zero instead. Extra elements are added to the structure after the recursive call to the constructor function so such a path is never actually allocated in the DDD structure. This results particularly useful when dealing with sparse matrices.

The actual formulation of the symbolic determinant expression is done by concatenating the symbols while searching the tree structure in depth-first fashion, numerical arithmetic operations are performed only to the symbol coefficient. To formulate the numerical expression, the same procedure is followed but instead the numerical values of the circuit element signature are read and the numerical arithmetic operation is performed on every recursion step.

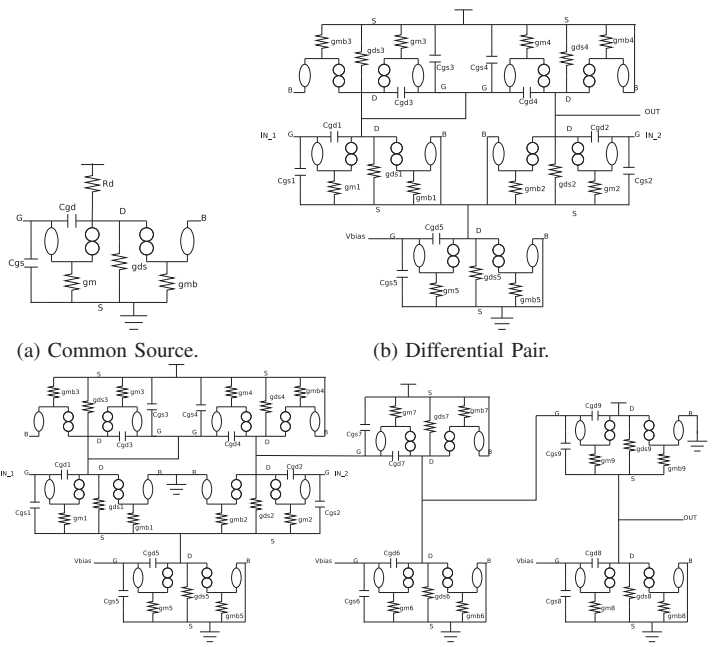
C. Numerical Evaluation and Validation

A final step consists of evaluating both s (complex variable) and f (frecuency in flicker noise equations) symbols in order to draw the output noise vesus frequency plot. The output noise table reported in the output listing of the HSPICE simulation is read and stored in vectors and then superimposition of both plots is done in order to compare results.

IV. SYMBOLIC NOISE ANALYSIS AND EXPERIMENTAL VALIDATION

Three MOSFET based amplfier circuits are selected from [2], [4], to perform symbolic noise analysis, they are: common

source amplifier, differential pair and an uncompensated three stages amplifier. Their nullor equivalents are shown in Fig. 2.



(a) Common Source. (b) Differential Pair.

(c) Three stages uncompensated amplifier.

Fig. 2. Nullor equivalents of the amplifier circuits.

The associated noise sources are added as explained before: one current noise source accounting for both thermal and flicker noise for each transistor and a current noise source for every resistance. That way, the symbolic voltage noise output expression for the amplifier in Fig. 2a is formulated by (1) for NLEV=0. It is evident that the automatic results provided by our proposed DDD-based tool coincide with hand calculation for the output noise. Recall that for NLEV 0 the term g_m^2 is not present and ${I_D}^{AF}$ is used, instead.

The symbolic expression for the common source amplifier is then evaluated and plotted against the HSPICE results in Fig. 3a for NLEV 0, and in Fig. 3b and Fig. 3c for NLEV 1 and 2, respectively.

$$V_{n,out}^2 = \frac{\frac{8}{3}kT(gds + gm + gmb) + \frac{4kt}{r_d} + \frac{{I_D}^{AF} \cdot KF \cdot TOX}{Leff^2 \cdot EOX \cdot f}}{(gds + s \cdot Cgd + 1/r_D)^2} \quad (1)$$

In Fig. 4 and Fig. 5, the responses for the differential pair and the uncompensated three stage amplifier are plotted for NLEV 0, 1 and 2.

V. Conclusion

Good agreenment between the numerical evaluation of the derived symbolic noise expressions and the results provided by the numerical simulator (HSPICE) were obtained. Besides, the developed DDD-based tool can run with the same netlist for input as HSPICE avoiding the need for intermediary processing steps. Results can be shown for any node in the circuit and current noise reported for any branch.

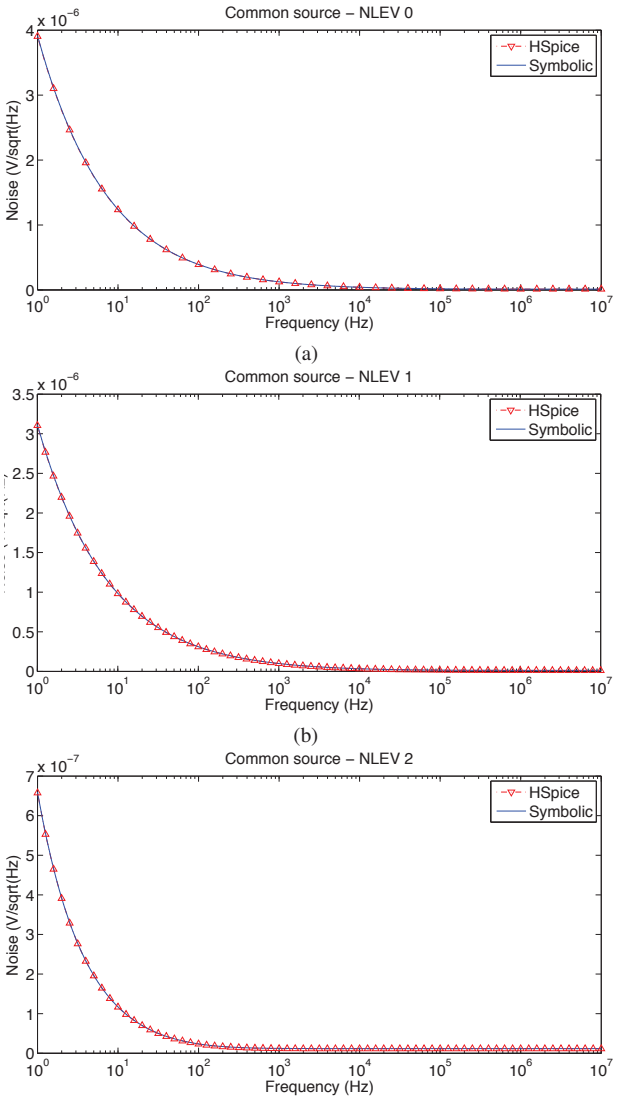


Fig. 3. Responses for the common source amplifier.

Symbolic evaluation of output noise figures have already been reported in [6] and in [4]. The improvement presented in this work is the implementation of efficient algorithms for the solution of the determinant, i.e. by aplying DDDs. According to [1] regarding DDDs, in general they present the most efficient way to compute the symbolic determinant of a matrix.

An additional advantage is the highly parallel nature of the resulting DDD structure which comes handy when evaluating big matrices with todays multicore computing systems. The formulated fully symbolic expressions represent the system to the highest accuracy bringing the possibility to perform with more detail analysis which benefit greatly by using symbolic expressions.

VI. Acknowledgements

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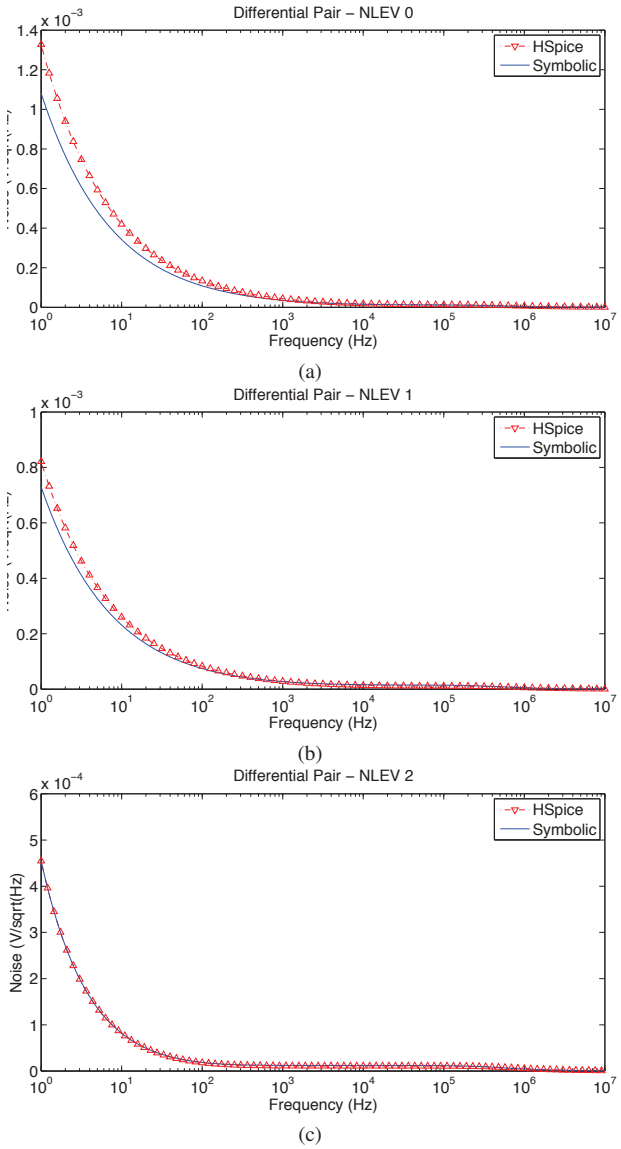

Fig. 4. Responses for the Differential Pair Amplifier.

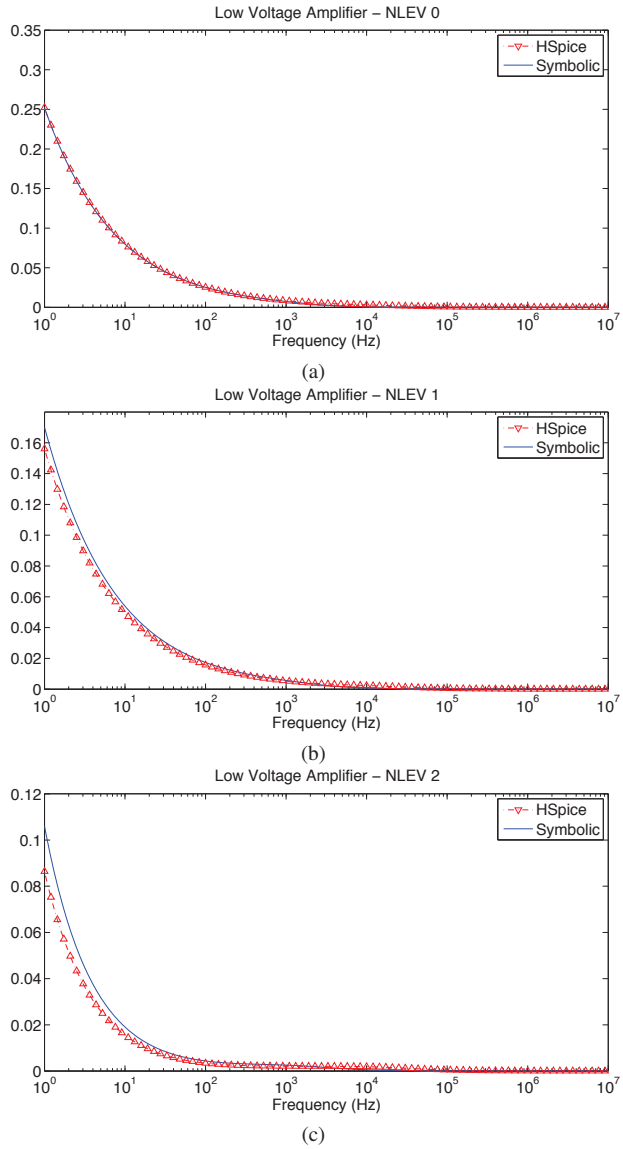

Fig. 5. Responses for the three stages uncompensated amplifier.

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