Macromodeling for RF Passives via Circuit Reduction of VPEC Model

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Abstract **To accelerate the macro-model generation for RF passive components considering parasitics, we introduce the Vector Potential Equivalent Circuit (VPEC) to ef ciently model the massively coupled passives, like transmission lines and inductors. It enables the passive sparsi cation of the inductance matrix by pruning the small off-diagonal elements with the desired accuracy. To further reduce the model order, we apply a hierarchical s-domain circuit reduction to generate a reduced driving-point impedance function, and then use the Brune's one-port network synthesis to realize the impedance function by a low-order RLCM ladder circuit as the compact macro-model. We have applied this method to generate the macro-model for the spiral inductor during the design of a cross-coupled LC oscillator. The synthesized lower-order macro-model is accurate up to 10GHz with 50X speedup in the time-domain simulation.**

Index terms: Hierarchical Circuit Reduction, VPEC Model, RF Passives Modeling

I. INTRODUCTION

As RFIC technology advances with increased operating frequency and decreased feature size, the passive components become increasingly signi cant as the active device. It is due to the fact that parasitics of passive components will detune RF circuits with the sub-optimized performance [1]. To accurately model parasitics in a wide frequency range, Partial Element Equivalent Circuit (PEEC) [2] in terms of RLCM (M here stands for mutual inductance) networks are generated from discretized conductors by volume decomposition according to the skin-depth and longitudinal segmentation according to the wavelength at the operating frequency. The parasitic extraction based on this approach [3] [5] has less computation effort than the full-wave modeling and higher accuracy than the simple lumped models. However, because PEEC model typically results in a large RLCM network with densely coupled partial inductance matrix L, it still challenges the circuit level simulation in two aspects: (i) a dense inductively coupled network sacri ces the sparsity of circuit matrix; (ii) the model order of the circuit matrix is too high. It slows down the simulation and even makes the simulation infeasible. Therefore, inductance sparsi cation and model order reduction are two necessary approaches to reduce the model complexity.

In this paper, we proposed a new RLCM circuit reduction and realization ow for any distributed high-order circuits. We rst pre-sparsify the massively coupled mutual inductance by the VPEC (Vector potential Equivalent Circuit) model [6], [7] with the preserved passivity, where we have developed a window-based VPEC model extraction to avoid the expensive full-inversion as in [7]. With the sparsi ed VPEC model for the RLCM circuit, we further apply a general hierarchical circuit reduction technique (H-reduction for short in the sequel) [8] to generate the driving-point impedance function. To reduce the order of the impedance function and further improve its numerical stability, we have proposed an ef cient data scaling scheme during the H-reduction. Finally, a direct circuit synthesis based on the Brune's procedure [9] is applied to realize the driving-point impedance function, and it results in a low-order RLCM ladder circuit as the macro-model.

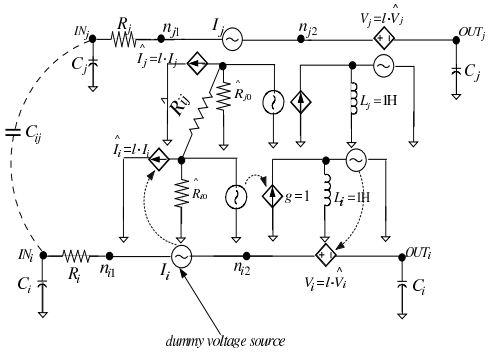
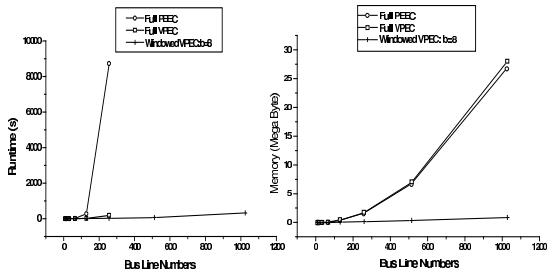


Fig. 1. The Vector Potential Equivalent Circuit model for two fi laments.

The remaining part of this paper is organized as follows. In Section II, we discuss the VPEC model sparsi cation for the massively coupled inductance. In Section III, we review the H-reduction with a dynamical scaling technique to generate the numerical stable and reduced driving-point impedance function. Furthermore, we present the macro-model realization based on the Brune's one-port network synthesis. In Section IV, we present the experimental results for several industry examples, including interconnects and spiral inductors. Finally, we conclude the paper with discussions in Section V.

II. VECTOR POTENTIAL EQUIVALENT CIRCUIT

Because the inductance is the long-range effect, it sacri ces the sparsity of the circuit matrix, and becomes the primary contribution to increase the complexity of the model. Furthermore, the direct truncation of the inductance matrix results loss of passivity [10]. In this paper, we utilizes the newly developed VPEC model [6], [7] to sparsify the mutual magnetic coupling. By pre-removing the dense mutual inductive couplings, we



(a) (b)

Fig. 2. Runtime and memory usage comparisons of bus lines with one segment each line using the PEEC model, the full VPEC model, and the windowed VPEC model (b=8).

can obtain a less dense RLCM network and hence further ef ciently apply the hierarchical circuit reduction.

The VPEC model is derived from following vector potential based Maxwell equations for inductive effects:

$$\nabla^2 A^z = -\mu J^z \tag{1}$$

$$\frac{\partial A^z}{\partial t} = -E^z \tag{2}$$

Its circuit equations contain an *effective resistance* matrix that is positive de nite and strictly diagonal dominant [7]:

$$(\frac{1}{\hat{R}_{i0}} + \sum_{j\neq i}\frac{1}{\hat{R}_{ij}})V_i + \sum_{j\neq i}(-\frac{1}{\hat{R}_{ij}})V_j = l^2\frac{\partial I_i}{\partial t} \tag{3}$$

where l is the lament length. As shown in Fig.1, this model consists of electrical circuit (PEEC resistance and capacitance) and magnetic circuit (VPEC effective resistance and controlled source). It includes the following components: (1) The wire resistance and capacitance same as those in the PEEC model; (2) A dummy voltage source (sensing electrical current I_i) to control $\hat{I}_i$; (3) A voltage controlled current source to relate $\hat{V}_i$ and $\hat{I}_i$ with gain $g = 1$; (4) An electrical voltage source V_i controlled by $\hat{V}_i$; (5) Effective resistances including ground $\hat{R}_{i0}$ and coupling $\hat{R}_{ij}$ to consider the strength of inductances; and(6) A unit inductance L_i to: (i) take into account of the time derivative of A_i; and (ii) preserve the magnetic energy from the electronic circuit.

However, the truncation-based sparsi cation in [7] needs the full inductance matrix (L) inversion ($O(N^3)$), it becomes impractical for both extraction time and memory allocation for the large sized system. Moreover, the directly truncated matrix may be not accurate enough to represent the original full matrix. As shown in [11] that all entries of the L inverse matrix can be approximately reconstructed just from entries of the sub-matrices in L corresponding to the coupling window of the active aggressor. Based on this windowing technique, we develop an ef cient VPEC model extraction and sparsi cation with a reduced computation complexity ($O(Nb^3)$), where b is the size of the window.

We compare the runtimes and model size by extracting and simulating a number of aligned parallel buses using the PEEC model, the full VPEC model, and the windowed VPEC (wVPEC) model (b=8), respectively. The runtime for the full or wVPEC model includes both VPEC extraction and SPICE simulation time. The model size refers to the le size of the resulting SPICE netlists. We plot the runtime vs. the bus size in Fig. 2 (a) and the model size vs. the bus size in Fig. 2 (b).

When the scale of wire number is small, there is no runtime speedup observed for the full VPEC model. However, when the scale of wire becomes larger (greater than 64-bit), the runtime of the full VPEC model is found 10X times faster than the PEEC model on average. For the 256-bit bus, the full VPEC model is 47X (185.39s vs. 8726.85s) faster than the PEEC model. Due to the additional introduced circuit elements, the size of SPICE netlist for full VPEC model is around 10% larger than the full PEEC model in average.

Both the PEEC model and the full VPEC model can only handle the bus circuit with up to 256-bit because HSPICE can not further allocate enough memory to complete the simulation. On the other hand, the wVPEC model (b=8) can handle much larger size up to thousand bits. Moreover, it is easy to see that the scalability of the wVPEC models shows a slow increase with respect to the increase of the bus line numbers. For example, it achieves over 1,000X (9.71s vs. 8726.85s) speedup for 256-bit bus in runtime compared to the PEEC model. In all the simulation, the wVPEC model has a very small waveform difference (less than 3%) in terms of delay when compared to the PEEC model.

In the following part, we further apply the hierarchical circuit reduction and the Brune's one-port synthesis based realization. Because VPEC based sparsi cation preserves passivity, the sparsi ed VPEC model is positive real and can be further realized as a passive RLCM circuit.

III. Circuit Reduction and Realization

With pre-sparsi ed VPEC model for the RLCM circuit, we can ef ciently perform the hierarchical circuit reduction. The general s-domain H-reduction can be viewed as a generalized block-level Gaussian elimination algorithm based on MNA (modi ed nodal analysis) formulation [8]. Unlike the existing circuit reduction algorithms [12] [14], where nodal voltages are eliminated or current branches are merged one at a time. The hierarchical reduction method reduces multiple nodes at a time. Furthermore, this method allows the more general MNA formulation, and performs the reduction on the circuit matrices directly. As a result, it allows the reduction of any SPICE compatible model even with controlled sources, such as the VPEC model.

A. Hierarchical Circuit Reduction with Dynamic Scaling

We rst review the H-reduction. Assume $\mathbf{A}^{II}$ is the sub-matrix to be reduced in the original circuit matrix $\mathbf{A}$:

$$\begin{bmatrix} \mathbf{A}^{II} & \mathbf{A}^{IB} & 0 \\ \mathbf{A}^{BI} & \mathbf{A}^{BB} & \mathbf{A}^{BR} \\ 0 & \mathbf{A}^{RB} & \mathbf{A}^{RR} \end{bmatrix} \begin{bmatrix} \mathbf{x}^I \\ \mathbf{x}^B \\ \mathbf{x}^R \end{bmatrix} = \begin{bmatrix} \mathbf{b}^I \\ \mathbf{b}^B \\ \mathbf{b}^R \end{bmatrix}. \tag{4}$$

After $\mathbf{A}^{II}$ is reduced, $\mathbf{A}^{BB}$ will become $\mathbf{A}^{BB} - \mathbf{A}^{BI}(\mathbf{A}^{II})^{-1}\mathbf{A}^{IB}$. It was shown in [15], the new element at (u, v) in the modi ed $\mathbf{A}^{BB}$ will become

$$a^{BB*}_{u,v} = \frac{det(\mathbf{A}^{II}_{(u,v)})}{det(\mathbf{A}^{II})}, \tag{5}$$

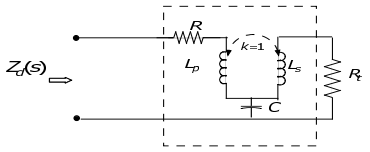


Fig. 3. Brune's driving point synthesis by multiple stage of RLCM ladders (Brune's cycle).

where $det(\mathbf{A}^{II}_{(u,v)})$ is the determinant that consists of matrix A^{II} plus row u and column v of the atten matrix of the whole circuit. Some new admittances in the reduced matrix become rational functions of s after the reduction, and we can obtain the driving-point impedance function when there are only one-port remained.

It was shown in [8], this circuit reduction will give the s-polynomial (that can be truncated) of the determinant of the original atten circuit matrix. However, to nally obtain a reduced and realizable output model, it requires the resulted impedance/admittance rational function to be numerically stable. Without a robust scaling, the reduction process will be very sensitive to the numerical magnitudes of the admittances in the given circuit and is not numerical stable for general circuit reduction. We have used an ef cient dynamic scaling scheme during the H-reduction. The idea of dynamic scaling is to scale the non-zero coef cient of the smallest order of s in the denominator of $a^{BB*}_{u,v}$ to 1. For instance, for polynomial $\frac{10+2s+0,4s^2}{20+4s+0.8s^2}$, the scaled polynomial is $\frac{0.5+0.1s+0.02s^2}{1+0.2s+0.04s^2}$. A polynomial with the non-zero coef cient of the smallest order of s scaled to 1 is called normalized. For a rational function, normalization means its denominator is normalized. To further guarantee the passivity of the scaled rational function, we nally apply the passivity enforcement via quadratic programming based constrained least squares tting [16].

B. Brune's One-port Synthesis

To obtain a low-order compact RLCM model for RF passive components, we further devise a driving-point synthesis procedure extended from circuit admittance realization theory. The driving point synthesis for RLCM circuits was studied earlier by Brune in his signi cant paper [17], where he pointed out that any positive real (PR) driving-point impedance $Z(s)$ can be realized by a passive multiple-stage RLCM ladder network (see Fig. 3). Note that implementation of this synthesis procedure primarily depends on the numerical stability of the rational function to be synthesized. In this paper, with the enhanced scaling theory during the H-reduction, we are able to practically implement this procedure for macro-model realization. The synthesized macro-model is a one-port model that can be used for the impedance matching for LNA or central frequency tuning for VCO [18]. However, for the synthesis of the general transfer function, the synthesis two-port or multi-port network needs be applied.

We present our realization procedure in Fig. 4. The procedure has the input of driving-point impedance ($Z_{in}(s)$), and the desired cycle number (Nc) for the macro-model. The output will be a RLCM spice netlist. During each cycle, we check the PR property of the remainder impedance $Z_f(s)$ ($Re\{Z_f(s)\} > 0$). After Nc (user speci cation) cycles we exit

BRSYN ($Z_{in}(s)$, Nc)
While ($iter \leq Nc$ and Z_0 is PR) {
  Do $j\omega$-axis pole/zero check/remove {
    $Z_0(s)$ = Foster' Preamble Procedure;
  }
  Search minimum resistance $Re\{Z_0(s)\}$ at its frequency ω_0;
  Synthesize Brune's RLCM ladder-cycle (Z_0, ω_0);
  $Z_0(s)$ = $Z_f(s)$ = Remainder impedance;
  $iter++$;
}
Calculate termination resistor R_t by $Z_f(s)$;

Fig. 4. Brune's One-port RLCM Macro-model Synthesis

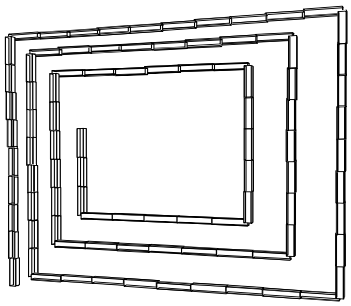


Fig. 5. A discretized spiral inductor to generate the distributed RLCM PEEC/VPEC model.

the synthesis procedure with a remainder impedance $Z_f(s)$, and terminate the procedure by adding a termination resistor R_t:

$$R_t = Z_f(s)|_{s\to 0} \tag{6}$$

Generally, the order a driving-point rational function decreases 2 degrees during every synthesis cycle with increasing 1 order of a RLCM ladder. By increasing ladder stage number Nc, we increase the model order and capture more poles.

IV. Experimental Results

In this section, we present experimental results. The accuracy and ef ciency of the reduction procedure is illustrated through various industrial examples, including interconnects and spiral inductors. We rst present the extraction speedup of windowed VPEC model compared to the full inversion based approach. Then we compare waveforms predicted by our synthesized macro-model with the original circuit. In the end, we give the simulation ef ciency comparisons scaled with different circuit sizes.

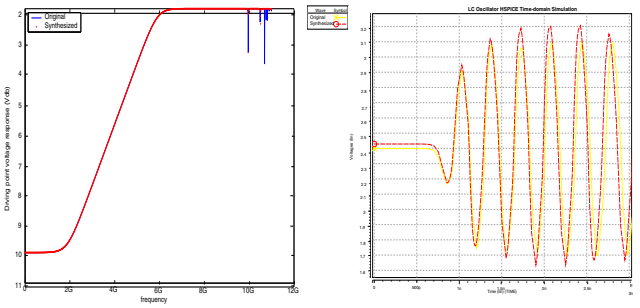
We assume the copper ($\rho = 1.7 \times 10^{-8}\Omega \cdot m$) metal. The partial inductance is extracted by FastHenry [4], where each wire segment is modeled by one lament, and coupling between any pair of segments (including segments in a same line) is considered. Hence a much high-ordered RLCM circuit is generated. Moreover, volume- lament decomposition is applied to take into account the skin and proximity effects. The capacitance is extracted by FastCap [3]. Because capacitive coupling is a short-range effect, only adjacent couplings are considered. By applying an ac current source at one input port, we observe the near-end response. All circuits are simulated by SPICE3 on Linux workstation with dual 1GHz P-III CPUs and 2G memory.

We rst present the result of a 3-turn spiral inductor with 92 segments discretized as shown in Fig. 5. A distributed

1	2	3	4	5	6	7	8
Circuits	#Nodes	Sparse Ratio	Reduction Ratio	Overhead Time(s)	Simulation Time(s) w/o Redu.	Simulation Time(s) w Redu.	Simulation Speedup
ckt1	21	No SP	55.2%	0.12	0.05	0.04	1.2X
ckt2	180	33.3%	90.1%	0.77	0.17	0.04	4.1X
ckt3	3460	77.5%	94.2%	8.6	6.13	0.10	58.3X
ckt4	20650	90.5%	98.1%	21.1	99.14	0.11	901X
ckt5	81900	95.2%	99.7%	23.7	2241.12	0.52	4309X

TABLE I

COMPARISON OF SIMULATION EFFICIENCY BETWEEN THE ORIGINAL AND SYNTHESIZED MODEL.



(a) (b)

Fig. 6. (a) Frequency-domain responses at the driving-point of the original and synthesized models for a 92-segmented spiral inductor. (b) Time-domain waveforms at the output of the original and synthesized models for a cross-coupled LC oscillator.

PEEC/VPEC model is then generated and further reduced. In Fig. 6 (a), the frequency domain response at the driving-point of the synthesized macro-model with 3 stages agrees well with original circuit up to 10GHz. Furthermore, we compared the time-domain waveforms of the synthesized and original model of the spiral inductor in a cross-coupled LC oscillator. As shown in Fig. 6 (b), there is only 2% waveform differences but with 50X simulation speedup. Note that the synthesized one-port macro-model can be used to ef ciently predict the critical performance parameters of spiral inductor, such as the ω_T and Q factor [18]. Moreover, the substrate loss can be included during the generation of the distributed RLCM circuit and is intended for the future study.

Table I further shows the ef ciency of the model reduction procedure as measured in CPU runtime vs. the corresponding sparsi cation and reduction percentage. Several different sized industry circuits are used. The synthesized models are RLCM ladders up to 3 stages. It compares the simulation time of PEEC input circuits without reduction with that of reduced and realized VPEC output circuits. Simulations of both original circuits and reduced circuits are performed by SPICE3 in frequency domain. As seen from the table, signi cant speedup (up to 4000X) is obtained for synthesized low-order macro-modeling simulation with little overhead paid in circuit sparsi cation, reduction and realization. Since macro-model generation is only performed once, their overhead time are not included in the simulation time during the comparison with SPICE3.

V. CONCLUSIONS AND DISCUSSIONS

The proposed compact modeling methodology leverages the novel circuit reduction [8] and electromagnetic modeling [7] with the well-developed network synthesis [9], which is the potential complexity reduction approach for the design and simulation of RF passives when considering parasitics. Our experimental results show the low-order macro-model can well capture the original system frequency-response up to 10GHz and with 1000x times simulation speedup.

However, the impedance function is obtained from the single-point expansion, which introduces the primary error in the ultra-high frequency range. A multi-point expansion based approach is under study to improve the accuracy.

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