Leveraging Recovery Effect to Reduce Electromigration Degradation in Power/Ground TSV

Shengcheng Wang*, Zeyu Sun†, Yuan Cheng‡, Sheldon X.-D. Tan†, and Mehdi B. Tahoori*
*Chair of Dependable Nano Computing (CDNC), Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany
†Department of Electrical and Computer Engineering, University of California, Riverside, CA, USA
‡Department of Micro/Nano-electronics, Shanghai Jiao Tong University, Shanghai 200240,China

***Abstract*—With increasing temperature and current density, electromigration (EM) becomes a major interconnect reliability challenge in power distribution networks (PDNs) of three-dimensional integrated-circuits (3D ICs). In order to improve the EM reliability of power/ground (P/G) through-silicon-vias (TSVs), the conventional solution is to use larger TSVs in order to decrease the current densities. In this work we exploit the recovery effects for EM reliability improvement by periodically deactivating P/G TSVs. In order to predict EM-related lifetime for TSV accurately, a novel three-phase EM model is proposed with a focus on single damascene via-last process. Different from existing TSV EM models, the new TSV EM model considers the nucleation phase and the impacts of initial thermo-mechanical stress, which is significant for the TSVs in addition to this recovery effect modeling. Furthermore, a recovery-aware repair architecture is developed for EM reliability improvement. Applied to 3D benchmark designs, the proposed repair approach increases EM-related lifetime of the P/G TSV grid by 4.4X in average relative to the conventional TSV sizing method, with negligible area overhead.**

I. Introduction

Through-silicon-via (TSV)-based three-dimensional integrated circuits (3D ICs) have emerged as a promising option to overcome interconnect bottlenecks in CMOS scaling by leveraging fast, dense inter-die vias [1]. The vertical connections between stacked dies (i.e., TSVs) can provide abundant interconnect bandwidth with improved performance and less communication-energy consumption. However, concerns related to TSV reliability are key obstacles in the commercial exploitation of TSV-based 3D ICs technology [2]. One of the critical TSV reliability challenges is electromigration (EM).

EM refers to the diffusion of metal atoms induced by electric current [2], which can reduce system reliability and potentially cause short or open circuit failures. Compared to the conventional interconnects in 2D ICs, EM reliability in TSVs becomes further exacerbated by increasing current density, higher temperature, and thermal-mechanical stress [3]. In addition, as power/ground (P/G) TSVs in the 3D power distribution network (PDN) experience large amount of unidirectional currents, they are more susceptible to EM degradation than signal TSVs carrying bidirectional currents. As a result, the EM effect can lead to void nucleation and growth in TSVs during field-operation, and significantly increase their resistances, which affects the power distribution to the underlying logic circuitry and may cause harmful voltage drops [4]. Therefore, long-term EM reliability challenge for P/G TSVs needs to be addressed.

For TSV modeling, recently, some physics-based EM analysis methods have been proposed based on solving the basic mass transport equations [5–8]. However, those EM models consider the failure of a wire as specific atomic concentration changes due to EM-induced atomic flux. But as we mentioned early, the practical voids do not nucleate inside TSVs. Also those models do not consider the void growth phases, which plays as the key role in the TSV resistance changes [9]. Recent works on TSV EM analysis focus on thermo-mechanical stress impacts on TSV. Work in [10] developed a model for TSV resistance changes over time. But this model ignores the nucleation phase.

In order to improve the EM reliability of P/G TSV, the conventional approach is based on increasing TSV diameter for current density reduction. Such "TSV sizing" technique can be combined with 2D PDN optimization under the constraints of EM reliability, temperature, and voltage drop [11]. This way, the EM-related lifetime of TSVs can be extended at the cost of reduced available routing area. While such scheme only focuses on current density reduction, the transient recovery effect in EM-induced stress evolution is ignored. Here, the "recovery effect" refers to the EM stress relaxation in the TSV, which occurs when there is no/lower/reverse current passing. Consequently, this healing process can extend the EM-related lifetime of a TSV as it will take longer time for the stress to reach to the critical threshold for void nucleation [12]. Such phenomena have been observed in many previous experimental work [13], [14]. According to the observations in these experiments, the EM recovery effect possesses directional property, i.e., the recovery phenomenon is more visible when the interconnect is stressed by bi-directional current waveforms compared to unidirectional ones. Since P/G TSVs in 3D PDNs carry unidirectional currents, the major challenge here is how to leverage recovery effect for lifetime enhancement without impacting the normal operation.

In this paper, a recovery-aware repair solution is proposed to enhance the EM-related lifetime reliability of P/G TSV grid. Here we trade off the current density with EM recovery effect by using more TSVs of smaller diameters, which can be partially deactivated in a periodic manner. This way, the *ab initio* voltage drop constraints can be met with the similar routability impacts. To this end, we propose a set of TSV repair methodology including recovery-aware lifetime-prediction model and a TSV repair architecture. Overall, our contributions are summarized as follows:

- A specific 3-phase EM model for TSVs is proposed, which focuses on single damascene via-last process. The new TSV EM model considers the nucleation phase and the impacts of initial thermo-mechanical stress, which is significant for the TSVs in addition to this recovery effect modeling.
- A P/G TSV repair architecture for EM reliability based on periodic TSV deactivation is developed by leveraging recovery effect.
- A set of optimization approaches for balancing the trade-off between TSV count, TSV size, and the number of deactivated TSV under the constraints of EM reliability, routing area, and *ab initio* voltage drop.

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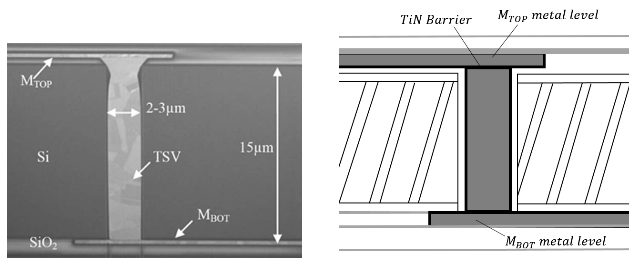
Our simulation results demonstrate that the recovery-aware repair approach increases EM-related lifetime of the entire P/G TSV grid by 4.4X in average compared to the conventional method [11] with negligible area overhead.

The rest of this paper is organized as follows. Preliminaries and related prior work are presented in Section II. Section III and Section IV describe the proposed TSV EM model and repair architecture in detail. In Section V, we report simulation results. Finally, conclusions are drawn in Section VI.

II. Preliminaries & Related Work

A. EM reliability of single damascene TSV structure

Figure 1(a) shows a real SEM cross section of a real copper TSV single damascene structure. Figure 1(b) shows the schematic of the same TSV structure. This method is based on a stack of two silicon wafers using Direct Bonding technology. In this TSV structure, both Cu metal layers (top and bottom, M_{BOT} and M_{TOP}) have a TiN encapsulation barrier, and a SiN capping. Since M_{BOT} is processed prior to wafer bonding, both M_{BOT}/TSV and M_{TOP}/TSV interfaces are TiN. As a result, the TSV is completely encapsulated by the TiN barrier at the both top and bottom (in addition to the side of the TSV). With that specific structure, EM analysis for TSV is different with dual damascene copper interconnect. It was reported that voids would only be found in M_{TOP} and M_{BOT} right above or below the TSV depending on the electric flux direction [15]. Also, initial stress due to thermo-mechanical stress generated during fabrication process is significant and its distribution is not uniform.



(a) SEM cross section of a copper TSV structure, courtesy of [9].

(b) Schematic description of the TSV structure

Figure 1: (a)The SEM view of a TSV structure, courtesy of [9] , (b)The schematics of a TSV structure.

B. 3D power distribution network

In a 3D IC, the supply power is fed from the package through Controlled Collapse Chip Connection (C4) bumps and distributed over the bottom-most tier via on-chip mesh-based PDN. In order to reach upper tiers, the supply power needs to travel through P/G TSVs connecting different tiers. As shown in Figure 2(a), the on-chip PDN is based on a mesh structure, in which the pitch and the width of the mesh determine the distance between each P/G line and the thickness of each power wire, respectively. As shown in Figure 2(b), a 3D PDN can be constructed using a global level mesh routed in the top metal layers, where there is one P/G network for the entire chip. For each tier, there is an individual 2D P/G mesh, which is connected using TSVs.

C. Related prior works

Although EM has been studied for many decades until now, the TSV EM is still an open problem as an unavoidable source of degradation. Several works have explored the EM reliability issues on P/G TSVs, which can be divided into two categories. One category is focused on TSV EM modeling. Recently, some physics-based EM analysis methods have been proposed based on solving the basic mass transport equations [5–8]. However, those EM models consider the failure of a wire as specific atomic concentration changing due to EM-induced atomic flux. But as mentioned before, voids do not nucleate inside TSVs. Also those models do not consider the void growth phases, which plays a key role in the TSV resistance changes [9]. Work in [10] developed a model for TSV resistance changes over time. But this model ignores the nucleation phase.

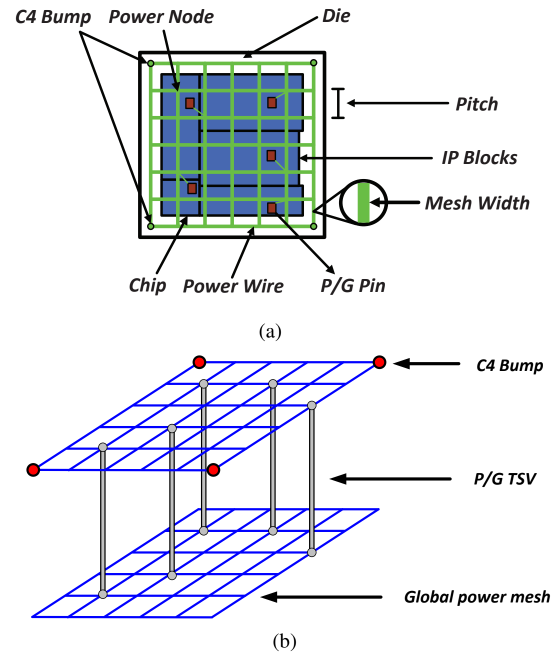


Figure 2: (a) On-chip power distribution network. (b) Three-dimensional uniform power distribution network.

The focus of the other category is on EM robustness from the perspective of 3D PDN design optimization. In [11], a tier-based optimization approach for resizing the 3D PDN (including 2D metal track widths and P/G TSV sizes) was proposed to satisfy voltage drop, thermal, and EM reliability constraints. For via-first/middle P/G TSVs, a design technique was proposed in [16] to handle the trade-off between EM reliability of P/G TSVs and the timing performance of 3D ICs. The optimal number of local vias for each P/G TSVs can be determined to minimize the routing congestion induced by local vias while satisfying the given requirement of EM reliability. In [17], a P/G TSV/micro-bump fault tolerance scheme was developed to improve the reliability of 3D PDNs. In summary, the main idea of these approaches is to utilize the increased silicon area (e.g., the increased 2D metal track widths and TSV diameter in [11], multiple local vias in [16], and TSV redundancy in [17]) for TSV EM reliability improvement. However, these techniques ignored the EM recovery effect during the optimization of 3D PDN design.

III. Novel three-phase EM model for TSVs

EM is a physical phenomenon that mental atoms migrate along a direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate along the trajectory of conducting electrons. Due to momentum exchange between lattice atoms, hydrostatic stress is generated with the migration process. Void and hillock formation is caused by conducting electrons at the opposite ends

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of the wire when stress reaches critical level and make the wire fail when they are large enough.

As reported in [9], TSV failure process consists of three phases in general. The first phase is nucleation phase. When TSV is stressed by currents, the stress will be developed in the feeding metals (the top or bottom metals connecting the TSV). Taking down-stream configuration for example, in which case the electrons flow from TSV to the bottom metal, cathode node is the M_{BOT} segment close to interface of TSV/barrier layer. When the tensile stress is larger than the critical stress, void will be nucleated there. Time from $t = 0$ (when the wire is stressed at $t = 0$) to the moment when stress reaches the critical level t_{nuc} (nucleation time) is defined as the *nucleation phase*. For TSV, it was reported that the initial stress due to the thermo-mechanical stress can be significant [8], [18]. As a result, non-zero initial stress has to be considered in the model of nucleation phase.

The second phase is incubation phase. After the void formed, it starts to grow to a larger size. However, the resistance of TSV (with its feeding metals) does not change right away. It starts to increase when the void becomes larger than the TSV conductive section since it forces the electrons to flow through the high resistive TiN barrier as shown in Figure 3. We define the time from t_{nuc} to the moment of resistance change, t_i(incubation time), where the *incubation phase* (or *latency phase*) starts.

The third phase is growth phase. After incubation phase, resistance of TSV will change over time as shown in Figure 4 [15]. But it is observed that the resistance change versus time is not linear [9], which is quite different than the copper damascene wires. Resistance changes versus time of it is thought to be linear [19], [20]. This period after t_i is defined as *growth phase*. As a result, we need to develop a new EM model for the three phases, which will be presented in the following subsections.

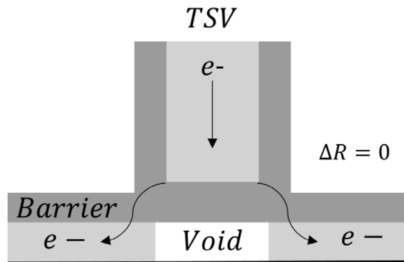

Figure 3: Void smaller than TSV section - no resistance increase.

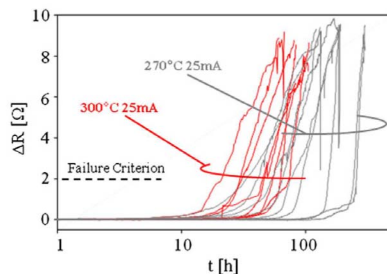

Figure 4: TSV resistance changes over time, courtesy of [15].

A. Nucleation phase modeling considering non-zero initial stress

For nucleation phase modeling of TSVs, non-zero, arbitrarily distributed initial stress in the feeding metal, for example in Figure 5 [21], need to be considered. However, existing compact models [20], [22] can not consider the arbitrary distributed initial stress. In this section, we propose a novel EM stress compact model considering non-zero initial stress and time-varying current density.

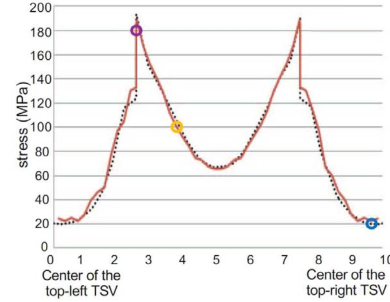

Figure 5: The initial stress from thermo-mechanical stress of a TSV, courtesy of [21].

The stress development in a confined metal with material block conditions can be described by the well-known Korhonen's equation [23]:

$$\frac{\partial\sigma(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[\kappa(\frac{\partial\sigma(x,t)}{\partial x} + G(t))\right] \tag{1}$$

In this equation, $\sigma(x,t)$ stand for the stress at corresponding position and time. The diffusivity κ is taken to have the form: $\kappa = \frac{D_a B\Omega}{kT}$,where B is the bulk modulus, Ω is the atomic volume, D_a is the effective atomic diffusivity which can be expressed as : $D_a = D_0 \exp\left(-\frac{E_a}{kT}\right)$, where D_0 is the pre-exponential factor, E_a is the activation energy, k is Boltzmann's constant. T is the absolute temperature, which affects the thermal energy of the atoms leading to the increase of the diffusivity. $G(t)$, which is the electronic driving force, can be written as

$$G(t) = \frac{Eq^*}{\Omega} = \frac{e\rho|Z^*|j(t)}{\Omega} \tag{2}$$

where the effective charge $q^* = |Z^*|e$ is a known quantity, e is the electric charge. ρ, Z^*, Ω stand for the product of the resistivity, the effective charge number, and the atomic volume, respectively. $j(t)$ is the time-varying current density, which can be a function of time. In our problem, $G(t)$ is only function of time, not the distance x as we only look at EM problem for one feeding metal segment wire as shown in 3. For nucleation phase, atomic flux at the terminals are blocked, i,e.,

$$(\frac{\partial\sigma(x,t)}{\partial x} + G(t))|_{x=0,x=L} = 0 \tag{3}$$

which is the boundary condition for (1).

For TSVs, study shows that the thermo-mechanical stress can be quite significant [21], which means that we have following initial condition to consider:

$$\sigma(x,0) = g(x) \tag{4}$$

Note that the initial stress is function of distance x in general. Then the Korhonen's equation, the boundary conditions and initial stress conditions of $\sigma(x,t)$ can be expressed in the following partial

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differential equation (PDE) form:

$$\begin{cases} \frac{\partial\sigma(x,t)}{\partial t} - \kappa\frac{\partial^2\sigma(x,t)}{\partial t^2} = 0, \ 0 \le x \le L, t > 0 \\ \frac{\partial\sigma(0,t)}{\partial x} = G(t), \qquad t > 0 \\ \frac{\partial\sigma(L,t)}{\partial x} = G(t), \qquad t > 0 \\ \sigma(x,0) = g(x), \qquad 0 \le x \le L \end{cases} \tag{5}$$

By using the Green's function method, PDE (5) with given boundary and initial conditions, can be solved exactly and the solution is given as:

$$\begin{aligned} &\sigma(x,t) = \sigma(x,0) \\ &+ \frac{2}{L}\int_0^L \sum_{n=1}^{\infty}\left[\cos\frac{n\pi x}{L}\cos\frac{n\pi\xi}{L}e^{-\frac{n^2\pi^2}{L^2}\kappa t}g(\xi)\right]d\xi \\ &+ \kappa\frac{4}{L}\int_0^t \sum_{n=1}^{\infty}\left[\cos\frac{(2n-1)\pi x}{L}e^{\frac{(2n-1)^2\pi^2}{L^2}\kappa(\tau-t)}G(\tau)\right]d\tau \end{aligned} \tag{6}$$

The second sub-item stand for the response from the position-related initial condition and the third sub-item stand for the response from the boundary conditions. Since this function can take care arbitrary distributed initial stress and time varying current density, it is suitable for TSV EM analysis for nucleation phase.

As a result, the nucleation time t_{nuc} is computed when $\sigma(cathode, t_{nuc}) = \sigma_{crit}$. Also practically, we only need take a few hundred terms in (6) to get the accurate results.

We first show the results and comparison for the proposed EM nucleation model. Figure 6 shows the EM stress development calculated by the new EM model, with non-uniform initial stress and time-invariant condition, where initial stress value is a cosine function with position as $8 \times 10^7 \times \cos(\frac{4\pi}{L}x)Pa$. We choose three representative time points:$t = 1 \times 10^6 s, 3 \times 10^6 s$ and $5 \times 10^6 s$ to show the degree of fitting between proposed stress model and COMSOL results.

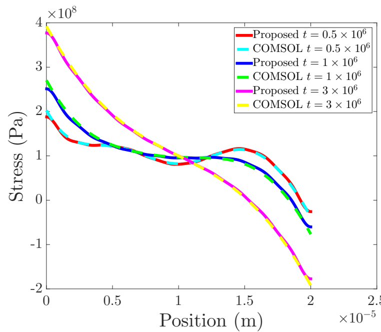

Figure 6: Comparison results under a non-uniform initial stress.

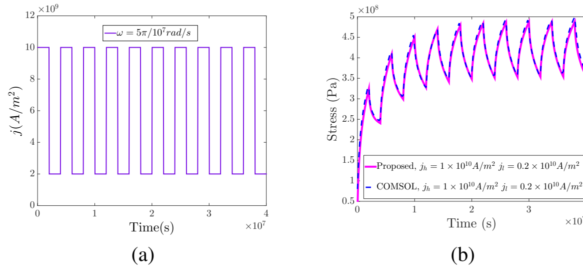

Figure 7: (a) Square wave used in experiments.(b) Stress recovery results by analytical solution loaded with square wave.

Figure 7(b) shows that the stress recovery effects from the proposed EM model, which was not presented in the existing TSV models [9]. We also use the square wave of $j_h = 1 \times 10^{10}\ A/m^2$, $j_l = 0.2 \times 10^{10}\ A/m^2$as shown in Figure 7(a) to stress the TSV. As we can see, when the current density goes down, the stress also goes down, which can help extend the life time of the TSVs and the whole circuit if recovery effects are explored.

B. The Incubation and growth phases models for TSVs

Once the void nucleated, it starts to grow. We follow the similar idea in [10] for the incubation and growth phase and that work will be reviewed in this part. In this case, voids are assumed to be quasi-cylindrical shapes during growth. It is located under the TSV as shown in Figure 8 with a radius of the void (r_{void}) and copper thickness. Measurable resistance increase will occur when r_{void} becomes larger than the radius of the TSV r_{TSV}. Resistance increase is relative to the radial length of barrier ($r_{void} - r_{TSV}$), through which electrons have to flow as void grows.

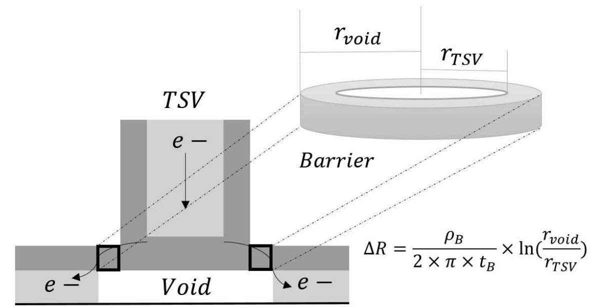

Figure 8: Void larger than TSV section - logarithmic resistance resistance.

We assume that the atomic flow induced by the electron wind can be expressed as (the backflow induced by the gradient of matter concentration can be ignored)

$$\Gamma_{EM} = \frac{eZ}{\Omega}\rho j \tag{7}$$

So the volume of atomic matter V_M depleted by electromigration along whole line at the instant t can be expressed as:

$$V_M(t) = \int_0^t \Gamma_{EM}dt = \Gamma_{EM}t \tag{8}$$

Assuming that the ratio of vacancy flow captured by the main void over the whole vacancy flow is constant for given time and stress conditions, then void volume is

$$V_{void} = \alpha\Gamma_{EM}t, \alpha \in [0,1]\ ,\ d\alpha/dt = 0 \tag{9}$$

where α is the portion of atomic flow contributing to the void growth. If we claim that the void growth under the TSV is isotropic in the plane, that is to say, r_{void} is equal in all directions. So the void volume is expressed as

$$V_{void} = \pi r_{void}^2 T_{Cu} \tag{10}$$

where T_{Cu} is the copper thickness of the pad and line. As a result, we have

$$t_1 = \frac{T_{Cu}\pi r_{void}^2}{\alpha F} \tag{11}$$

where t_1 the time passed after void nucleated, i.e., $t = t_{nuc} + t_1$. Due to the isotropic nature, we can treat the cylindrical shape of the barrier as one-dimensional wire as current flows along the radius

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direction. Once the void is larger than TSV section, the resistance increase dR can be represented as

$$dR = \rho_B \frac{dr_{void}}{2\pi T_B r_{void}} \tag{12}$$

where T_B is the thickness of the barrier, ρ_B is the specific resistance of the barrier. As a result, the resistance increase becomes

$$R(r_{void}) - R_0 = \int_{r_{TSV}}^{r_{void}} dR = \frac{\rho_B}{2\pi T_B} ln(\frac{r_{void}}{r_{TSV}}) \tag{13}$$

Since the t_i has the quadratic relationship with the void radius r_{void}, we then can represent the resistance changes as

$$R(t) - R_0 = \frac{\rho_B}{2\pi T_B} ln(\frac{\sqrt{t_1}}{\sqrt{t_i}}) = \frac{\rho_B}{4\pi T_B} ln(\frac{t_1}{t_i}),\ t_1 > t_i \tag{14}$$

$t_i = \frac{T_{Cu}\pi r_{TSV}^2}{\alpha F}$ is the incubation time, the critical time when void grows larger than TSV pad.

Then the total time for the whole EM failure process is $t = t_{nuc} + t_1$. The void will nucleate at t_{nuc}, the resistance of TSV will not change until $t_{nuc} + t_i$. After this the resistance of TSV will change over time. But the resistance changes over time indeed are not linear as shown in (14). Figure 9 shows the calculated TSV resistance changes from our new EM model, which is close to the experimental data in [10].

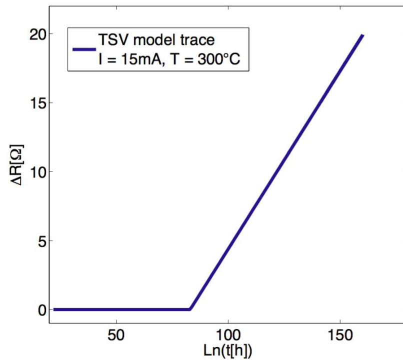

Figure 9: TSV resistance trace described by proposed model.

IV. Recovery-aware P/G TSV Repair

A. Motivation & basic idea

In the conventional approach, P/G TSV EM reliability can be improved by increasing its diameter (upsizing) [11]. This way, the current density within each TSV can be reduced, which is a major contributor to EM degradation. This so-called "TSV sizing" technique can improve EM-related lifetime at the cost of increased routing area consumption. As opposed to increasing the size of P/G TSV size, the proposed approach mainly focuses on the EM recovery effect. This is done by placing more TSVs with smaller diameter (as shown in Figure 10), consuming the same silicon area. Afterwards, by periodically deactivating a subset of P/G TSVs, the onset of EM failure can be delayed due the recovery effect, which significantly extends the effective TSV lifetime. At the same time, the subset of activated P/G TSVs can satisfy *ab initio* voltage drop constraints of 3D PDN.

The proposed repair approach is based on two stages. At design-time, the entire P/G TSV grid is partitioned uniformly into several tiles under the constraints of EM lifetime and 3D PDN voltage drop. The corresponding partitioning algorithms will be discussed in Section IV-B. Afterwards, the TSVs in each group are deactivated on

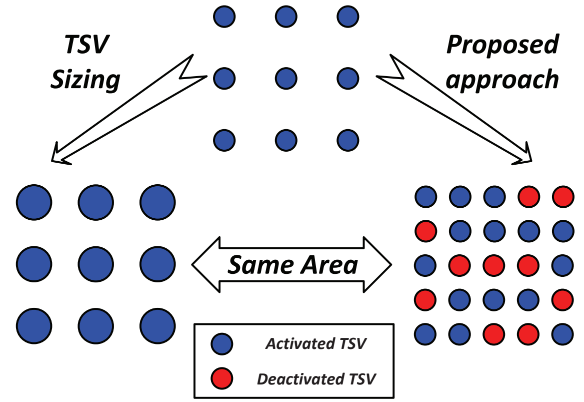

Figure 10: Illustration for the motivational example.

a rotating basis and recover from EM wear-out well before failing. In this work, a periodic recovery schedule is used, in which EM recovery can occur at regular time intervals. The detailed implementation and design consideration will be presented in Section IV-C.

B. Design-time TSV partitioning

Given an $m \times n$ TSV grid $\mathbf{T}$ containing N_T TSVs, the objective of this stage is to partition $\mathbf{T}$ into tiles, which is of the same fixed sizes. More specifically, the rows and columns of $\mathbf{T}$ are partitioned into $u \times v$ disjoint uniform intervals, which induces $N_t = uv$ tiles from the $u \times v$ partitioning (as shown in Figure 11). Therefore, each tile contains N_T/N_t TSVs, and one TSV in each tile will be deactivated on a rotating basis at run-time. As a result, there are $(N_T - N_t)$ activated TSVs at any given time. In order to satisfy the constraints of EM reliability and voltage drop simultaneously, the number of activated TSVs, which depends on the number of partitioned tiles, should be determined carefully.

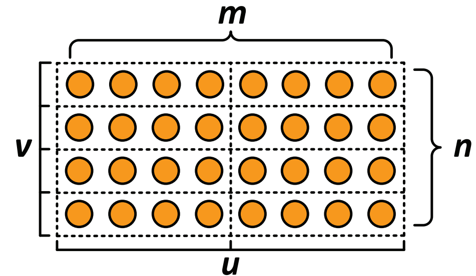

Figure 11: A $m \times n$ TSV grid is partitioned into $u \times v$ tiles uniformly.

1) Voltage drop-constrained partitioning: Since each TSV needs to be periodically deactivated during field-operation, it is necessary to guarantee a sufficient number of activated TSVs for reliable power supply. Due to the periodical switching between ON/OFF states of each TSV, $(N_T - N_t)$ TSVs are activated as power delivery paths at any given time. As a result, the upper bound on the number of partitions, $N_t^{\max}$, (i.e., the lower bound on the number of activated TSVs which guarantees to satisfy the constraints of voltage drop) should be determined.

In this work, we propose a greedy algorithm to obtain this upper bound value on the number of partitions which is required to satisfy the given constraints of IR-drop (as shown in Algorithm 1). Based on the power consumption of each standard cell (contained in $\mathbf{P}$) and its location (contained in $\mathbf{X}$), the power weight (PW) of each power node (i.e., TSV location candidate contained in $\mathbf{C}$) can be estimated [17]. Here, PW is a metric indicating the importance of

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each TSV location candidate on voltage drop, and placing TSV at the candidate location with larger PW can impact the voltage drop more significantly. Afterwards, an incremental TSV placement is performed, in which the TSV in each iteration is placed at the power node with the existing minimum importance. Since the worse-case scenario is considered here (i.e., always placing TSV at the power node with the minimum importance), the obtained activated TSV count can guarantee the constraints of voltage drops at any given time. Consequently, the upper bound on the number of partitions can be estimated under the voltage-drop constraints.

Algorithm 1 Iterative method for estimating low bound of activated TSV number N_{LB}

Input: $\mathbf{C}$, $\mathbf{X}$, $\mathbf{P}$, $\text{IR}_{\text{constrainted}}$
Output: N_{LB}
1: **for** $\forall$ candidate $c_i \in \mathbf{C}$ **do**
2: **for** $\forall$ cell $x_j \in \mathbf{X}$ **do**
3: calculate distance D_{ij} between c_i and x_j;
4: $PW_{ij} = p_j / D_{ij}$;
5: **end for**
6: $PW_i = \sum_j PW_{ij}$;
7: **end for**
8: Sort $\mathbf{C}$ in ascending order according to PW;
9: $N_{LB} = 0$;
10: **repeat**
11: place TSV at $c_0 \in \mathbf{C}$;
12: N_{LB}++;
13: delete the selected candidate in $\mathbf{C}$;
14: calculate the existing IR-drop of 3D PDN $\text{IR}_{\text{existing}}$;
15: **until** $\text{IR}_{\text{existing}} \leq \text{IR}_{\text{constrainted}}$
16: **return** N_{LB}

2) Reliability-constrained partitioning: In order to improve EM reliability effectively, each TSV should be guaranteed sufficient recovery time. Since a periodic recovery schedule is used in this work, EM recovery can occur at regular time intervals. As a result, the recovery time of each TSV is highly dependent on the size of each partitioned tile. According to the TSV count in each tile N_T/N_t, each repair cycle can be split into multiple sub-cycles uniformly. Therefore, for each TSV, the deactivated time (i.e. recovery time) is equal to:

$$\frac{N_t}{N_T} T_{\text{cycle}} \tag{15}$$

in each recovery cycle. Here T_{cycle} is the duration of each repair cycle, which is a user-defined parameter. According to Equation (15), the entire TSV grid cannot be partitioned into too few tiles (i.e., small N_t) in order to provide sufficient recovery time, and the lower bound on the number of partitions, $N_t^{\min}$, needs to be determined according to the given T_{cycle}. This lower bound value can be estimated using the proposed TSV EM model in Section III. Given a set of representative workloads, we can generate the power/thermal characteristics of each TSV by power and temperature analysis, and then estimate its EM-related lifetime without the consideration of recovery effect. Afterwards, the TSV with the lowest recovery-unaware lifetime can be selected to estimate the lower bound of N_t. The recovery time of this TSV is increased from T_{cycle}/N_T to $N_t T_{\text{cycle}}/N_T$ until satisfying the given requirement of EM-related lifetime. Consequently, the lower bound of N_t can be determined under the constraints of EM reliability by considering worst-case scenario (i.e., targeting the TSV with the minimum lifetime). Note that, since we look into large time scales for EM recovery periods in this work, here a steady-state temperature analysis is enough.

After obtaining the lower and upper bounds, the number of partitioned tiles is within these bounds [1]. In case there are multiple values in this range, the Pareto-optimal points can be identified within the bounds based on reliability and performance constraints.

3) Discussion: So far we have considered uniform tiling and as a result, the deactivated TSVs are uniformly distributed in the grid. However, a non-uniform partitioning could be more efficient for EM reliability improvement. This means that the size of each tile can be decided based on the power and thermal profile of the grid, so there will be more activated TSVs in power-hungry regions. We plan to investigate non-uniform tiling in our future work.

C. Run-time TSV repair

After obtaining the TSV tiles at design-time, a repair architecture that enables periodic deactivation of TSVs should be implemented within each tile. In order to leverage the recovery effect for EM reliability improvement, each TSV needs to be provided with dedicated shut-off time in the field. To this end, transistor switch is equipped with one terminal of TSV, connecting to global power mesh (as shown in Figure 12). Similar to 2D planar technologies, sleep transistors with high-threshold voltage can be utilized to achieve the power gating in 3D ICs [24]. In this work, the sleep transistor can be used to control the ON/OFF state of each TSV for activation/deactivation, respectively. Moreover, since the periodical recovery schedule can be fixed at design-time, it is unnecessary to control the sleep transistors from outside. Instead, a small finite-state machine can generate the control signal internally.

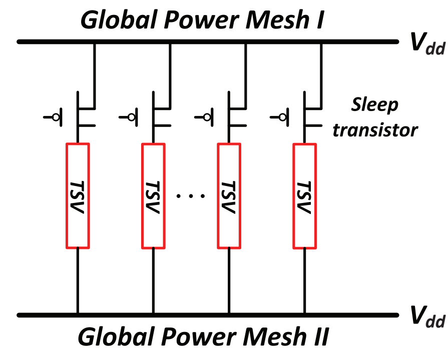

Figure 12: Illustration for the hardware implementation of repair architecture.

Since a periodical recovery scheduling is considered in this work, all partitioned tiles can share the same finite-sate machine for generating control signal. Therefore, the area overhead introduced by this repair solution is dominated by the sleep transistors, which are equipped with each P/G TSV. For a single sleep transistor, the typical physical area is in the range between 0.45-18 μm^2 for 45 nm technology [25]. Due to the large resistance of an active sleep transistor, an extra voltage drop can be observed between the global power grid and TSV, resulting in a delay penalty. Therefore, in order to achieve a smaller voltage drop, a larger sleep transistor is conventionally preferred to introduce less resistance on the power supply path. On the other hand, a larger sleep transistor produces higher in-rush current during the wake-up process, and occupy similar

[1] Without loss of generality, N_t is always decomposed into $u \times v$, in which $u \leq v$ and $|u - v|$ is minimal.

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silicon area as TSV. In order to reduce the area overhead introduced by the sleep transistor, we assume a smaller transistor size in this work. The penalty is the increased sleep transistor-induced voltage drop, accompanied with performance degradation. However, this penalty is unavoidable since the EM-induced timing failures can be more severe without the proposed repair solution.

V. Numerical results and discussions

A. Simulation setup and implementation flow

For our simulations, six 3D benchmark designs selected from OpenCore benchmark suite [26] were used, including *des_perf–i*, *cf_rca_16–i*, and *cf_fft_256_8–i* $(\mathrm{i}=2,4)$. Here, i is the number of stacked dies in each design. For P/G TSV, its resistance R_{TSV} can be divided into two parts: DC resistance R_{DC} and contact resistance R_{contact}. Here, R_{DC} and R_{contact} can be calculated as [27]

$$R_{\mathrm{DC}} = \rho \frac{h_{\mathrm{TSV}}}{\pi r_{\mathrm{TSV}}^2} \tag{16}$$

and

$$R_{\mathrm{contact}} = \frac{\rho_c\left(N_a\right)}{2\pi r_{\mathrm{TSV}} h_{\mathrm{TSV}}} \tag{17}$$

respectively. The definition and the relevant value of each parameter in Equations (16) and (17) are listed in Table-I. In addition, the detailed information about the benchmarks, including footprint, power consumption, and 3D PDN design, etc., are listed in Table-II.

Table I: Experimental setting for P/G TSV.

Item	
TSV radius r_{TSV} $(\mu\mathrm{m})$	2.5 [28]
TSV height h_{TSV} $(\mu\mathrm{m})$	50 [28]
Cu resistivity ρ $(\mathrm{n}\Omega \cdot m)$	16.8 [28]
Contact resistivity $\rho_c\left(N_a\right)$ $\left(\Omega \cdot \mu m^2\right)$	0.45 [28]

The basic implementation flow is as follows. First, based on the given netlist of each die, Cadence SoC Encounter was used to perform placement for all the dies in each design separately using the Nangate 45 nm library [29]. In the floorplan, P/G and signal TSVs were placed regularly. Afterwards, the proposed P/G TSV partitioning technique was conducted on the generated layout files of each design to obtain TSV tiles. Based on a periodic recovery schedule with a user-defined T_{cycle}, the recovery-aware EM-related lifetime can be estimated by the developed TSV EM model. To this purpose, the power/thermal characteristics of each P/G TSV need to be generated. After creating a top-level Verilog netlist for the design, post-synthesis simulation was performed in Modelsim with a testbench containing 10^5 random input vectors. The generated switching activity interchange format (SAIF) file was forwarded to Power Compiler in order to obtain the power consumption of each cell. By the static analysis of 3D PDN, the voltage drop on each P/G TSV ΔV_{TSV} can be estimated, then the current density is obtained by $j_{\mathrm{TSV}} = \Delta V / R_{\mathrm{TSV}} \pi r_{\mathrm{TSV}}^2$. In addition, based on the generated power profile and layout files, the experienced temperature of each TSV can be estimated using the 3D Hotspot [30]. Note that, since TSV rotation is local and evenly distributed within tile, the change in power and temperature due to periodic deactivation can safely be ignored during run-time repair.

During TSV partitioning, the IR-drop constraint is set as 10% voltage drop in average, and the EM failure criteria is set as 10% increase in resistance. Until the number of non-faulty TSVs is less than the lower bound of required TSV count for satisfying IR-drop constraint, the entire TSV grid is considered as reliable and the corresponding EM-induced lifetime is reported.

B. Comparison with prior works

We compare our proposed recovery-aware repair approach with the conventional recovery-unaware technique [11], and the results in terms of EM-related lifetime, average IR-drop, and area overhead are listed in Table III. In the baseline approach, P/G TSVs are placed uniformly with the parameters listed in Table-I. In order to improve the EM reliability of TSV grid, we assumed that the radius of each TSV is increased to $2 \times r_{\mathrm{TSV}}$, but the pitch is the same as the baseline. According to simulation results, the average IR-drop can be reduced by the decreased resistance of larger TSV (35.24% in average). However, the achieved EM-related lifetime is still unacceptable even applying the recovery-unaware "TSV-sizing" technique. On the other hand, the proposed recovery-aware approach places the P/G TSVs with smaller radius ($0.5 \times r_{\mathrm{TSV}}$ in this work) but increased number (16 times in this work). This way, the area overhead introduced by P/G TSVs is the same between the recovery-unaware and recovery-aware approaches. However, by leveraging recovery effect, the proposed approach can extend EM-related lifetime by 4.4X in average compared with the conventional recovery-unaware one. Here the duration of each repair cycle T_{cycle} is set to 1,000 seconds. Moreover, the average IR-drop can be reduced further due to the increased number of placed TSVs (28.87% in average). The penalty of the proposed approach is the extra area overhead introduced by the sleep transistors. However, according to our simulation results, the increased area overhead introduced by the proposed repair solution (i.e., sleep transistors) is pretty small (0.20% in average compared to the recovery-unaware technique), which can be negligible for a large design.

VI. Conclusion

In this paper, we propose a novel repair approach based a three-phase TSV EM model to combat electromigration (EM) in power/ground (P/G) Through-silicon-vias (TSVs) by taking use of the recovery effect. Applied to 3D benchmark designs, our proactive approach improves the lifetime reliability of P/G TSVs susceptible to EM failure by approximately 4.4X over the conventional reactive one based on upsizing with negligible area overhead. While our methodology with even simple recovery scheduling significantly improves TSV lifetime reliability, more sophisticated recovery scheduling can be studied in future in order to further enhance EM reliability.

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Table II: Design Statistics for all benchmark.

Benchmark	Footprint (μm^2)	Power (mW)	# P/G TSVs	Mesh Granularity
des_perf–2	51,076	63.5	25	40×40
des_perf–4	25,600	64.7	48	48×48
cf_rca_16–2	230,400	172.5	64	64×64
cf_rca_16–4	129,600	175.2	192	64×64
cf_fft_256_8–2	722,500	491.2	196	112×112
cf_fft_256_8–4	360,000	496.1	432	96×96

Table III: Comparison between the proposed recovery-aware approach and the conventional recovery-unaware approach [11]. Here ΔA is the percentage of area introduced by repair solution with respect to total chip area ($T_{\text{cycle}} = 1,000s$), and Δ_{avg} is the difference of each metric between different approaches (i.e., B/L: baseline; R-U: recovery-unaware; R-A: recovery-aware) in average.

Benchmark	ΔV_{dd}^{avg} (mV)			Lifetime (yrs)			ΔA (%)	
	B/L	R-U [11]	R-A	B/L	R-U [11]	R-A	R-U [11]	R-A
des_perf–2	99.73	76.38	64.14	1.36	6.43	12.93	1.44	1.62
cf_rca_16–2	115.55	92.80	82.10	0.93	4.80	10.30	2.76	3.10
cf_fft_256_8–2	106.59	84.92	39.95	0.21	1.28	4.31	0.82	0.92
des_perf–4	215.80	115.65	97.92	0.26	0.97	5.21	2.18	2.45
cf_rca_16–4	155.86	76.46	48.05	0.30	1.73	10,01	0.80	0.90
cf_fft_256_8–4	195.64	96.58	57.74	0.13	0.59	4.57	1.77	1.99

Δ_{avg}	R-U vs B/L	R-A vs R-U	R-U vs B/L	R-A vs R-U	R-A vs R-U
	35.24% (improvement)	28.87% (improvement)	5.0X	4.4X	0.20% (overhead)

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