Voltage-Based Electromigration Immortality Check for General Multi-Branch Interconnects

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ABSTRACT

As VLSI technology features are pushed to the limit with every generation and with the introduction of new materials and increased current densities to satisfy the performance demands, Electromigration (EM) is projected to be a key reliability issue for current and future VLSI technologies. Existing EM signoff mainly relies on current density-based assessment using Black's equation and Blech product. This model does not work well for multi-branch interconnect wires as the stresses developed in each wire segment is not independent of one another. In this paper, we present a novel and fast EM Immortality check for general multi-branch interconnect trees. Instead of using current density as the key parameter as in traditional methods, the new method estimates the EM-induced stress in general multi-branch interconnects based on the terminal voltages or potentials. It can be viewed as the *Blech product* for multi-branch interconnects for fast check of EM immortality of wires. Besides, this voltage-based EM (VBEM) assessment technique can naturally comprehend the impact of the topology of the wire structure on EM-induced stress. As a result, this new VBEM analysis method is very amenable to EM violation fixing as it brings new capabilities to the physical design stage. The VBEM stress estimation method is based on the fundamental steady-state stress equations. This approach eliminates the need for complex look-up tables for different geometries and can be implemented in CAD tools very easily as we demonstrate on real design examples. We show that its solution is consistent with the physics-based dynamic EM stress evaluations from the numerical analysis by COMSOL.

1. INTRODUCTION

Reliability has become a major design challenge and limiting factor for nanometer VLSI designs. Electromigration (EM) is the major failure mechanism for metal wires. It was predicted that EM failure will become more significant for interconnects in FinFET based technologies at 10nm and beyond due to increased current density and elevated heating. Traditional compact EM checking approaches such as Black's equation [1] and Blech product [2] can lead to significant over design [3]. These conservative over-design rules are not suitable for future technology scaling since more design guard bands are required for chip timing accuracy, thus such a worst-case design methodology results in inefficiency and considerable penalties in the area, performance, power, and reliability budgets. Existing EM signoff mainly relies on current density-based assessment using the very conservative Black's model. Such a model does not work well for multi-branch interconnect wires as the stresses developed in each wire segment are not independent of one another. As a result, more accurate EM modeling and analysis are required for complicated interconnect wires commonly seen in the power grid and clock networks on a chip.

Existing EM modeling and analysis techniques mainly focus on the simple straight line interconnect with two line end terminals. However, a practical integrated circuit layout often has interconnects such as clock and power grid networks with more complex structures, which typically consist of multi-branch metal segments representing a continuously connected, highly conductive metal (Cu) lines within one layer of metallization, terminating at diffusion barriers. The EM effects in those branches are not independent and they have to be considered simultaneously. Currently employed Blech length [2] (for the elimination of immortal segments) and Black's equation [1] mainly target single wires. They ignore the geometry and topology impacts on the EM failure effects.

To mitigate those problems, recently some physics-based EM analysis methods for through-silicon via (TSV) and power grid networks have been proposed based on solving the basic mass transport equations [4–7]. Those models treat the resistance changes of a wire over time as the atomic concentration changes due to atomic flux. Since these proposed methods solve the basic mass transport equations using the finite element method, they can only solve for very small structures such as one TSV structure. A complicated look-up table or models have to be built for different TSVs and wire segments for full-chip power grid analysis at reduced accuracy. Alternatively, a more compact physics-based EM model was proposed recently in [8]. It is based on the hydrostatic stress diffusion equation [9]. The new model is

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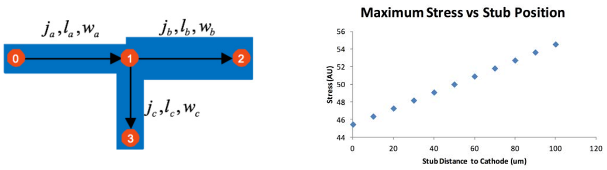
mainly derived from a single wire. It can consider many geometry parameters like wire lengths, residual stress. The new physics-based model was also extended to consider the multi-branch interconnects based on the projected steady-state stress. But complicated equations have to be solved based on the current density of each branch. Recently, a compact EM model which can provide the time-dependent hydrostatic evolution of hydrostatic stress for multi-branch interconnect wires has been proposed [10]. But this model can only deal with a limited number of interconnect structures and cannot deal with general interconnect topologies.



(a) (b)

Figure 1: (a) Illustration of T-junction interconnect with directed graph inserted to indicated electron flow. (b) Stress at cathode end increases linearly as the stub is placed further away from the cathode end

To further illustrate wire topology impacts on the EM-induced stress, Fig. 1 shows a T-shaped wire with the wire 3 as a stub. If one changes the stub location of the wires as shown in Fig. 1(a) (branch (1,3) is a stub if $j_c = 0$), the projected steady state stress (maximum stress the wire can reach in steady-state) will change noticeably as shown in Fig. 1(b). As one can see, the location of the stub in the wire can change steady-state stress at the cathode node significantly.

In this paper, we propose a novel and fast EM Immortality check for general multi-branch interconnect trees with DC current. Instead of using DC current densities as the key parameter in traditional methods, the new method estimates the EM-induced stress of general multi-branch interconnects based on the terminal voltages or potentials. Our new contributions lie below:

- We show that the new method can be viewed as the *Blech product* for multi-branch interconnects for fast check of EM immortality of wires and EM signoff analysis.
- We show that the voltage-based EM (VBEM) assessment technique can naturally comprehend the impact of the topology of the wire structure on EM-induced stress as it does not consider the branch related information such as branch currents anymore. This new VBEM analysis method is very amenable for EM violation fixing as it brings new design capabilities into the physical design stage. The new voltage-based EM stress estimation method is based on the fundamental stress steady-state equations.

This approach eliminates the need for complex look-up tables for different geometries and can be implemented in CAD tools very easily as we demonstrate on real design examples. Our experimental results show that the new method is consistent with the physics-based dynamic EM stress evaluations from the numerical analysis by COMSOL.

2. EM PHYSICS AND STRESS MODELING

EM is a physical phenomenon of the migration of metal atoms along a direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate toward the anode end of metal wire along the trajectory of conducting electrons. During the migration process, hydrostatic stress generated inside the embedded metal wire due to momentum exchange between lattice atoms and conducting electrons is a prime cause of void and hillock formation at the opposite ends of the wire. Indeed, when metal wire is embedded into a rigid confinement, which is the case with interconnect metallization, the wire volume changes (induced by the atom depletion and accumulation due to migration) create tension at the cathode end and compression at the anode ends of the line. Over time, the lasting unidirectional electrical load will increase hydrostatic stress, as well as the stress gradient which acts as counter-forces for atomic migration along the metal line. In some cases, usually, when a line is long, this stress can reach a critical level, resulting in a void nucleation at the cathode and/or hillock formation at the anode end of line.

Specifically, let $\sigma(x)$ denote the stress at location x, the atomic flux, Γ_σ, caused by the inhomogeneous distribution of the hydrostatic stress is [9]

$$\Gamma_\sigma = \frac{D_a}{kT}\frac{\partial \sigma}{\partial x} \tag{1}$$

The atomic flux flowing toward the anode caused by electromigration effects, Γ_{EM}, can be described by

$$\Gamma_{EM} = \frac{D_a}{\Omega kT} eZ\rho j \tag{2}$$

where $D_a = D_0 exp(Ea/kT)$ is the effective atomic diffusivity, E_a is the activation energy of the failure process, T is the absolute temperature and k is the Boltzmann constant. Ω is the atomic lattice volume, where e is the electron charge, eZ is the effective charge of the migrating atoms, ρ is the wire electrical resistivity, j is current density.

2.1 Steady-state EM-induced stress modeling

At the steady state, the atomic flux becomes zero, which means that $\Gamma_\sigma = \Gamma_{EM}$. As a result, we have

$$\frac{\partial \sigma}{\partial x} = \frac{eZ\rho}{\Omega} j \tag{3}$$

On the other hand, the hydrostatic stress also leads to displacement of interconnect materials, which can be described as

$$\begin{aligned} \frac{\partial u}{\partial x} &= \alpha\sigma \qquad (4) \\ \sum_k u_{ik} w_{ik} &= 0 \qquad (5) \end{aligned}$$

where, u_{ik} is the displacement and w_{ik} is the width at k-th node on a branch between nodes i and k, and $M = 1/\alpha$ is the Young's modulus of the interconnect materials.

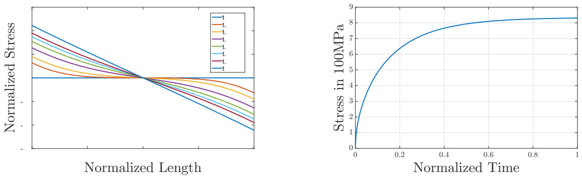
We note that equations (4) and (5) can be viewed as the atom conservation (in the sense that the total number of metal atoms will be keep the same during the migration process in the wire) in the stress kinetics. We notice that similar conservation equation was given in [8] for steady-state stress computation for multi-branch interconnects.

2.2 Transient EM-induced stress modelings

More complete modeling of transient hydrostatic stress evolution due to EM effects was proposed by Korhonen [9]. In this model, stress $\sigma(x,t)$ is described by Korhonen's equation:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma}{\partial x} + G\right)\right] \tag{6}$$

Here, $\kappa = D_a B \Omega / kT$, B is the effective bulk elasticity modulus, Ω is the atomic lattice volume. And $G = \frac{eZ\rho j}{\Omega}$, where e is the electron charge, eZ is the effective charge of the migrating atoms, ρ is the wire electrical resistivity, and j is the current density. Existing physics-based models are mainly based on the solutions of Korhonen's equation [8,10,11].



(a) (b)

Figure 2: (a) EM-stress distribution change over time in a simple metal wire. (b) EM-stress evaluation versus time

Fig. 2(a) shows stress development over time in a metal line with Korhonen's equation. Over time, tensile (the positive) stress will be developed at the cathode node (left node) and compressive (negative) stress will be developed at the anode (right) node. The stress changes polarity in the middle of the wire. The built-up stress (its gradient) will serve as the counterforce for atomic flux. Fig. 2(b) shows stress evolution on the cathode, which reaches a steady state over time. If the highest stress at the cathode node exceeds the critical stress, then voids will be created.

In this work, we first present the compact EM model based on the solution of steady-state modeling of EM effects, which lead to the voltage-based assessment for EM failures for interconnect trees. We show that VBEM assessment is more suitable for multi-branch interconnect trees. We compare the results from voltage-based VBEM with ones from dynamic EM models to validate the new VBEM models on some complex interconnect wire structures.

3. VOLTAGE-BASED EM STRESS ESTIMATION

In this work, we first present the formula to calculate the steady-state stress for any node in a multi-branch interconnect tree based on the terminal voltage. Then we discuss several special cases.

Figure 3: A three terminal wire and the direction indicate electron flow

One important observation is that the stress difference between two nodes at the steady state can be expressed in terms of voltage, instead of current density [12]. To demonstrate this, we can discretize (3) in space, if we ignore the initial or residual stress, leading to

$$\sigma_k - \sigma_i = \frac{eZ\rho}{\Omega} l_{ik} j = \frac{eZ}{\Omega} V_{ik} \tag{7}$$

where σ_k is the steady-state stress at node k, V_{ik} is the voltage or potential difference from node i and node k. When $V_{ik} > 0$, stress at node k is higher than the stress at node i (we assume that tensile stress is positive and compressive stress is negative). From (4) and (5), we have

$$\sum_k a_k \sigma_k = 0 \tag{8}$$

where a_k is the total area of branches connected to the node k. This equation represents the conservation in the stress kinetics. For instance, in the Fig. 3, the area for node 1 is $l_a w_a + l_b w_b$. For this case, (8) can be expressed as $l_a w_a \sigma_0 + (l_a w_a + l_b w_b)\sigma_1 + l_b w_b \sigma_2 = 0$. We also notice that for this case, we have

$$\sum_k a_k = l_a w_a + l_a w_a + l_b w_b + l_b w_b = 2(l_a w_a + l_a w_a) = 2A \tag{9}$$

where A is the total areas of the branches in the wire. By considering (7), we can compute the stress for any node i in terms of all the node voltages with respect to the node i:

$$\sigma_i = \frac{\beta}{2A} \sum_{k \neq i} a_k V_k^i \tag{10}$$

where $\beta = \frac{eZ}{\Omega}$, V_k^i is the nodal voltage at node k with respect to node i (node i is treated as the reference node).

If we select the reference node as the ground node (with zero voltage), then the stress at the ground node can be expressed as

$$\sigma_g = \frac{\beta}{2A} \sum_{k \neq g} a_k V_k \tag{11}$$

where, V_k is the normal nodal voltage (with respect to ground node g) at the node k in the wire. Note that the ground voltage typically is the lowest voltage in a wire (in case we have no negative voltages). The node typically is the cathode node in the segment a and its tensile stress σ_g is the largest one.

If we further define a virtual voltage that will generate the same stress at the ground node, σ_g, as

$$V_g = \frac{1}{2A} \sum_{k \neq g} a_k V_k \tag{12}$$

which can be viewed as *EM ground voltage*. Then according to (7), the stress at any node with nodal voltage V_i (with respect to ground node), can then be computed as [12]

$$\sigma_i = \beta(V_g - V_i) \tag{13}$$

This equation shows that the EM-induced stress at any node can be easily determined by the difference between the node voltage and the *EM ground voltage* for an interconnect tree. Therefore, EM stress determination is simplified to a problem of analyzing the node potentials and combining them with geometric information of the interconnect. Node potentials are readily available after circuit simulation and additional numerical solution is not required.

For EM effects, when the hydrostatic stress (EM-induced stress plus other existing stresses) at a node hits the critical stress, σ_{crit}, then the void starts to be nucleated and the resistance of the wire starts to increase over time, which can be measured experimentally [13,14]. Assume that initial or residual stress is σ_{init}, which is the same for all the nodes (this may not be true in general, but we have the assumption to simplify our presentation), then we can determine the voltage required for the nucleation to happen as

$$V_{crit} = \frac{\Omega}{Ze}(\sigma_{crit} - \sigma_{init}) \tag{14}$$

For a multi-branch wire, when it is stressed only by positive voltages, if $V_g < V_{crit}$, no wire will have EM failure as even the ground node (with the lowest voltage) will not fail in this case. Otherwise, EM failure may happen. For any nodal voltage V_i, one only needs to future check whether

$$V_{crit} > V_g - V_i \tag{15}$$

If this condition is meet for all the terminal voltages of the wire, then no EM failures will happen.

We note that if a wire fails the immortality check in (15), then more detailed and time dependent stress analysis are required to determine the time to failure or mean time to failure, which still remain a difficult problem for general multi-branch interconnect trees [10].

3.1 Relationship to Blech product

We show that the Blech product essentially is the voltage-based EM assessment for single wire. The proposed VBEM method actually can be viewed as the general extension of this technique to multi-branch interconnect wires.

Specifically, Let L be the length of a single wire and j is the current density of the wire. Starting the steady-state condition of EM stress shown in (3), which is also called *Blech condition*, if we integrate (3) along the line, we obtain

$$\sigma(x) = \sigma_{init} + \frac{eZ\rho j}{2\Omega}x \tag{16}$$

where, σ_{init} is the residual stress. The maximum tensile stress can be achieved at the cathode end of the wire ($x = L$).

If the critical stress that the wire can withstand is σ_{crit}, we can define the critical product for EM failure as

$$(jL)_c = \frac{2\Omega(\sigma_{crit} - \sigma_{init})}{eZ\rho} \tag{17}$$

which is called *Blech product* [2]. A wire is EM immortal if it satisfies $jL < (jL)_{crit}$. As a result, Blech product can help to identify all the immortal wires efficiently.

Notice the ρ is the resistivity, ρLj is actually the voltage across the wire, then (17) becomes

$$(Lj)_{crit} * \rho = V^b_{crit} = \frac{2\Omega(\sigma_{crit} - \sigma_{init})}{eZ}. \tag{18}$$

where V^b_{crit} is actually the critical voltage for this single wire. As we can see that this equation is almost the same as (14). If the stressing voltage of the wire is larger than this critical voltage, EM failure will happen. As a result, Blech product essentially is the voltage-based EM assessment method for a single wire.

3.2 Study of some special cases

In this subsection, we study three multi-branch interconnect structures to illustrate the proposed method. The three structures consist of straight-line 3 terminal wire in Fig. 4, the T-shaped 4 terminal wire in Fig. 7 and comb structure wire in Fig. 8. We stress that the proposed method can be applied to any multi-branch tree-structured interconnects.

3.2.1 *The straight-line 3 terminal wire*

Figure 4: Interconnect examples for EM analysis for Straight-line 3-terminal wire

The straight-line 3-terminal wire is shown in Fig. 4. In this wire, the node 0 is treated as the ground node. Note that current densities in two segments are j_a and j_b and may not the same which will be determined by the rest of the circuit. Then EM stress equation becomes:

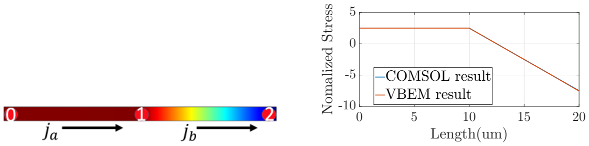
$$\begin{array}{lll} V_0 = 0, & A_0 = l_a w_a, & \sigma_0 = \beta V_g \\ V_1 = j_a l_a, & A_1 = l_a w_a + l_b w_b, & \sigma_1 = \beta(V_g - V_1) \\ V_2 = j_b l_b + j_a l_a, & A_2 = l_b w_b, & \sigma_2 = \beta(V_g - V_2) \end{array}$$

where

$$V_g = \frac{V_0A_0 + V_1A_1 + V_2A_2}{2A} = \frac{V_1A_1 + V_2A_2}{2A}$$

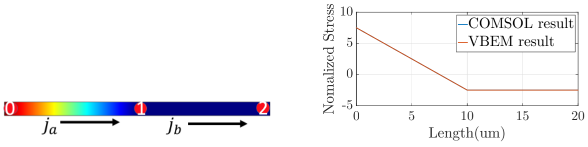
where $\beta = \frac{eZ\rho}{\Omega}$. Passive sink, active sink, passive reservoir and active reservoir configurations, described in [15], are a usual condition in the common interconnect tree.

Fig. 5 and Fig. 6 show the steady-state stress for the cases with passive reservoir (segment a with $j_a = 0$) and passive sink (segment b with $j_b = 0$). Here we define “passive” and “active” represent zero current density and nonzero current density respectively. The analysis will be focusing on mitigating the EM effect in the active segment. It can be observed from Fig. 5 that the passive reservoir (segment a) is characterized with higher stress compared with the active sink (segment b). Thus the void will first nucleate in the reservoir which can relax the EM effect in the sink. On the contrary, as shown in Fig. 6, the existence of passive sink (segment b) will lead to higher stress in the active reservoir (segment a), which accelerates the void formation thus EM failure in the reservoir. A comparison of the steady-state stress predicted by VBEM with the finite element analysis (COMSOL) simulation in both cases has demonstrated an excellent agreement.



(a) (b)

Figure 5: (a) 2-D stress distribution on wire at steady state for passive reservoir (b) EM-stress evaluation versus length at steady state



(a) (b)

Figure 6: (a) 2-D stress distribution on wire at steady state for passive sink (b) EM-stress evaluation versus length at steady state

3.2.2 *The T-shaped 4 terminal wire with stub*

The structure of the T-shaped 4-terminal wire has been shown in Fig. 7. In this case, we have three segments which connect through the middle node 1. Current density are j_a, j_b, and j_c on three branches. In this case, we make the branch c, the vertical branch the stub (its current density is set to zero, $j_c = 0$), then the EM stress can also be obtained:

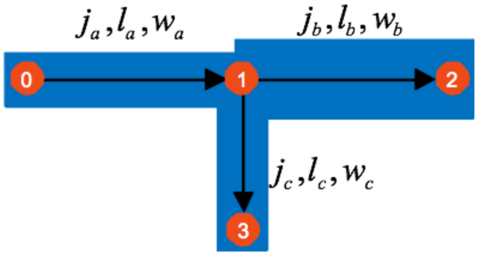


Figure 7: Interconnect examples for EM analysis for T-shaped 4-terminal wire

$$\begin{aligned}
V_0 &= 0, & A_0 &= l_a w_a \\
V_1 &= j_a l_a, & A_1 &= l_a w_a + l_b w_b + l_c w_c \\
V_2 &= j_b l_b + j_a l_a, & A_2 &= l_b w_b \\
V_3 &= j_a l_a + j_c l_c, & A_3 &= l_c w_c \\
\sigma_0 &= \beta V_g, & \sigma_1 &= \beta(V_g - V_1) \\
\sigma_2 &= \beta(V_g - V_2), & \sigma_3 &= \beta(V_g - V_3)
\end{aligned}$$

where

$$V_g = \frac{V_1 A_1 + V_2 A_2 + V_3 A_3}{2A}$$

The stub is acting as a sink when it approaches to anode and servers as a source when it is closer to cathode. The distance between stub and cathode and length of stub itself can be an important situation related to EM stress. As shown in Fig. 1(b), the when the stub is moved away from the cathode node (node 0), the stress at the cathode is increasing as it allows more atom to migrate to the stubs and thus create more tensile stress at the cathode node. This is a commonly seen structure in interconnect circuit design and EM analysis is necessary. We will discuss the effects of distance between the stub and the cathode as well as the length of the stub on EM stress. So by adjusting the stub location and length, we can actually adjust the stress at the cathode node to fix the EM failures in the physical design.

3.2.3 *The interconnect wires with comb structure*

Now, we study a more complicated interconnect structure, which is the comb or ladder structure as shown in Fig. 8.

In this comb-structured interconnect, we have N fingers, in which each finger structure is assumed to be the same. R_{sh} is the sheet resistance of the metal and I is the current along each finger. We assume that node 0 is still the ground node. L_B and W_B are the length and width respectively for the body structures, L_F and W_F are the length and width respectively for the fingers. i refers to i-th node on the body and i' is the node on the i-th finger.

The total area connected to node k, except node N, is A_k and total area connected to node k' is $A_k{}'$, total area connected to node N is A_N, and the total area of the whole comb structures, A, can be expressed as:

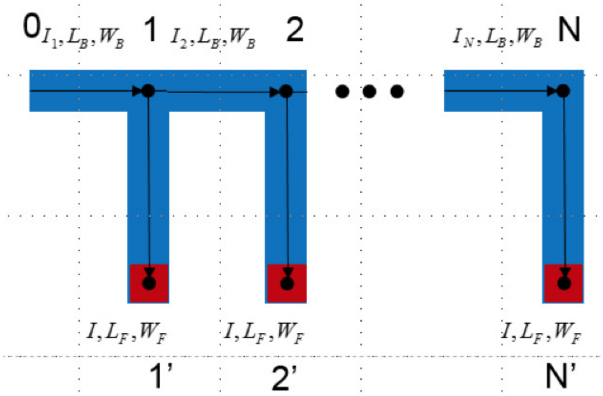


Figure 8: Interconnect examples for EM analysis for Comb Structure

$$\begin{aligned}
A_k &= 2W_B L_B + W_F L_F, & A_k{}' &= W_F L_F, \\
A_N &= W_B L_B + W_F L_F, \\
A &= N(W_B L_B + W_F L_F)
\end{aligned}$$

Note that since the N-th node is only connected with one part of the body structure, a total area connected with node N is different from other nodes. Since current flows in the same direction (which is opposite to the arrows in the figure), the highest EM tensile stress will be generated at node 0 since it has the lowest potential. Hence, in this case, we only need to check V_g against the critical stress.

The potential at each node for V_k and $V_k{}'$ can be obtained as:

$$\begin{aligned}
V_k &= \left[Nk - \frac{k(k-1)}{2}\right] \times I \times \frac{L_B}{W_B} R_{sh}, \\
V_k{}' &= V_k + I \times \frac{L_F}{W_F} R_{sh}
\end{aligned}$$

Finally, the EM stress of the comb structure can be obtained as:

$$\begin{aligned}
V_g = \frac{IR_{sh}}{12} \times \Bigg[& \frac{(N+1)(4N-1){L_B}^2}{W_B L_B + W_F L_F} \\
& + \frac{2(N+1)(2N+1)L_B L_F W_F/W_B + 6{L_F}^2}{W_B L_B + W_F L_F}\Bigg], \\
\sigma_0 = \beta V_g &
\end{aligned}$$

As shown in the above equation, three factors, N, L_F and L_B have a strong influence on stress. Fig. 9 shows how the EM-induced stresses at the node 0 change with the L_F and L_B. As we can see, L_B has much larger impacts on the stress than the L_F, which can be used for EM optimization. Other trends of stress change will be analyzed and discussed in the numerical result section.

4. NUMERICAL VALIDATION RESULTS AND DISCUSSIONS

In this section, we validate the proposed voltage-based EM (VBEM) immortality check tool against the numerical analysis results. We validate the VBEM method against the results by a finite element analysis (FEA) tool, COMSOL [16], based on the dynamic stress evaluations described

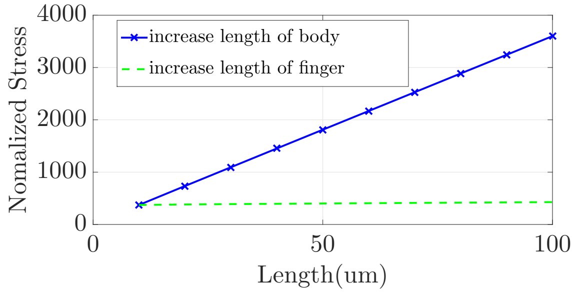


Figure 9: EM stress validations for each comb structure interconnect for changing of L_B and L_F

Table 1: Parameters for each straight-line 3-terminal interconnect case

Case	**Branch a**			**Branch b**		
	l	w	j	l	w	j
	μm	μm	MA/cm^2	μm	μm	MA/cm^2
1	25	1	1.25	0	1	0
2	25	1	1.25	175	1	0
3	25	1	1.25	175	1	0.125
4	25	1	1.25	175	1	0.625
5	25	1	1.25	175	1	1.25
6	10	0.1	10	25	1.25	1.25
7	10	0.2	5	25	1.25	1.25
8	10	0.3	3.3	25	1.25	1.25
9	10	0.4	2.5	25	1.25	1.25
10	10	0.5	2	25	1.25	1.25

by Korhonen equation ((6)). In the following, we list the results for the three structures we discussed.

4.1 Straight-line 3-terminal interconnects

The parameters used for the validation cases are summarized in Table 1 and the results of 3-terminal wires are shown in Fig. 10, which shows the largest tensile stress at the node 0.

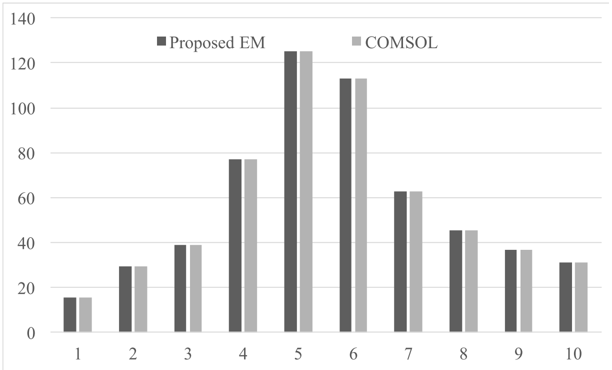


Figure 10: EM stress validations for each straight-line 3-terminal interconnect case (x: case number, y: EM stress at the node 0 (cathode node))

As demonstrated Fig. 10, the results of the proposed method agree well with COMSOL results. With the increase of length and current density in the branch b, the EM stress increases. If the current density in branch a decreases, EM stress also decreases.

4.2 T-shaped 4-terminal interconnect

We next validate VBEM method on the T-shaped 4-terminal interconnect case. Again, we list the parameters used for the validation cases in Table. 2 and results of 3-terminal wires are shown in Fig. 11, which shows the largest tensile stress at the node 0.

Table 2: Parameters for each T-shaped 4-terminal interconnect case ($l = \mu m$, $w = \mu m$, and $j = MA/cm^2$)

Branch	**Case**	1	**2**	**3**	**4**	**5**	**6**
a	**l**	6	10	11	20	20	20
	w	0.14	0.14	0.14	0.14	0.28	0.28
	j	7.142	7.142	7.142	7.142	3.571	3.571
b	**l**	4	0	9	0	0	0
	w	0.14	0.14	0.14	0.14	0.28	0.28
	j	7.142	7.142	7.142	7.142	3.571	3.571
c	**l**	5	5	10	10	5	10
	w	0.28	0.28	0.14	0.14	0.14	0.14
	j	0	0	0	0	0	0

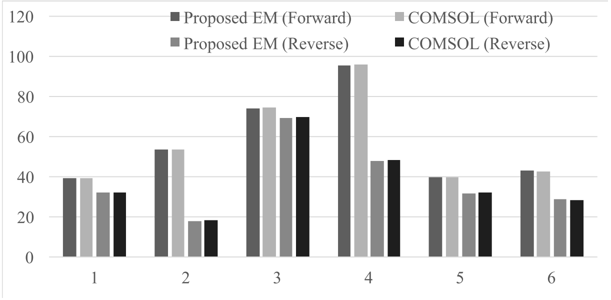


Figure 11: EM stress validations for each T-shaped 4-terminal interconnect case (x: case number, y: EM stress at the node 0 (cathode node))

During the analysis of T-shape, forward and reverse currents are provided in branches *a* and *b*. Again, we observe that the obtained results are also very close to COMSOL results and the average error rate is 0.56% while the maximum error is 1.42% in case 2 reverse. Also, it can be seen if the total length of branches *a* and *b* increases, the stress increases. Furthermore, the stub can have huge impacts on the stress at the stub (branch *c*) with zero current density can decrease the stress if it is closer to the cathode, or its length is decreased. Also, if the stub is placed further away from the cathode and its length is longer, the stress increases.

4.3 Comb structure interconnects

Now we further validate the proposed VBEM method on the comb structured interconnect. We list the parameters used for different test cases and the predicted stress and error rate in Table. 3. Fig. 12 shows the impact of the number of fingers, N, on the stress at the node 0 for these three cases or configurations. As we can see, with increase in N, the EM stress increases super linearly. Besides, we can observe from Fig. 9 that, increasing L_B and L_F increases EM-induced stress at node 0. However, the increase in L_F only has a small effect on EM stress compared to the increase in L_B. Furthermore, the results of VBEM show good agreement with the results obtained from COMSOL. The average error is 0.49% and maximum error is 1.3% in case 3 at N=8.

5. CONCLUSION

As VLSI technology features are pushed to the limit with every generation and with the introduction of new materials and increased current densities to satisfy the performance demands, EM failure risk is ever-increasing. In this paper,

Table 3: EM stress validations for comb structure interconnect cases

Comb Case	Method	Number of fingers					
		1	**2**	**4**	**6**	**8**	**10**
Case 1 - $W_B = 1$,$W_F = 1$, $L_B = 10$,$L_F = 10$	**Proposed EM**	10	23.75	71.25	145.42	246.25	373.75
	COMSOL	10	23.78	71.33	146.50	245.10	375.88
	Error	0.00%	0.08%	0.11%	0.74%	0.47%	0.57%
Case 2 - $W_B = 1$,$W_F = 1$, $L_B = 20$,$L_F = 10$	**Proposed EM**	15	41.67	135	281.67	481.67	735
	COMSOL	15	41.59	136.28	279.80	486.41	738.12
	Error	0.00%	0.18%	0.94%	0.67%	0.98%	0.42%
Case 3 - $W_B = 1$,$W_F = 1$, $L_B = 10$,$L_F = 20$	**Proposed EM**	15	29.17	77.5	152.5	254.17	382.5
	COMSOL	15	29.42	77.19	152.07	257.51	385.73
	Error	0.00%	0.85%	0.41%	0.28%	1.30%	0.84%

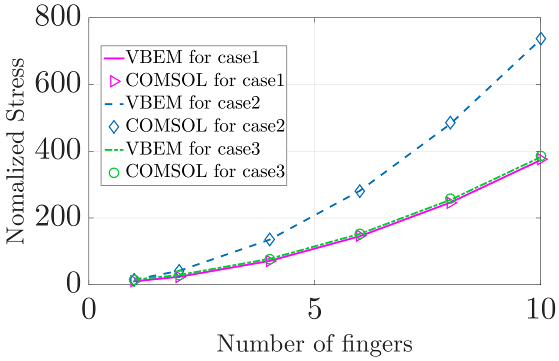


Figure 12: EM stress validations for each comb structure interconnect case (x: number of fingers, y: EM stress at the node 0 (cathode node))

we present a novel and fast EM immortality check for general multi-branch interconnect trees. It can be viewed as the *Blech product* for multi-branch interconnects for fast check of EM immortality of wires. The new VBEM analysis method is very amenable for EM violation fixing as it brings new design knobs and capability in the physical design stage. The resulting EM risk assessment method can be much easier integrate with the physical design tools. The new voltage-based EM stress estimation method is based on the exact solution of fundamental stress steady-state equations. We show that its solution is consistent with the physics-based dynamic EM stress evaluations from the numerical analysis by COMSOL. This approach eliminates the need for complex look-up tables for different geometries and can be implemented in CAD tools very easily as we demonstrated on real design examples.

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