EM-Based on-Chip Aging Sensor for Detection and Prevention of Counterfeit and Recycled ICs

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***Abstract*—The counterfeiting and recycled integrated circuits (ICs) has become a major security threat for commercial and military systems. In addition to the huge economic impacts, they post significant security and safety threats on those systems. In this paper, we propose a new lightweight on-chip aging sensor, which is based on the electromigration (EM)-induced aging effects for fast detection and prevention of recycled ICs. Our new EM-based aging sensor exploits the natural aging/failure mechanism of interconnect wires to time the aging of the chip. Compared with existing aging sensor, the new aging sensor can provide more accurate prediction of the chip usage time at smaller area footprints due to its simple structure. The new sensor is based on a newly proposed physics-based stress evolution model of EM effects for accurate prediction of the EM failure. As a result, we can design the interconnect wire structures based on copper interconnect technology so that the resulting wires will have detectable EM failure at a specific time with sufficient accuracy. In order to mitigate the problem of the inherent variations in the metal grain sizes and assess its impacts on the nucleation time of metal wires, a number of parallel properly structured wires are used in the sensor. The parameters of the wires are optimized using the new EM model. Our statistical and variational analysis shows that the proposed aging sensor can accurately predict the targeted failure times in the presence of both inherent uncertainties. Our study also shows that more parallel wires will lead to more accurate statistical predictions at costs of more areas.**

I. Introduction

The counterfeiting and recycling of integrated circuits (ICs) have become major problems in recent years, potentially impacting the security of electronic systems especially for military, aerospace, medical and other critical applications. In addition to diminishing system dependability and usability, counterfeiting reduces total revenue of companies from their research and development efforts, discourages innovation through the theft of intellectual properties (IPs), and produces low-quality products under established brand names [1]. A counterfeit component is defined as an electronic part that is not genuine because it is an unauthorized copy; it does not conform to the original component manufacturer's (OCM) design, model, and/or performance; or it is not produced by the original component manufacturer or is produced by unauthorized contractors; it is an off-specification, defective, or used OCM product sold as "new" or working; it has incorrect or false markings and/or documentation [2].

Today the most widely reported type of counterfeit parts is the recycled type. It is reported that in today's supply chain, more than 80% of the counterfeit components are recycled [3]. These used or defective ICs enter the market when electronic "recyclers" divert scrapped circuit boards away from their designated place of disposal for the purposes of removing and reselling the ICs on those boards. The recycling process involves removing ICs from the board or even dies in the ICs. There are several security issues associated with these ICs. Firstly a used IC can act as a ticking time bomb [4] since it does not meet the specification of the OCM of the ICs; secondly additional die on top of the recovered die can carry a back-door attack, sabotage circuit functionality under certain conditions, or cause a denial of service [5].

The detection methods for recycled chips can be classified into physical methods and electrical methods [1]. Physical methods consist of incoming inspection methods such as visual inspection, X-ray imaging, package analysis method such as laser scanning microscopy, delid method, and the material analysis method such as using Fourier transform infrared, and X-ray fluorescence. Electrical methods contain the parameter tests, function tests, built-in tests and structural tests. In general, physical methods can be applied to all part types, but some of the methods are destructive and take hours to test. As a result, sampling is required to certify a batch of parts by observing a small number of parts. On the other hand, conventional electrical test methods are non-destructive and time efficient, yet they can be very expensive because such techniques are not necessarily designed for counterfeit detection. Electrical test techniques are advantageous because the sampling is not required, and all parts can be tested. However, there are some issues associated with electrical tests that must be addressed.

In order to fast detect and effectively prevent the recycled chip, one viable approach is to insert a lightweight aging detecting sensor, which can directly tell the usage of the chips and some early efforts have been explored [6], [7], [8]. Method in [7] designed the ring-oscillator-based (OR-based) aging sensor that relies on the aging effects of MOSFETs to change a ring oscillator frequency in comparison with the reference one embedded in the chip. As the chip ages owing to the wear-out mechanisms such as negative biased temperature instability (NBTI) and hot carrier injection (HCI), the shift threshold voltage of MOSFET devices, thus the frequency of ring oscillator indicates the level of aging, and provides a simple readout of the value. However, this method can only give very rough estimation of the usage age of the chip as the shift of the frequency depends on many factors. In order to mitigate this problem, the antifuse-based (AF-based) sensor was developed in [1]. The AF-based sensor essentially is a

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counter, which counts the clocks or derivatives of the clock events to log the usage of the chip. The antifuse memory is used to make sure the data in the count will not be erased or altered by attackers. However, the AF-based sensors suffer large area overhead especially when more accurate usage is required [1]. Another problem with this method is that it may not reflect the true aging-dependent usage of a chip. For instance, it will log the same usage time for a chip for different on-chip temperatures, however, which can have dramatically impacts on the aging effects from electromigration, NBTI and HCI [9].

In this paper, we propose a new lightweight on-chip aging sensor, which is based on the electromigration-induced aging effects for fast detection and prevention of recycled ICs. Instead of using traditional aging effects from devices (such as MOSFETs), the new EM-based aging sensor exploits the natural aging/failure mechanism of interconnect wires to time the aging of the chip. As a result, compared with existing the ring-oscillator-based aging sensor, it has following two advantages: First, this structure is much simpler as it only requires metal interconnect wires, which was driven by DC currents. In comparison, the ring oscillator has to be used to detect the threshold voltage shift. Second, it is more accurate as we can measure the EM-induced failure (such as wire resistance changes) time with more accurate than the frequency shift over time. The new sensor is based on a newly proposed hydrostatic stress evolution model of EM effects for accurate prediction of the EM failure [10]. As a result, we can design the interconnect wire structures based on the copper interconnect technology so that the resulting wires can have detectable EM failure at a specific time with sufficient accuracy. In order to mitigate the problem of the inherent variations in the metal grain sizes and assess its impacts on the nucleation time of metal wires, a number of parallel properly structured wires are employed in the sensor. The parameters of the wires are optimized with using the new EM model. Our experimental results show that the proposed aging sensor can accurately predict the targeted failure times in the presence of both inherent uncertainties. Our study also shows that more parallel wires will lead to more accurate statistical predictions at costs of more areas.

This paper is organized as follows. Section II reviews the EM effect and recently proposed physics-based EM model. In Section III, we present the new lightweight on-chip aging sensor circuit as well as the interconnect wire structures. Several statistical and variational analyses are presented in Section IV. Last, Section V concludes.

II. Review of EM effects and EM models

A. Review of EM-induced failure effects

The proposed on-chip aging sensor is based on the observation that the EM-induced failure of interconnect wires can be designed such that the wires can fail at a specific time frame detected by the increase of their resistances over a pre-defined threshold. To understand this, let's first have a brief review of the EM failure effects from the first principles and then we present the problems and solutions to design the wire structure for timed failure based on EM physics.

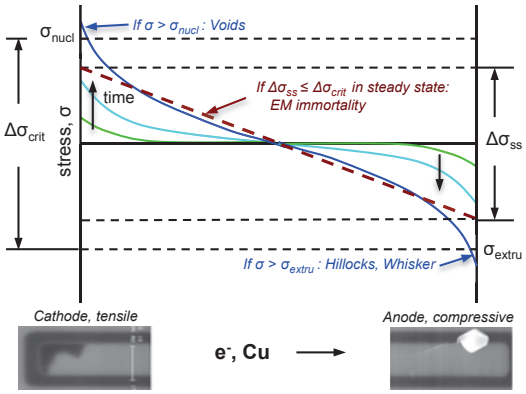


Fig. 1: The EM-induced stress development and distribution of an interconnect wire.

EM is a physical phenomenon of the migration of metal atoms along a direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate toward the anode end of the metal wire along the trajectory of conducting electrons. This oriented atomic flow, which is caused mostly by the momentum exchange between atoms and the conducting electrons, results in metal density depletion at the cathode, and a corresponding metal accumulation at the anode ends of the metal wire. This depletion and accumulation happen because atoms cannot easily escape the metal volume.

The interconnect segment here means a continuously connected, highly conductive metal within one layer of metallization, terminated by diffusion barriers. Thin layers of refractive metals form these diffusion barriers for Cu atoms, preventing them from diffusing into inter-layer (ILD) and inter-metal dielectrics (IMD). When metal wire is embedded into a rigid confinement, which is the case with interconnect metallization, the wire volume changes (induced by the atom depletion and accumulation due to migration) creating tension at the cathode end and compression at the anode ends of the line. Over time, the lasting unidirectional electrical load increases these stresses, as well as the stress gradient along the metal line. Fig. 1 shows the stress evolution in a straight wire over time. The cathode node has the tensile stress (positive stress) built up, while the anode node has compressive stress generated (negative stress). In some cases, usually when a line is long, this stress can reach a critical level, resulting in void nucleation at the cathode and/or hillock formation at the anode end of line as shown in Fig. 1. Different physical mechanisms can be responsible for generating these damages. In the case of voiding, existing cohesive or interfacial micro-cracks near or at the barrier/Cu interfaces can develop into a void by the action of the appropriate stresses. Hillock formation, which is a compression-induced extrusion of metal into the surrounding dielectric that can cause a shortage between neighboring metal lines, can be initiated by micro-cracks in the adhesion/barrier layers. However, typically the voids are the major defects from EM.

One important observation of EM effects is that the time to failure (TTF) of a wire show some degree of randomness. This TTF represents the instant in time when an increase in

line electrical resistance caused by the void growth reaches a critical level (for example, a 10% increase over the original value). The reason is that the grain boundaries (GB) of metal wires has random sizes and orientations, which lead to variations in the atomic diffusivities. Actually the EM-induced TTF follows the lognormal distribution [11]. This inherent uncertainty in TTF is one of the challenges to designing accurate aging sensor.

B. Physics-based EM model

Traditionally the EM effects are modeled by the semi-empirical Black's equation. However, Black's equation suffers several problems for accurate TTF estimation. The major drawback of this model is that it fails to consider impacts of wire length and residual stresses.

Recently, more accurate and physics-based EM model has been proposed [12], [10]. In this model, the EM kinetics consists of two phases: (1) the void nucleation phase and (2) the void growth phase. In the nucleation phase, the void nucleation time (t_{nuc}) can be computed as follows:

$$t_{nuc} \approx \tau^* e^{\frac{E_V}{kT}} e^{-\frac{f\Omega}{kT}\left(\sigma_{Res}+\frac{eZ\rho l}{4\Omega}j\right)} ln\left\{\frac{\frac{eZ\rho l}{4\Omega}j}{\sigma_{Res}+\frac{eZ\rho l}{4\Omega}j-\sigma_{crit}}\right\} \quad (1)$$

where $\tau^* = \frac{l^2}{D_0} e^{\frac{E_D}{kT}} \frac{kT}{\Omega B}$. Here, E_V and E_D are the activation energy of vacancy formation and diffusion, f is the ratio of volumes occupied by vacancy and lattice atom. In this model, we consider the residual stress of $\sigma_{Res} = \sigma_T + (B/9)(R/\delta)exp\{-E_V/kT_{ZS}\}$ when electrical stressing was applied. Here, σ_T is the thermal stress developed in the metal line confined in the ILD/IMD dielectric during cooling from the zero stress temperature T_{ZS} down to the temperature of use condition, $(B/9)(R/\delta)exp\{-E_V/kT_{ZS}\}$ is an additional stress generated by vacancy relaxation to the equilibrium concentration corresponding to new stress value and temperature [12], R is the mean grain size, and δ is the GB thickness. Dependence of t_{nuc} on grain size allows one to introduce a simple statistical model for void nucleation at the line cathode edge.

Note that the nucleation time t_{nuc} is also function of the wire length l, which is totally ignored in the existing EM models. We further note that in the new physics-based EM model, one needs to explicitly consider the residual stresses, σ_{Res}, which can have huge impacts on the nucleation time and thus the failure time of a wire. As a result, it is important to have an accurate estimation of residual stresses and more accurate residual stress can be computed using multi-scale numerical method [13].

In the second growth phase, void starts to grow and wire resistance starts to change. Kinetics of the wire resistance change can be approximately described as:

$$\Delta r(t) = \vartheta(t - t_{nuc}) \left[\frac{\rho_{Ta}}{h_{Ta}(2H+W)} - \frac{\rho_{Cu}}{HW}\right] \quad (2)$$

Here ρ_{Ta} and ρ_{Cu} are the resistivity of the barrier material (Ta/TaN) and copper, W is the line width, H is the copper thickness, and h_{Ta} is the barrier layer thickness. $\vartheta = \frac{D}{kT} eZ\rho j$ is the drift velocity of the void edge.

III. Proposed EM-based aging sensor circuit

A. Wire structure for accurate EM-Induced aging detection

In the section, we investigate the new wire structures so that we can have more accurate detection of the EM induced resistance changes based on the new physics-based EM models. There are several factors we need to consider to design the right interconnect wire structures as the critical component of the aging sensors. First, there are the inherent variations in the metal wires, which will lead to the uncertainties in the nucleation time and the growth time. For a metal wire, its grain boundaries (GBs) may have different crystallographic orientations, which are characterized by different atomic diffusivities. Second, the grain sizes have a random distribution. As a result, the lifetime of the metal wires obeys the lognormal distributions [11]. Hence, we cannot use only one metal wire as the aging sensor. Third, how to design the geometry of the wires (length and width) to have a small area and power overhead for the sensors. We want the sensors to have a small footprint with considering their power consumptions and areas. In addition, they will meet the design rules, which are compatible with given design technologies. Fourth, we need to have an accurate estimation of the residual stresses σ_{Res} (mainly the thermal stresses), which largely depend on the temperature of the manufacturing process and even the packaging process.

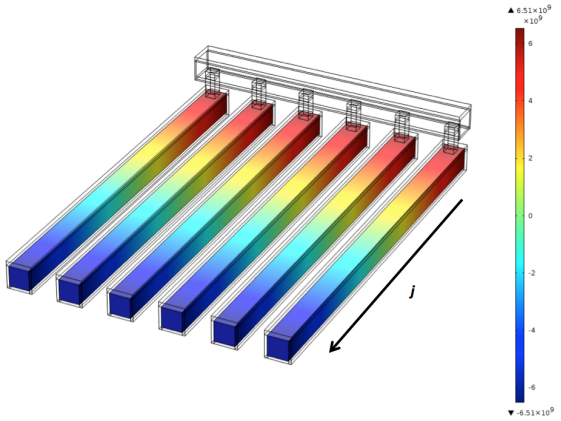


Fig. 2: The proposed parallel multi-wire structure for the aging sensor and its stressed condition.
Note: the *j* represents the direction of electron flow

In order to mitigate the inherent uncertainties in the atomic diffusivities in a metal line, one solution is to use a number of wires connected in parallel as shown in Fig. 2, in which each wire will have its own diffusion barriers at both ends (so they are treated as individual wires in the EM sense). However, they are connected in parallel by another metal layer through vias. The color in the figure shows the simulated stress distributions in each wire. Those wires will be stressed all the time (with constant current running through them). We can design the wires such that they will fail at a specific time such as one year, two years, ..., or n years. Assume that the resistance value of the stressed wire at $t = 0$ is r_0. The failure time can be defined as the time when the wire resistance increases 10% of

its values, i.e. $1.1 * r_0$, which can be predicted by the physics-based EM model. We also need to design a *reference* wire, which is not normally stressed (unless its resistance value is read during the detection time). The resistance value of the reference wire should be set to $1.1 * r_0/k$, k is the number of wires in the stressed wire set. For the reference wire, we only need one wire segment as it will not age (the uncertainties in the EM-induced aging will not affect it). Our preliminary study shows that depending on the inherent variations, we can determine the number of wires such that we can confine the lifetime variations to a sufficient small range. The exact number wires used will be explored and validated by the actual silicon data. We remark that the intra-die process variations will affect the resistance values of those wires. However, if they are placed very closely, as this should be the case, the impacts will not be significant.

B. Resistance detection sensor circuit

Fig. 3 shows the schematic of the proposed EM-based aging sensor circuit. The circuit is composed of a constant current source, an EM stressed parallel wire (EMS) set, an EM reference wire (EMR), which will not be stressed in normal operation, a one-bit ADC (essentially an Opamp circuit), two resistors, one multiplex (MUX), one switch and one register to store the sensor digital output. The EMS contains a number of parallel wires (such as 6 in our initial analysis) with identical geometries. The EMR is just a single wire. The constant current source provides the current to stress EMS when the power is on. The one-bit ADC is used as a comparator to decide if the stressed EMS has a larger resistance than the EMR. If the voltage on EMS is higher than the voltage on EMR, it outputs 1, which indicates the failure happens, otherwise 0, which indicates that failure has not happened yet. The MUX and the switch are controlled by the *Read_en* signal from outside. When *Read_en* is off, the output of one-bit ADC will not be read into the register and the there is no current on EMR as it is in an open circuit. When Read_en is on, there will be a voltage on EMR, which is 10% higher than the original voltage on EMS and the comparison result from one-bit ADC can be written into the register. As time going, the resistance of the EMS will increase due to the EM effect, which means the voltage of the non-inverting input of the one-bit ADC will increase. If the chip has been used for time longer than the designed failure time, the output of one-bit ADC will be 1 instead of 0.

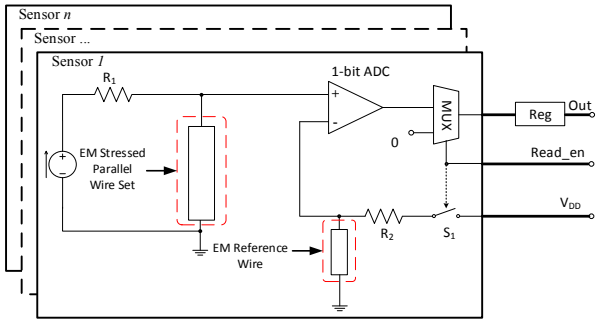


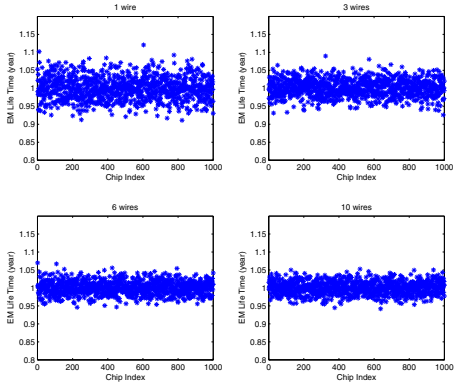
Fig. 3: The structure of the EM-based aging sensor.

We will design a number of such aging sensors for the specific years (for instance 1 year to 10 years) in this project for validation purpose. Similar to the other on-chip aging sensors, the output registers can be connected by the JTAG circuits of the chip design so that one can read the aging information out in-situ during the testing or diagnosis time. The aging information can also be read out before the chips are put into the system. Note that the proposed EM-based sensor can automatically consider the temperature impacts on the lifetime of the chips as it is based on the EM aging effects.

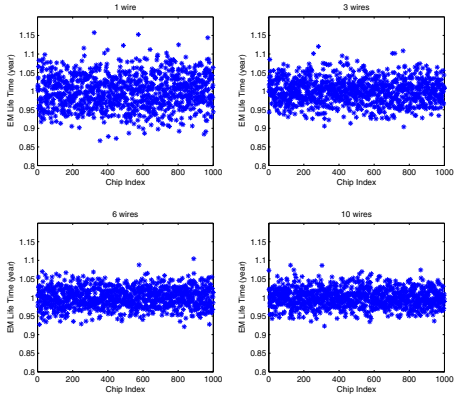
IV. Performance Analysis and Experimental Results

In this section, we will present the performance analysis of the proposed EM-based aging sensor including simulation results.

A. Effect of number of wires



(a) Variance $\theta = 0.001$

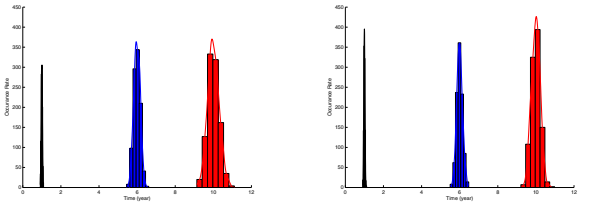


(b) Variance $\theta = 0.002$

Fig. 4: (a) and (b) the statistical study of stressed wires connected in parallel with different wire numbers and variations.

For the proposed EM-based aging sensor, if the inherent variations are same for all the wires, then the wire (wire set), which fails at longer time, will have less absolute accuracy. For instance, 10% life time variation for a one-year wire will have

an accuracy of about one month. While 10% lifetime variation for 10-year wire will lead to errors about one year. In order to mitigate this problem, one solution is to add more parallel wires for longer year wire set. Because more parallel wires we have, the smaller lifetime deviation the whole wire set will have. Fig. 4(a) and Fig. 4(b) show statistical analysis results for EM lifetime of stressed wire set connected in parallel versus number of wires in each set and different variations. These results come from 1000 Monte Carlo simulation runs and the aging sensor wires are set for the one-year lifetime. The EM-induced lifetime follows the lognormal distribution [11] and the variance are set to 0.001 and 0.002 respectively for the two figures. With 0.001 variance, we can see that with one wire, the EM lifetime will fall into $\pm 10\%$ lifetime mean with 99.83% chance and into $\pm 5\%$ lifetime mean with 88.64% chance. If we use 6 wires, we can have 100% chance to achieve $\pm 10\%$ life mean and 98.66% chance for $\pm 5\%$ life mean, which is good enough. If we increase the variance to 0.002, then one wire can reach 97.46% chance for $\pm 10\%$ life time mean; 6 wires can achieve 99.95% chance for $\pm 10\%$ lifetime mean and 92.00% chance for $\pm 5\%$ lifetime mean. For 10 wires, we can achieve 99.99% chance for $\pm 10\%$ lifetime mean and 95.33% chance for $\pm 5\%$ lifetime mean. As we can see, with large inherent variations, we have to increase the number of wires to mitigate to reduce lifetime variations. We remark that the intra-die environmental variations will also affect the resistance values of those wires. However, if they are placed very closely, as this should be the case, the impacts will not be significant.



(a) Number of wires used: 6; Variance $\theta = 0.002$

(b) Number of wires used: varying; Variance $\theta = 0.002$

Fig. 5: The statistical lifetime detections from the stressed wires: (a) using the constant 6 wires; (b) using the varying number wires (6 wires for 1 year, 10 wires for 6 years, and 14 wires for 10 years).

Fig. 5 studies the lifetime variations versus the number of parallel wires used in each wire set for specific years (1 year, 6 years, 10 years). If we use the constant 6 wires for each set as shown in Fig. 5(a), we can see that the lifetime prediction variations in the 10-year wire set is quite significant for given variance ($\theta = 0.002$). But if we use varying numbers of wires for the same design (6 wires for 1 year, 10 wires for 6 years, and 14 wires for 10 years), the variations for the wire sets at the longer time lifetimes will be reduced as shown in Fig. 5(b).

B. Effect of length of wires

Fig. 6 shows the relationship between wire length L and wire EM lifetime. The current density j is constant and set

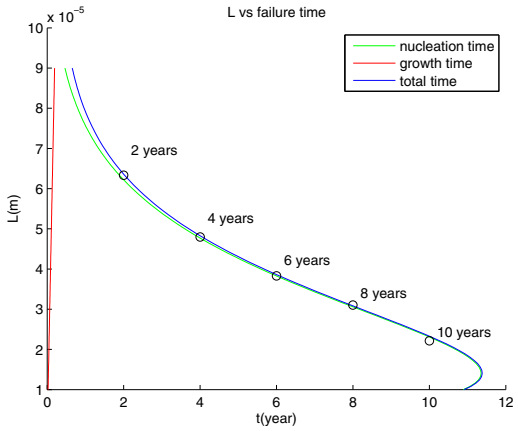


Fig. 6: Length versus EM lifetime of a wire.

to $3 * 10^{10} A/m^2$. We show both the nucleation time and the growth phase time predicted by the new EM models. As we can see, the total lifetime increases with decreasing L (so does the area), which shows that shorter failure time will need larger area compared to the longer failure time.

For a specific failure year designed, the area for the sensor wires can be estimated as $A = W * L * k$, where W is the width of each stressed wire (assuming that all the stressed wire are same) and L is the length of the stressed wire. The area of reference wire is $1.1 * W * L/k$, which is typically less significant compared to stressed wires. The power consumption for total stressed wires can be estimated as $P = k{*}I^2{*}R{=}k{*}(j{*}A)^2{*}\rho{*}L/A{=}k{*}j^2{*}L{*}\rho{*}A{=}k{*}j^2{*}L{*}\rho{*}W{*}H$, where ρ is the resistivity of the metal wire, j is current density, and H is the height of the wire segment as shown in Fig. 2. From the two formulas above, we can see that we should try to use the minimum width allowed by the technology node to save both area and power in theory. Our initial study shows that area and power are two performance metrics for trading-off in the design. Fig. 7 shows the power values versus the possible wire length (L) and current density j. The 10 red curves show the possible L and j values from 1 year to 10 years. We can clearly see the trade-off between L (area) and power.

Bear in mind that tens of EM-based aging sensor can be inserted into commercial chips, which would easily detect the counterfeit and recycled ICs and show the age of the chip. Such a method is practical because the area overhead is small. An EM-based aging sensor with 10 stressed wires costs 100-500 um^2 with an SMIC 180nm technology, which depends on the length of the wire. Assuming a total of 10 sensors, the overhead is only 0.02% of the 25,000,000 um^2 area available in a 5 mm $\times$ 5 mm chip.

C. Experimental results

The proposed EM-based aging sensor circuit has been designed and validated using SPICE simulation. We performed 1000 Monte-Carlo simulation runs considering the variation of the nucleation time for the stressed wires. We design the wires such that they will fail (its resistance increase just 10%) around

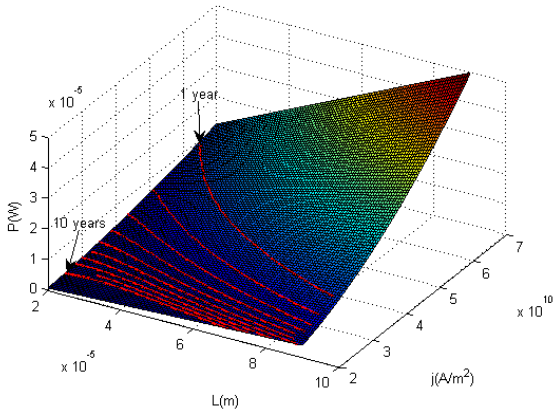
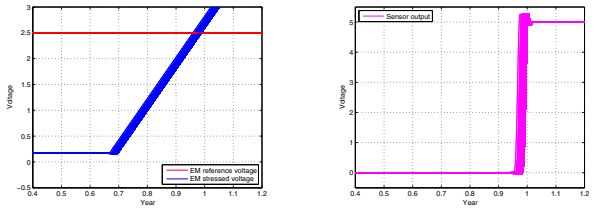


Fig. 7: The power consumption of stress wires versus wire length and current density.

one year with lognormal distribution (standard deviation is set to 0.001) in their nucleation times.



(a) (b)

Fig. 8: (a) The statistical voltage inputs for the ADC; (b) The statistical ADC output.

Fig. 8(a) shows the voltage waveforms at the two inputs of the ADC. In the beginning, the two inputs are clearly different. At the around 0.68 year, the voltages on the stress wires start to increase, which is also the nucleation time for the wires. Then, the voltage of the stressed wires starts to increase gradually until it runs across the 2.5 volts, and then the ADC output will change '1' from '0'. Fig. 8(b) shows that the ADC output will start to change from '0' (zero volts) to '1' (5 volts) around one year. As we can see, when the input voltage of stressed wires reaches the reference voltage, the output signal starts to change, which happens at one year in this case.

Fig. 9 shows the statistical distribution of the lifetime detection results of the sensor wires at the output of the ADC. As we can see, the distribution is lognormal owing to the lognormal distribution of the nucleation time of the wires. This clearly shows that the proposed aging sensor work well as the failures of the wires can be very accurately detected around one year.

V. Conclusion

In this paper, we have proposed a new on-chip aging sensor based on the EM-induced failure mechanisms to fast detect the recycled integrated circuits, which is one of the major

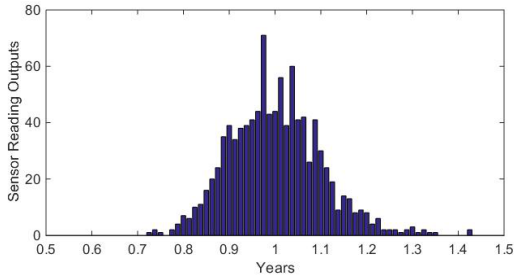


Fig. 9: The statistical distribution of the lifetime of the sensor wires detected.

hardware security issues facing the semiconductor industry. The new sensor is based on failure detections of DC current stressed metal wires to time the usage of chips over time. Compared with the existing ring-oscillator-based aging sensors, it can offer a simpler circuit implementation and smaller area footprints. It also provides a more accurate prediction of the chip usage time. The new aging sensor design is based on a newly proposed physics-based EM model. Experimental results show that the proposed aging sensor can accurately predict the targeted failure times in the presence of both inherent uncertainties. Our study also shows that more parallel wires will lead to more accurate statistical predictions at the cost of areas.

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