IR-Drop Based Electromigration Assessment

Parametric Failure Chip-Scale Analysis

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***Abstract*—This paper presents a novel approach and techniques for electromigration (EM) assessment in power delivery networks. An increase in the voltage drop above the threshold level, caused by EM-induced increase in resistances of the individual interconnect segments, is considered as a failure criterion. This criterion replaces a currently employed conservative weakest segment criterion, which does not account an essential redundancy for current propagation existing in the power-ground (p/g) networks. EM-induced increase in the resistance of the individual grid segments is described in the approximation of the physics-based formalism for void nucleation and growth. A developed technique for calculating the hydrostatic stress distribution inside a multi branch interconnect tree allows to avoid over optimistic prediction of the time to failure made with the Blech-Black analysis of individual branches of interconnect segment. Experimental results obtained on the IBM benchmark circuit validate the proposed methods.**

Keywords—electromigration; power-ground networks; IR-drop; void; failure

I. INTRODUCTION

Governed by a technology scaling continuous increase in the die size accompanying by reduction of the metal line cross sections and, hence, by increase of the current densities, results in an increasingly difficult EM signoff when the traditional EM checking approaches are employed. Widely predicted decrease in EM lifetime, which should follow the transition to advanced technological nodes, should be responsible for the pessimistic performance–reliability paradigm: high chip performance is accompanied inevitable by poor reliability and vice versa, a very reliable chip cannot demonstrate the top performance. This pessimistic conclusion is based on current assessment where an EM-induced failure rate of the individual segment is considered as a measure of EM induced reliability and, in the extreme end, a mean time-to-failure (MTTF) of the weakest segment is accepted as a measure for the chip life-time. It results in very conservative EM-aware current density design rules for the leading-edge technology nodes.

A very different way to EM assessment can be proposed if we take a look at the interconnect reliability from the position of its functionality, when the failure of interconnect just means its inability to function properly [1]. There are two most important functions of the chip interconnect, which are: providing a connectivity between different parts of design for a proper signal propagating, and delivering everywhere a needed amount of voltage. While the cutting-off the individual segments of the interconnect circuits can degrade both these functions, the role of EM is quite different in these two cases of degrading the power supply chain and the signal circuits. The difference is in the types of electrical currents employed in these two cases. Indeed, the majority of signal lines carrying bidirectional pulsed currents are characterized by very long times to the EM-induced failure. It is caused by a repetitive increase and decrease of the mechanical stress at the segment ends, caused by the atom accumulation and depletion due to interaction with the electron flow through a momentum exchange with the conduction electrons. In contrast, power lines carrying unidirectional currents can fail in much shorter times due to continues stress buildup under EM action. Thus, we can conclude that in the majority of cases the EM induced chip failure is happening when interconnect cannot deliver needed voltage (V_{dd}) to any gate of the circuitry. It means that loss of performance, which is a parametric failure, should be considered as the practical criterion of EM-induced failure rather than a catastrophic electrical breakdown or short. It is clear that a structure of the power grid, which is characterized by high level of redundancy, can affect the kinetics of failure development. Indeed, due to redundancy the failures of some amount of interconnect segments do not necessary result in the unacceptable voltage drop on the grids, [2]. Thus, more accurate and less pessimistic full-chip EM assessment and MTTF prediction will require a development of new methods that deal with the grid structure and take redundancy into account. Ideally the distributions of time-to-failure of individual segments should be provided by measurements.

Described EM assessment assumes a prior knowledge of current densities and temperatures in each segment across interconnect. A complexity of extraction of these distributions is acerbated by an uncertainty in work load taking place in modern chips. Its complex multi-modal behavior results in a dependency of the power dissipated by different blocks on the modes of operation. It means that current densities and temperatures in different interconnect segments should be estimated for different workloads and should be used for prediction of MTTF happening in different scenarios including worst-case conditions for voltage drop [3].

Additional problem that should be addressed in order to develop a robust methodology for the full-chip EM assessment is an availability of the physics based models for void/hillock

initiation and evolution that cause a time dependent degradation of the segment electrical characteristics. Currently employed Blech limit [4] (for the out filtration of immortal segments) and Black's equation [5] (for calculating MTTFs for segments characterized by known current densities and temperatures) are subjects for the hard criticism [6-8]. Across-die variation of residual stress makes the Blech's "critical product" to be layout dependent variables rather than experimentally determined constants. Interdependency of the Black's activation energy (E_a) and current density exponent (n) on the current density and temperature makes rather controversial the widely accepted methodology of calculating the MTTF at use condition, represented by chip operation current density and temperature, while using n and E_a determined at the stressed (accelerated) condition, characterized by high current densities and elevated temperatures. Hence, the new approach to the full-chip EM assessment should provide a robust methodology for EM failure check and capability for more optimistic prediction of the EM-restricted current density design rules for the future technological nodes. Solid criterion of the failure on the basis of increase of voltage drop above acceptable level, which is caused by an EM-induced increase of segment electrical resistance with accounted grid redundancy, should be developed and validated with the chip performance measurements.

II. Dynamical EM-Assessment on P/G Nets

A. *Interconnect Tree EM Assessemnt*

Traditional physics-based EM assessment models and simulation flows are attributed to a single interconnect line confined by the liners serving as barriers for atomic diffusion. But, the modern p/g networks consist of large segments representing a continuously connected, highly conductive metal (Cu) lines within one layer of metallization, terminated by diffusion barriers, Fig. 1. These segments may have multiple voltage input/output and current source ports represented by interlayer vias and contacts. The major difference between iso-lines and individual limbs of interconnect segments, which are also known as interconnect trees [9], is in absence of blocking boundaries at one or both ends of the limbs. It prevents atoms from accumulation/depletion, and eliminates related stress buildup at the branch ends, and, hence, makes both, the traditional immortality assessment and MTTF calculation as a groundless, [10].

A physically viable approach to the EM assessment in chip interconnect was proposed in a number of publications by MIT team of C. Thompson, see for example [9]. In their approach the on-chip interconnect should is divided on a set of interconnect trees with the following calculation of the void nucleation time and void growth time performed for each tree. While being physically correct (in the scope of used approximations), this approach has missed a dynamical nature of the failure development: the nucleated and growing voids in a number of limbs/segments of different trees by changing the resistances of these segments affect the current densities in other voidless segments. Later undermines a validity of any

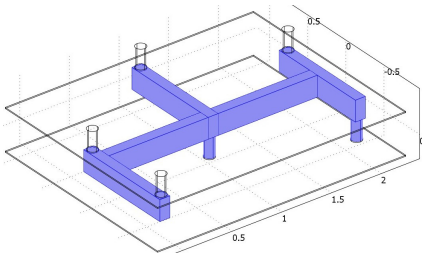

Fig. 1. Interconnect segment confined by diffusion barriers/liners.

steady state filtration of "immortal" trees. A correct approach to the full-chip EM assessment requires a calculating the cooperative void evolution dynamics resulting in the continuously changing current density distribution, that in turn results a change in the void population. An interconnect time-to-failure (TTF) should be calculated as an instant in time when a change in V_{dd} will reach a threshold, say 10%. This time-iterative approach requires a repeated calculation of the current densities in each p/g segment at each time-step.

B. *EM-Induced Voiding Dynamics Inside Interconnect Tree*

An accurate calculation of the void nucleation time inside an interconnect tree can be done based on resolving the hydrostatic stress evolution kinetic inside multi-segment tree. It can be done by solution of the system of the second order partial differential equations (PDE), [11], describing the hydrostatic stress (σ^i_{Hyd}) evolution in each individual segment

$$\frac{\partial \sigma^i_{Hyd}}{\partial t} = \frac{\partial}{\partial x}\frac{D^i_a B^i \Omega}{k_B T^i}\left(\frac{eZ^i \rho j^i}{\Omega} + \frac{\partial \sigma^i_{Hyd}}{\partial x}\right) \qquad (1)$$

Here, D_a is the effective atomic diffusivity, eZ is the effective charge of migrating atoms, B is the effective bulk elasticity modulus, Ω is the atomic lattice volume, ρ is the copper resistivity, j is the current density, k_B is the Boltzmann constant, T is the temperature, x is the coordinate along the segment length, and t is time. Boundary conditions (BC) for these equations reflect the continuities of stresses and atomic fluxes at the segment joints, and the zero flux conditions at the terminating segment ends. Fig. 2 demonstrates an evolution of the stress distributions across the segments of the T-shape tree shown in Fig. 3 that was obtained by analytic solution of the corresponding system of PDE (3). Here, for the sake of simplicity, we assume same D_a , eZ, B, and T for all segments. A differentiation in B can be introduced in a way similar to one proposed by S. Hau-Riege in [12]. Across layout distributions of j and T can be calculated with the method described in [13]. Effective product $D_a \times Z$ is the cross section $(W \times H)$ averaged for the 3D line characterized by the presence of a realistic grain structure and grain boundaries and interfaces between Cu and diffusion barriers:

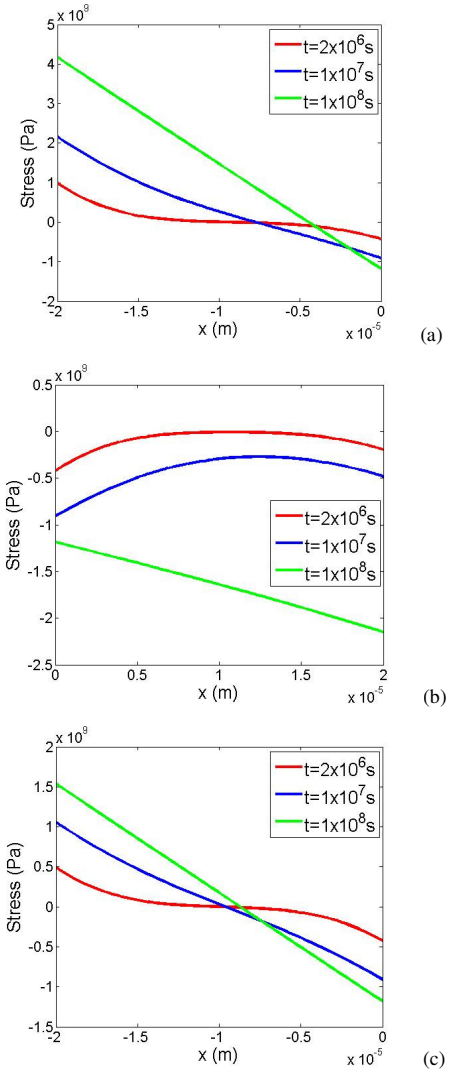

Fig. 2. Evolution of the stress distribution along the segment of the T-shaped tree shown in Fig. 3; (a) line 1, (b) line 2, and (c) line 3.

$$Z \cdot D_a = Z_{GR} \cdot D_{GR} + Z_{GB} \cdot D_{GB} \delta_{GB} \frac{1}{d}\left(1 - \frac{d}{W}\right) + \\ + 2Z_{Int} \cdot D_{Int} \delta_{Int}\left(\frac{1}{W} + \frac{1}{H}\right) \quad (2)$$

Here, the subscripts GR, GB, and INT are referred to the grain interior, grain boundary and interface; δ_{GB} and δ_{Int} are the width of the GB and interface, correspondingly, d is the mean grain size. Analytic solution of (3) allows us to extract the instant in time t_{nuc}, when the developing stress reaches the critical value (σ_{crit}) needed for nucleation of the thermodynamically stable void. Dependence of calculated interconnect-tree specific nucleation time on the mean grain size allows us to exercise a statistical procedure of extraction of the layout-specific mean nucleation time.

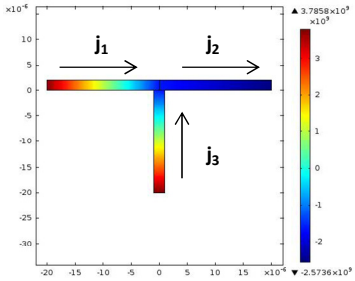

Fig. 3. T-shaped interconnect tree with shown directions of the electron flows.

Kinetics of the stress evolution accompanying the void growth and the void volume kinetics $V(t)$ were determined in [14, 15] from the solution of eq. (1) with the zero stress and zero flux BC at the cathode (void edge) and anode ends of the line. It demonstrates that in the short-time limit the void volume is linear in time

$$V(t) \approx \frac{eZ\rho j D_a WHt}{k_B T} \quad (3)$$

In the long-time limit we have:

$$V_{SV} = \frac{eZ\rho j L^2 WH}{2\Omega B} \quad (4)$$

This solution provides the saturated volume of the void, which can be achieved in the finite-length line at $t = t_{VS}$, when the stress gradient induced back atomic flux compensates the EM induced flux. Knowledge of the void kinetics and its saturated volume, that was developed in a metal line characterized by given geometries (L and $A = WH$), material properties (Ω , Z, ρ, and D_a), and a material surrounding the embedded line (B) allows us to get a time-dependent change in the segment resistance caused by applied j. A relation between the resistance increase and the volume of the void responsible for this increase is

$$\Delta R(t) = \frac{V(t)}{HW}\left[\frac{\rho_{lin}}{h_{lin}(W + 2H)} - \frac{\rho_{Cu}}{HW}\right] \quad (5)$$

When the void saturation volume is developed the further resistance change is stopped until the current density will be changed due to other voids developed somewhere inside same interconnect tree or in other trees. It should be mentioned that grain size distribution does not really affect the void growth rate due to its averaging over a large number of grains being consumed during the void edge propagation.

It should be mentioned that last results are valid for the case where the pre-EM void exists in the line. Hence, in this case we don't have t_{nuc}, and the limb resistance evolves from the initial moment till t_{VS}. In order to obtain more accurate relation between t_{TTF}, t_{VS} and t_{nuc} a more complex initial

and boundary problem should be solved. The solution of equation (1) for initially voidless state taken at $t = t_{nuc}$ and $\sigma = \sigma_{nuc}$ should be used as initial condition for the equation (1) with void-edge BC. This type of analysis of the system of PDE equations for stress evolution in all segments of the considered interconnect tree would be able to describe a dynamic of the multi-void nucleation and growth inside a tree.

For demonstrating the EM assessment performed with this new methodology on realistic p/g design we will use analytic approximations for t_{nuc} and t_{VS}, similar to the previously developed, [10]. A difference between current methodology and from [10] is in introducing the void saturation volume effect. As it will be shown below, this model enhancement results in a longer time to failure and a larger number of voids that need to be generated in order to cause a failure.

III. New Power Grid Reliability Analysis Algorithm

A. New Analysis Flow

Now we present the new EM-induced reliability analysis algorithm and flow for p/g networks. In our formulation of the dynamic p/g networks, the wire resistance begins to change (increase) starting with the nucleation time (t_{nuc}). After this, their resistance changes will be computed by Eq. (5). First we compute initial current densities $j_{0,mn}$ for each branch of every tree. Then, by using the proposed tree-based EM analysis method, we obtain the stresses for all branches in all trees. Next, we identify the trees, which are the subjects for void nucleation: hydrostatic stress at any of the tree nodes is larger than the σ_{crit}. Then, we find the time needed for the first nucleated void. Branch characterized by the largest stress and smallest t_{nuc} among others sets up the initial (starting) time t_0, which is indicated by $t_0 = \min\{t^i_{nuc}\}$ in the step 3 in the algorithm, and the branch will be included in the growth phase pool. After this, we move to next step $t_1 = t_0 + \Delta t$. The chosen time step Δt should be small enough to detect approximately an instant in time when the critical stress is developed in any branch of any segment. We update power grid conductance matrix G due to resistance change in the wire in the growth phase, re-compute current densities j for each wire of each tree again, and repeat the previous steps: stress calculation, identification of the branches satisfying $\sigma > \sigma_{crit}$, putting the most vulnerable branch into growth phase pool if reaches its t_{nuc}, and moving to the next step: $t_2 = t_1 + \Delta t$. We continue this process until the voltage drops at one or more nodes reach the given threshold such as 10% of the supply voltage. We identify this instant in time as the TTF of the whole p/g network.

It is worth noting that, in the step 6 in the algorithm, when updating the resistance of branches in the growth phase, we take into account the generation of the void saturated volume, which develops when growing void consumes all volumetric deformation generated by thermal stress and by redistribution of atoms removed from the space occupied by growing void.

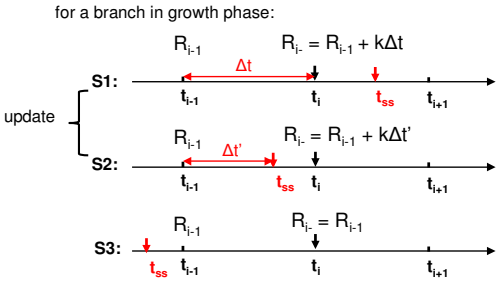

Fig. 4. Check void volume saturation at t_i before updating the branch resistance

For each branch in the growth phase, we first obtain its void volume saturation time (t_{VS}). Then we compare t_{VS} with current time t, as shown in Fig. 1, only under situation *S1* and *S2* the resistance would be updated. Here, *S1* corresponds to the situation that the void has not or has just saturated at instant in time t_i, so the void kept growing during the period $[t_{i-1}, t_i]$, the branch resistance has increased $k\Delta t$ at t_i, where k is the resistance change rate. Situation *S2* means that the void volume have saturated during period $[t_{i-1}, t_i]$, thus the resistance change is $k\Delta t'$, where $\Delta t = t_{VS} - t_{i-1}$. If the void volume has reached the saturated state before time t_{i-1}, which is described in *S3*, the void would be frozen. Under this circumstance the branch resistance remains unchanged during $[t_{i-1}, t_i]$. It is possible that this void might have a larger saturated volume in the future, due to current density change for instance, this frozen void would then start to grow again.

Algorithm 1 New power grid EM-induced reliability analysis algorithm considering void volume saturation

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Input: power grid networks with current inputs, time step, technology parameters
Output: The time reaching the threshold voltage drop (TTF).
1: Compute the initial effective EM current density.
2: Compute the steady state distributions of hydrostatic stress inside each interconnect tree.
3: Find all suspicious branches with the tensile stress larger than the critical one. Compute the nucleation time $t_0 = \min\{t^i_{nuc}\}$ for the most vulnerable branch (with the largest stress).
4: Start the analysis from time $t = t_0$. Branch with the nucleation time t_0 enters the growth phase.
5: **while** the largest voltage drop ≤ threshold **do**
6: Move to next instant in time $t := t + \Delta t$, for wires in the growth phase, check void volume saturation and update the resistances for wires in situation S1 and S2.
7: Perform the DC analysis of the power grids. Re-compute the current densities of each branch.
8: Identify new branches with the stresses exceeding the

critical value.

9: Calculate the nucleation time t^i_{nuc} for all suspicious braches in the nucleation phase. If $\min\{t^i_{nuc}\} \leq t$, the corresponding branch steps into the growth phase.

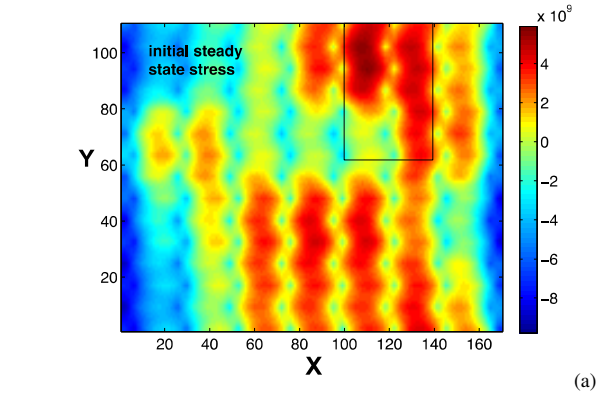
10: end **while**

11: Output t and the failed segment.

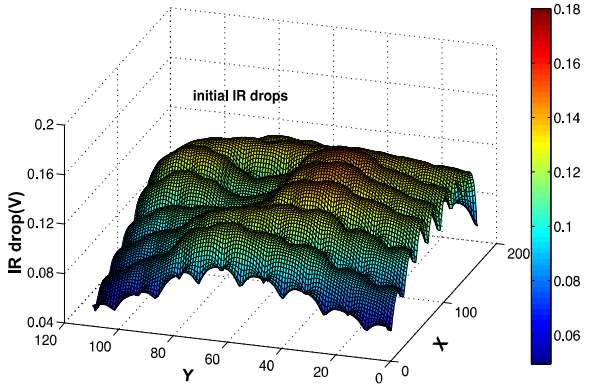
B. Numerical Results and Discussion

The proposed EM assessment method is implemented in C++ and a small IBM power grid benchmark circuit (IBMPG2) [16] is employed for the validation. We analyze the power network whose source current values are modified to guarantee the initial IR drop of any node in the circuit is smaller than the critical value, which is assumed to be 10%V_{DD} in this work. EM induced chip failure happens when the largest IR drop exceeds the threshold.

Fig. 5,a and Fig. 5,b shows the initial steady stress distribution and initial IR drop distribution in the metal layer that directly connects to the underlying logic blocks respectively, in which the units of x- and y- axes are normalized based on the circuit design. The locations of voids nucleated during the lifetime of the circuit are demonstrated in Fig. 6,a, which correspond to high EM stresses. In this experiment, IR drops changing over time have been tracked.

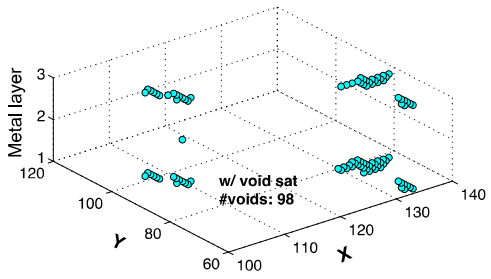


(a)

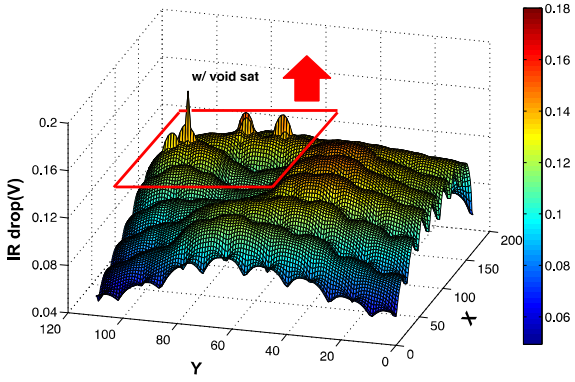


(b)

Fig. 5. Initial steady state stress (Pa) distribution, (a), and initial IR drop (V) distribution at in metal layer 1, (b).

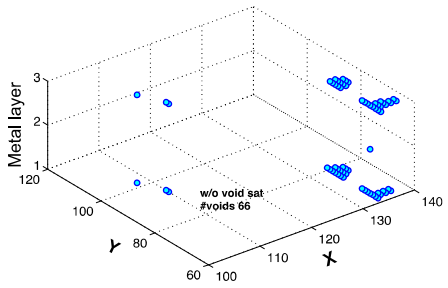


(a)

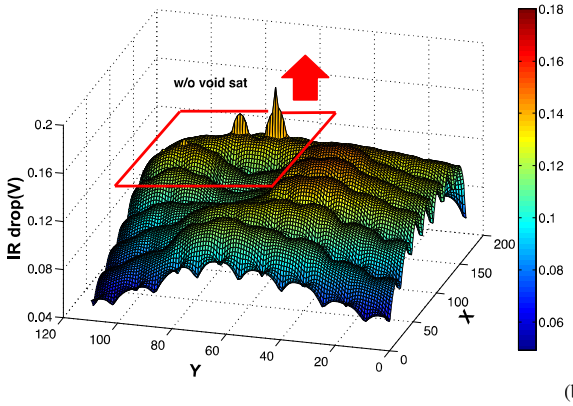


(b)

Fig. 6. (a) Voids distribution in the power network (three metal layers) and (b) IR drop distribution at MTTF of the power grid in metal layer 1.



(a)



(b)

Fig. 7. When void volume saturation is not considered, (a) voids distribution in the power network (three metal layers) and (b) IR drop distribution at TTF of the power grid in metal layer 1.

It is found that the branches with void nucleation and growth induced resistance change have more significant IR drops, as shown Fig. 6,b, when compared to the branches in the same circuit but have no voids nucleated.

The generation of void saturated volume is introduced in this EM model. As a comparison, we also implemented the assessment method, which assumes that the void keeps growing once it is nucleated. Fig. 7,a and Fig. 7,b are the experimental results obtained from the model in which the void volume saturation is not considered. The distribution of the voids in the power network and the distribution of IR drops in the first metal layer at the time when the circuit fails are depicted respectively. It is found that after the void saturated volume is taken into account, the more voids are distributed in the circuit when compared to the distribution where the voids keep growing upon nucleation.

Table I. Comparison between experimental results of IBMPG2 using w/ and w/o void volume saturation EM models

Void Volume Sat.	First Void Nuc. Time	TTF	#voids	#branches in growth phase
w/	6.67 yrs.	18.78 yrs.	98	196
w/o		16.85 yrs.	66	133

Table I summarizes the comparison between experimental results obtained when considering and neglecting void volume saturation EM analysis methods. The results from Table I suggest that, for the same circuit, introducing void volume saturation would result in a larger number of nucleated voids, thus a larger number of branches in the circuit whose resistance have changed due to EM effect, but a longer TTF. It is due to the fact that when the void volume saturation has been considered, a void would stop growing when its volume reaches the saturation state. It starts growing again only when the current passing this limb increases due to voids generated in neighbor limbs/trees. Thus the overall change of branch resistance is slower than that under the without void volume saturation assumption, more time and more voids will be needed for the circuit to meet the same failure criteria. So accounting for void volume saturation in the EM analysis is necessary in order to get precise circuit lifetime.

IV. CONCLUSION

In this work, a proposed new physics-based EM modeling and assessment method has been enhanced and implemented for the power grid networks of VLSI systems. This method accounts for the redundancy of the power grids, while assuming that the circuit is deemed to have failed if it cannot function properly. Void nucleation and growth are considered for assessing the resistance growth. The new EM modeling method is capable to account the statistical nature of the EM phenomenon due to a random grain size distribution. It can also account the thermal and other process-induced residual stresses, which is ignored by the Black's equation based EM assessment. Developed technique allows to assess the evolution of hydrostatic stress inside a multi-limb interconnect tree for more accurate prediction of the TTF in comparison with the traditional Blech-Black analysis of individual branches of the interconnect tree. The experimental results show that the Black's equation based analysis in either weak segment or mesh approximations would lead to more pessimistic results compared with the proposed method, [10]. It also reveals that for the IBM p/g circuits the EM induced failure is more likely to happen at longer times when the saturated void volume effect is accounted.

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