Compact Lateral Thermal Resistance Modeling and Characterization for TSV and TSV Array

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Abstract— **Thermal issues are among the major concerns for 3D stacked ICs, and Through silicon vias (TSVs) are used to effectively reduce the temperature of 3D ICs. Normally, TSV is considered as a good thermal conductor in its vertical direction, and its vertical thermal resistance has been studied extensively. However, lateral heat transfer of TSVs, which is also important, was largely ignored in the past. In this paper, we propose an accurate physics-based model for lateral resistance of TSVs in terms of physical and material parameters, and discuss the conditions valid for model accuracy. In addition to modeling the lateral thermal resistance of a single TSV, the proposed thermal model is also applicable to TSV arrays or TSV farms. We show that the TSV insulation linear and space between TSVs could impose a significant impact on TSV thermal behavior. The new TSV thermal model can be easily integrated into a finite difference based thermal analysis framework to improve analysis efficiency. The accuracy of the model is validated against a commercial finite element tool - COMSOL. Experimental results show that the proposed TSV lateral thermal resistance model is very accurate for both a single TSV and TSV arrays.**

I. INTRODUCTION

Thermal issues are among major concerns for three dimensional (3D) stacked integrated circuits (ICs). The major factors driving the issue are increased thermal resistance along the primary heat transfer path and high power density. Through silicon vias (TSVs) or thermal TSVs (TTSVs) are vertical vias in 3D ICs, which can effectively convey heat from multiple layers to the heat sink. TSVs have shown promise in alleviating the thermal problem seen in 3D stacked ICs [1], [2]. For thermal modeling of 3D chip structures, it is important to incorporate TSVs into the thermal model because it can significantly change the thermal profile of the 3D chip and TSV models are important for many thermal-aware physical optimizations [3]–[8].

Traditional approaches treat TSVs as a vertical lumped thermal resistor in each physical plane and its resistance value is proportional to the length and inversely proportional to the diameter of the TTSV [9], [10]. The TSV as a one dimensional (1D) network implies heat flows only in the vertical direction towards the heat sink of the system. This method is shown to be insufficient in capturing the thermal behavior of the TSVs since the lateral heat transfer through these structures is neglected. Recent study shows that the lateral thermal effects due to TSVs or TSV array or farms can have a significant impact on the thermal profile of the 3D chips [11]. Alternately, accurate numerical approaches such as finite difference (FD) and finite element methods (FEM) can be applied to build the thermal model of the chip package. However, to capture the small feature size of TSVs such as the diameter of TSV and thickness of the insulation layer of TSVs, very fine mesh grids are required, which significantly increase the model complexity and thus the cost of simulation.

For finite difference based analysis especially in the system and architecture levels, large grid sizes may be used in order to reduce the computation cost of thermal analysis of 3D stacked chips with TSVs. In this case, we may have one or more TSVs in one grid and it becomes important to drive the equivalent lumped models (in both vertical and lateral directions) for such TSV-bearing grids. In addition to fast finite difference analysis, a very compact and accurate TSV model which offers insight about the thermal properties of TSV structures and links the heat transfer process with the physical parameters will be very useful for architecture level TSV planning and inter-layer level thermal design for 3D ICs.

Recently, a compact thermal TSV model for 3D stacked ICs was proposed in [12], in which the lateral thermal resistance is considered. It is an initial effort to address this important thermal modeling problem. This method, however, mainly studied the stacked thermal TSVs across many active layers. It only considered the lateral thermal resistance due to the insulations. Furthermore, their thermal model works only for a single TSV, not for an array of TSVs. As we can see that the array of TSVs cannot be simply constructed by the individual TSV models. To mitigate the model accuracy issues, a larger model (called distributed model) is used in [12]. This in turn will impact the analysis efficiency.

In this paper, we propose a new analytical physics-based lateral thermal resistance model for both a single TSV and a TSV array. Our contributions lie in following aspects: First, our lateral thermal resistance model considers both insulation and the filling core of TSV because the thermal resistivity of copper is approximately one third of that of silicon and cannot be ignored. Second, we show that the space between TSVs has a significant impact on the lateral thermal resistance as TSVs change the isothermal profiles of each other, and the models for TSV array or farms must be TSV space dependent. Model calibration is usually required to take into account this variance. Third, we show that the thickness of the insulation layer has limited influence on the accuracy of the proposed model in many practical cases and does not need to be calibrated. In this work, we focus on developing a physics-based analytical expression for the lateral thermal resistance of TSVs and TSV arrays in terms of physical and material parameters. The proposed analytical lateral thermal resistance model is validated by the commercial FEM tool - COMSOL 4.1 [13], a tool that accurately captures the characteristics

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of the 3D stacked chip structures with practical material properties. Experimental results conducted on a single TSV and array of TSVs demonstrate the accuracy of the proposed method against the FEM analysis results.

The paper is organized as follows: Section II discusses the problem formulation for lateral thermal modeling. Section III describes the mathematical formulation of the closed form expression of the lateral thermal resistance of the TSVs. The experimental results are discussed in Section IV. Section V concludes the paper.

II. PROBLEM FORMULATION

Finite difference based method is a popular approach for thermal analysis [14]. This numerical approach uses mesh grids to discretize the partial differential equations from the heat diffusion dynamics. For thermal modeling of 3D chip structure, it is important to incorporate TSVs into the thermal model as they significantly change the thermal profile of the 3D chip [9], [11], [15]. However, to capture the small feature size of the TSV, like diameter of TSV and thickness of the insulation layer (liner) of TSV, very fine mesh grids are required. This significantly increases the model complexity and the cost of simulation. For example, the radius of a TSV typically ranges from $10\mu m$ to $100\mu m$ while the thickness of the liner ranges from 2% to 10% of the radius of the TSV [12], [16]. As a result, to make the thermal grids as small as a few μm can lead to very huge thermal equations, which typically is not necessary. Therefore, large grid sizes can be used for the finite difference process, resulting in a few TSVs inside a grid or cell. One such example is shown in Fig. 1 in which a TSV is placed in one cell.

The vertical resistance for the TSV model can be computed by:

$$R_v = \frac{L}{kA} \tag{1}$$

where L is the TSV length in the vertical direction, $A = \pi r^2$ is the cross section area of the TSV cylinder in the vertical direction and k is the thermal conductivity of the TSV material. In this paper, we focus on developing the analytical expression for the thermal resistance in the lateral direction in terms of physical and material parameters. For a TSV array or farms, the vertical resistance can be computed as $R_{v,array} = \frac{L}{k_{eff}A}$, where k_{eff} is the effective thermal conductivity, which depends on the ratio of the TSV areas versus the total areas considered [10].

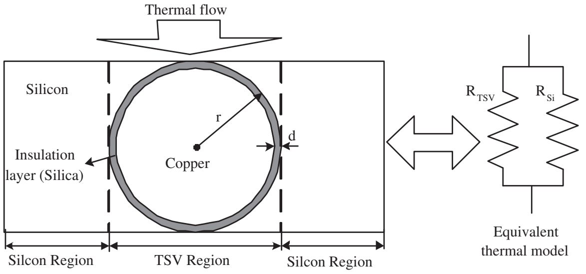


Fig. 1. A top view of TSV cell with copper core and insulation layer

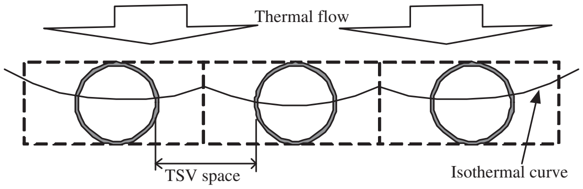


Fig. 2. Top view of TSV array built using individual TSV cells

The top view of a TSV cell is shown in Fig. 1. It consists of a TSV in the center of the cell surrounded by silicon region on either side. We assume the TSV is made of copper and is surrounded by a layer of silicon dioxide which acts as the insulation material. In the vertical direction, the copper core serves as a good thermal conductor for heat transfer from the inside. However, in the lateral direction , the insulation layer, although very thin, can have a large influence on the thermal resistance.

Let R_{TSV} and R_{Si} represent the lateral thermal resistances of the TSV region and the silicon region respectively. The lateral thermal resistance of the TSV cell can be expressed as a parallel combination of the two resistances as shown in Fig. 2.

The TSV cell shown in Fig. 1 can be used to build any TSV array as shown in Fig. 2. The space between two TSVs (TSV space) in the array is the total width of the silicon region of each TSV cell. The lateral thermal resistance model of one TSV cell can thus be extended to compute the lateral thermal resistance of a TSV array of any scale.

The following section discusses the closed form expression for the lateral thermal resistance of the TSV.

III. ANALYTICAL EXPRESSION FOR LATERAL THERMAL RESISTANCE OF TSVS

A. Mathematical derivation of the closed form expression

To determine the closed form expression for the lateral thermal resistance of the TSV region, we start with the following three major assumptions:

1. Inside the insulation layer, majority of the isothermal curve is parallel to the insulation layer, which means that the lateral thermal flow is always vertical to the insulation layer as shown in Fig. 3.
2. The lateral thermal resistance of the silicon region contributed by the four corners of the TSV region is small compared to the TSV and is not considered while formulating the closed form expression.
3. Inside the copper core, the heat flow is straight as shown in Fig. 3, and the detour of the heat flow close to the insulation layer is negligible.

With these assumptions, we can calculate the resistance across a small portion of the insulation layer of the TSV as shown in Fig. 4. Considering the symmetry of the entire structure, the thermal resistance going through the insulation layer is:

$$R_{ins} = 2\int_{r-d}^{r} \frac{\rho_{ins} dl}{\pi l h} \tag{2}$$

where r is the radius of cross section of the TSV, d is the thickness of the insulation layer, h is the height of the cell, l

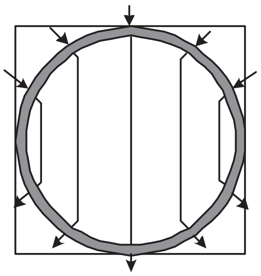


Fig. 3. Direction of lateral thermal flow (arrows) across the TSV region

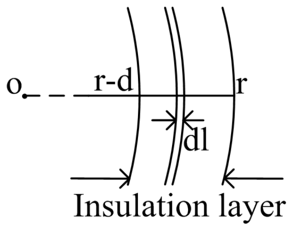


Fig. 4. Thermal resistance calculation across the insulation layer

is the position variable across the insulation layer, ρ_{ins} is the thermal resistivity of the insulation material and R_{ins} is the calculated thermal resistance of the insulation layer.

Using $\alpha = d/r$ as the ratio of the insulation layer thickness to the TSV radius, the equation (2) reduces to a closed form expression:

$$R_{ins} = -\frac{2\rho_{ins} ln(1-\alpha)}{\pi h} \tag{3}$$

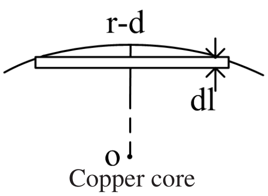


Fig. 5. Thermal resistance calculation across the TSV core

Assuming the heat flow is straight as shown in Fig. 3 and considering the symmetry of the structure, the lateral thermal resistance across a small portion of the copper core as shown in Fig. 5 is given by:

$$R_{cu} = \int_{0}^{r-d} \frac{\rho_{cu} dl}{h\sqrt{(r-d)^2 - l^2}} \tag{4}$$

where ρ_{cu} is the thermal resistivity of the copper core of the TSV, and $r-d$ is the radius of the copper core. Considering the symmetry of the entire structure, the lateral thermal resistance of the copper core is:

$$R_{cu} = \frac{\rho_{cu}\pi}{2h} \tag{5}$$

Therefore, from assumptions 1-3, the lateral thermal resistance in the TSV region in a TSV cell can be written as:

$$R_{TSV} = -\frac{2\rho_{ins} ln(1-\alpha)}{\pi h} + \frac{\rho_{cu}\pi}{2h} \tag{6}$$

Equation (6) shows that the value of lateral thermal resistance in the TSV region is proportional to $ln(1-\alpha)$ and $1/h$. This implies that the lateral thermal resistance is directly proportional to α and inversely proportional to the thickness.

The lateral thermal resistance of the entire TSV cell is the parallel combination of the thermal resistance of R_{TSV} and R_{Si}. This equivalent circuit model is shown in Fig. 1. Since the width of the silicon region vertical to the thermal flow is rP where P is the ratio of the TSV space to TSV radius r, neglecting the bending of isothermal lines close to TSVs, the lateral thermal resistance of the silicon region is:

$$R_{Si} = \frac{2\rho_{si}}{Ph} \tag{7}$$

Therefore, the total lateral thermal resistance of the TSV cell is:

$$R_{TSVcell} = R_{TSV} // R_{Si} \tag{8}$$

B. Model accuracy analysis and calibration

The derived analytical expression given in (8) is based on some assumptions and therefore will have some inaccuracies in some practical cases.

1. The lateral thermal resistance in equation (8) is based on the assumption that the isothermal curve is not bent in the silicon region in the TSV cell. However, due to the presence of TSVs, the isothermal curve has to be bent as shown in Fig. 2. Depending on the ratio of TSV space to TSV radius (P), the isothermal curve could be bent differently. Thus, the value of R_{Si} depends on the ratio of TSV space to TSV radius. This has not been captured by the closed form model.
2. The thickness of the insulation layer can influence model accuracy. If the insulation layer is too thick, the isothermal profile in the insulation layer may change, and majority of the heat flow will no longer be vertical to the insulation surface. Thus, the thermal flow in the tangential direction inside the insulation layer will not be negligible. On the other hand, if the insulation layer is too thin, the model accuracy may go down. As the insulation layer gets thinner (for instance, as α tends to 0), the lateral thermal resistance from the silicon part in the TSV region becomes significant and will need to be accounted for.

We first consider the errors caused by the variation of the space between two TSVs. This space is normally 2 to 6 times the radius of the TSV (the ratio of TSV space to TSV radius $P \in [2, 6]$) [1], [16], [17]. The isothermal curve is strongly influenced by this variation. Thus, to capture the influence of the space between the TSV arrays, model calibration based on numerical data is required to enhance the model accuracy. The modified lateral thermal resistance can be written as:

$$R_{TSVcell,cal} = R_{TSVcell}\theta \tag{9}$$

where θ, the modification factor, can be written as a linear function of the ratio of TSV space to TSV radius (P).

$$\theta = \beta_1 P + \beta_2 \tag{10}$$

β_1 and β_2 could be determined by linear fitting technique using just two data points from the measured data of lateral thermal resistance. In the following section, the closed form model is shown to be accurate with the linear modification factor θ.

Although the thickness of the insulation layer affects the model accuracy, its influence is limited to 2% to 10% of the TSV radius, the range of practical thickness of the insulation layer [12], [16]. Thus, the equation (6) is valid since our assumptions for deriving it are not violated for the practical thickness of the insulation layer within this range. Experimental results will show that the calculated thermal resistance error of the TSV cell due to the variation of the insulation layer thickness in this range is acceptable and does not need further calibration.

In this paper, we consider only one active layer and lateral direction in our model. For TSVs stacked across multiple layers with different materials, we can build the lateral TSV model for each layer. The final thermal model can be built by connecting lateral TSV models from each layer in the vertical direction as done in [12].

IV. NUMERICAL RESULTS AND ANALYSIS

Experiments are performed using COMSOL 4.1 software on a Linux server with 1.6GHz quad-core CPU, and 16GB memory and the results are compared against our proposed model.

A. *Experimental results of a TSV cell*

1) Experimental setup: To measure the lateral thermal resistance using COMSOL, we define a structure as shown in Fig. 6. A power source of $10^{-4}W$ is on the front face (top) of the structure and the convection surface with heat exchanging rate of $1000W/(m^2K)$ is on the back face (bottom). The back face is the only face that exchanges heat with the surroundings. All the other faces (left and right faces) have no heat exchange with the environment, and thus the lateral thermal resistance R_{Therm} of the entire structure in the direction of thermal flow can be measured by:

$$R_{Therm} = \frac{\Delta T}{q} \tag{11}$$

where ΔT is the temperature difference across the structure (from the front face to the back face), and q is the corresponding power flow.

The structure can be divided into 3 blocks where block1 and block3 are the silicon blocks, and block2 is the TSV cell block sandwiched between block1 and block3 as shown in Fig. 6. The figure also shows the isothermal curves from COMSOL simulation where the direction of thermal flow is represented by short arrows perpendicular to the isothermal curves. It can be seen that the isothermal curves are bent close to the location of TSV and the majority of the isothermal curves at the location of the TSV overlapping with the insulation layer. This shows that most of the heat flow is perpendicular to the insulation layer which is in line with the assumptions made in the previous section. In our experiments, the radius of the TSV (from the center to the outer interface between silicon and insulator) is fixed at $r = 25um$ and the height of the structure is fixed at $h = 50um$. The thickness of the insulation layer varies from $0.5um$ to $2.5um$ (2% to 10% of r). The width of the silicon region, denoted by rP (r is the TSV radius, P is the ratio of TSV space to TSV radius) in Fig. 6, varies from 2 to 6 times the TSV radius. Physically, the value of P represents the space between the TSVs in a TSV array built with this TSV cell. We study how the variation of P influences the accuracy of the proposed model for a TSV cell.

The lateral thermal resistance of the TSV cell can be measured as:

$$R_{TSV} = \frac{\Delta T}{q} - R_{SerSi} \tag{12}$$

where R_{SerSi} is the thermal resistance of the silicon region in the thermal flow direction. This thermal resistance is in series with the thermal resistance of the TSV cell. Here, $R_{SerSi} = 2\rho_{Si}/W$ represents the series connection of the two silicon blocks where the thermal resistance of each one is denoted as ρ_{Si}/W. W is the width of the blocks in the thermal flow direction and this is shown in Fig. 6. In the following subsection, the calculated lateral thermal resistance is compared against the measured data based on FEM results to validate the proposed closed form thermal resistance model.

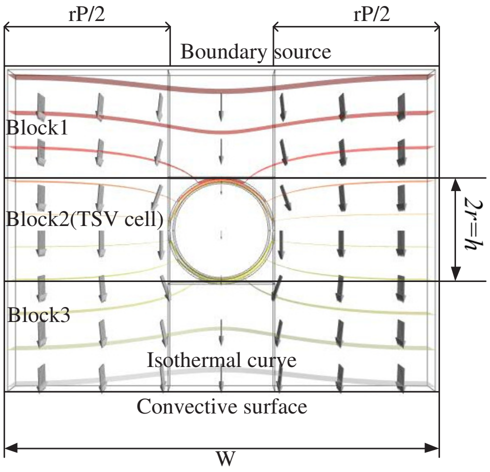
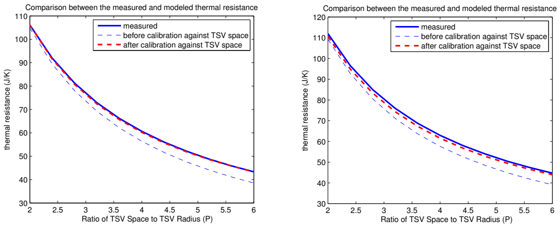


Fig. 6. Isothermal curve of the TSV cell under test

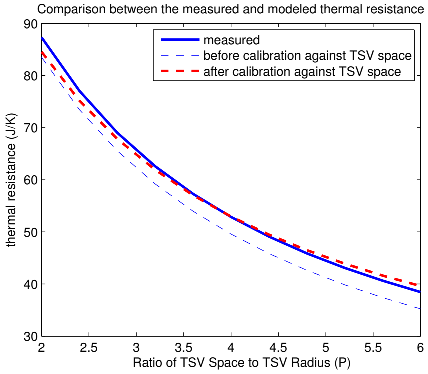
2) Result analysis and discussion: We first simulate the steady state temperature response of the structure using COMSOL. The lateral thermal resistance can be measured using equation (12). The modeled lateral thermal resistance before calibration can be calculated directly based on the material and geometry of the structure using equation (8). To determine the coefficient of the calibration factor (β_1 and β_2), we need to use the measured thermal resistance data of at least two TSV cells with different P. The values of P we choose for model calibration are $P_1 = 2$ and $P_2 = 6$. To reduce the calibration error under different values of insulation layer thickness ranging from $0.5um$ to $2.5um$, we choose the measured data of the structure with insulation layer thickness as $1.5um$, which is in the middle of the range: $0.5um$ to $2.5um$. Thus, the calculated coefficients of the linear function θ is computed as: $\beta_1 = 0.0279$, $\beta_2 = 0.956$.

In both Fig. 7 (a) and (b), the solid line shows measured lateral thermal resistance, the finer dash line shows the calculated result from the model before calibration, and the bond dash line shows the calculated result from the calibrated model. Our observations are as follows:



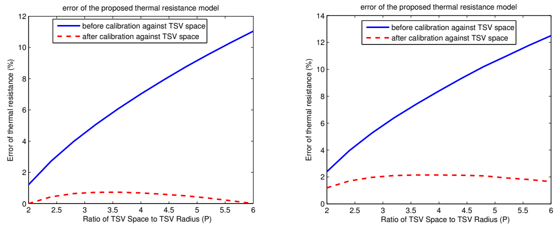
(a) thickness of the insulation layer is $1.5um$

(b) thickness of the insulation layer is $2.5um$



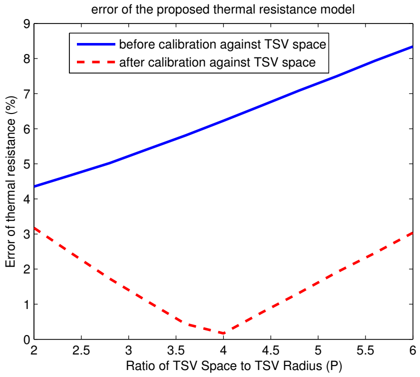
(c) thickness of the insulation layer is $0.5um$

Fig. 7. Comparison of the proposed model and the measured data



(a) thickness of the insulation layer is $1.5um$

(b) thickness of the insulation layer is $2.5um$



(c) thickness of the insulation layer is $0.5um$

Fig. 8. Error of the proposed model (before calibration and after calibration)

1. The model before calibration deviates from the measured data because of the modified isothermal lines introduced by the presence of TSVs.
2. Model calibration significantly increases the accuracy of the modeled thermal resistance in the targeted range of TSV space.

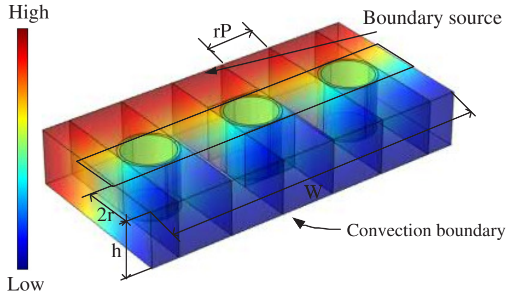
The relative model error with different TSV space is shown in Fig. 8. It indicates that without calibration, the error keeps increasing as the space between the TSVs increases. After applying the calibration, the model error reduces significantly and the smallest error is found for the structure that has insulation layer thickness of $1.5um$. This is because the calibration is directly applied to the measured data of this type of structure. For structures with different insulation layer thickness on TSVs, the error increases and the maximum error is found to be 2% to 3%, which is an acceptable error margin. This result confirms that variations in the insulation layer thickness of TSVs (of 2% to 10% of TSV radius) does not bring in significant error to the model. Thus, it is not necessary to calibrate the model for various value of this parameter in most practical cases. Hence, once the lateral thermal resistance model of a TSV cell is calibrated with different P, it can be reused to build the model for any TSV array.

B. Experimental results for TSV arrays

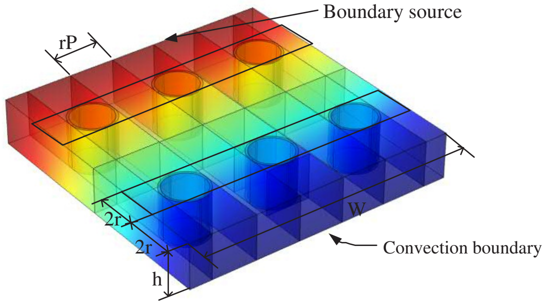
1) Experimental setup: Having validated the lateral thermal resistance model for a TSV cell in the previous section, we now compute the lateral thermal resistance in the thermal flow direction of a TSV array. For this purpose, we consider two examples: a 1D TSV array and a 2D TSV array as shown in Fig. 9 and compare the measured lateral thermal resistance against the modeled value for both the arrays. The heat source and the convection boundary is set up in the same way as before: $10^{-4}W$ at the front face and $1000W/(m^2K)$ at the back face. COMSOL 4.1 is used to simulate the temperature profile of the TSV array and that is compared against the lateral thermal resistance modeled by (12).

2) Result analysis and discussion: The results for the TSV array are obtained for a TSV radius of $r = 25um$, insulation layer thickness of $d = 2.5um$ (10% of the TSV radius) and a block height of $h = 50um$. The results for the 1D and 2D arrays are summarized in Table I and Table II respectively. The lateral thermal resistance is measured under different scenarios by varying the space between TSVs from $50um$ to $150um$. This corresponds to the ratio of TSV space to radius (denoted as P) of 2 to 6.

For the 1D TSV array shown in Fig. 9 (a), Table I shows the measured lateral thermal resistance. The lateral thermal resistance is modeled using equation (12) with $R_{Si} = 2\rho_{Si}/W$, where W is the width of the TSV array as indicated in Fig. 9 (a). Since the TSV array is a parallel combination of 3 TSV cells, the modeled lateral thermal resistance for this array can be calculated as: $R_{TSVcell,cal}/3$ where $R_{TSVcell,cal}$ is calculated using equation (9). The results in Table I show that



(a) 1 D TSV array



(b) 2 D TSV array

Fig. 9. TSV array structures used for lateral thermal resistance validation

the modeled thermal resistance closely matches the measured data for the 1D TSV array.

TABLE I

COMPARISON OF MODELED AND MEASURED LATERAL THERMAL RESISTANCE OF 1D TSV ARRAY

P	Measured(K/J)	Modeled(K/J)	Error
2	37.30	36.87	1.15%
4	20.96	20.66	1.43%
6	14.91	14.66	1.68%

Table II shows the measured total lateral thermal resistance of the 2D array as indicated by the enclosed region in Fig. 9 (b). The lateral thermal resistance is modeled using equation (12) where $R_{Si} = 4\rho_{Si}/W$ and W is the width of the TSV array as indicated in Fig. 9. The space between the two 1D TSV arrays in Fig. 9 lines up with the direction of the thermal flow and it does not influence the lateral thermal resistance because it does not change the lateral isothermal lines that are perpendicular to the thermal flow. Hence, the modeled resistance for the 2D array is $2R_{TSVcell,cal}/3$, as it is a series combination of two 1D arrays shown in Fig. 9 (a). The results show that the modeled thermal resistance closely matches the measured data for the 2D TSV array as well.

TABLE II

COMPARISON OF MODELED AND MEASURED LATERAL THERMAL RESISTANCE OF THE 2D TSV ARRAY

P	Measured(K/J)	Modeled(K/J)	Error
2	74.62	73.74	1.18%
4	41.35	41.32	0.07%
6	28.81	29.32	1.68%

V. CONCLUSION

In this paper, we have proposed a simple yet accurate physics-based analytical thermal resistance model for lateral TSV thermal resistance. Our research shows that lateral TSV model is not only a function of the geometry of the TSV such as radius and thickness of liner, but also strongly depends on the space between TSVs because of changes in the isothermal curves when TSVs are placed at different locations with respect to each other. With the new lateral TSV thermal resistance model, one can build more compact grids for finite difference based analysis that considers the effect of TSVs. The compact models can also be used for architecture and system level thermal design and optimization. Experimental results show that the proposed TSV model, which is a function of the TSV geometry and space between TSVs, can lead to very small errors compared to the detailed numerical analysis.

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