Physics-Based Full-Chip TDDB Assessment for BEOL Interconnects *

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ABSTRACT

As technology advances, Time-Dependent Dielectric Breakdown (TDDB) has become one of the major reliability threats for Copper/low-k interconnects. This article presents a novel approach, techniques, and flow for the physics-based chip-scale assessment of backend low-k TDDB. In our work, the breakdown development is considered as the complementary combination of electric current path generation by means of diffusing metal ions and field-based hoping conductivity of the current carriers. It replaces the widely accepted across-layout electrostatic field based TDDB assessment. As a result, the model generated time-to-failure (TTF) is governed by kinetics of the electric current path generation, which is controlled by a time-dependent minimum metal ion concentration in the inter-metal dielectrics (IMD) gap-fill. Finite element analysis (FEA)-based simulations are used for populating the set of lookup tables, which provide a time to breakdown for any interconnect pattern with given geometries and voltages. A pattern-matching technique is used for extracting from the layout all patterns belonging to different classes of pattern shapes with different geometries, locations and electric loads. Experimental results obtained on a test chip show that upon the calibration the proposed flow provides a capability to evaluate chip-scale low-k TDDB reliability based on the calculated TTF and detect most leaking shapes in the layout.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

1. INTRODUCTION

With aggressive technology scaling accompanied by employment of new advanced materials, Time-Dependent Dielectric Breakdown (TDDB) is becoming, a second, after electromigration (EM), killer of on-chip interconnects. In general, the TDDB is a failure mechanism in back-end-of-line interconnects (BEOL), when the inter-metal dielectric (IMD) breaks down as a result of long-time application of relatively low electric field (as opposite to the hard breakdown, which is caused by strong electric field). The breakdown is caused by formation of a conducting path through the IMD oxide between metal lines due to electron tunneling current. It results in a significant leakage increase that degrades the circuit performance and causes the chip operation failure. Early works on TDDB have been mainly focused on the gate oxide TDDB, caused by the excessive electric fields in thin gate oxides. In contrast, TDDB in the BEOL stacks has not been a concern until recent years, due to wide dielectric spacing between metal lines and high electric strength of the inter-metal silicon dioxide. This situation has changed with the layout feature dimensions shrink and design complexity growth. The drastically reduced wiring pitches lead to escalating electric fields among interconnects. In order to decrease the RC delay, dynamic power consumption, and cross-talk noise, porous low-k dielectric materials, with the dielectric constant $k < 3$, have been introduced, [1]. However, the low-k materials are characterized by poor mechanical, thermal, and electrical properties in comparison with silicon dioxide, [2]. Some of the process steps such as chemical mechanical planarization (CMP) and plasma etch can potentially damage the dielectric sub-surfaces regions, generating charge carrier traps and assisting the conduction, [3]. As a result, the IC chips integrated with the copper/low-k interconnects tend to be vulnerable to TDDB failure.

Great efforts have been made to model TDDB degradation, [4–8]. However, there is still no universal agreement between the proposed field acceleration models which are based on different TDDB mechanisms, [4]. The underlying physics of the dielectric breakdown is still not completely defined. The frequently employed the thermochemical E-model [5] and $1/E$-model [6] were initially developed for gate oxides, where the E-model describes weak bond breakage due to thermochemical heating and the $1/E$-model refers to high energy hole injection induced damage. These models were later examined toward extension on the copper/low-k interconnect TDDB. The major difference between TDDB in low-k BEOL dielectrics and gate oxides is the presence of metal ions in the former interior. Accordingly, the $\sqrt{E}$-model was first proposed for metal-SiN-metal capacitors [7], and further employed for the low-k TDDB, assuming that the copper ions play a major role in dielectric breakdown, by Chen and Suzumura *et al.* [8, 9]. Lately, the experimental data collected at the low fields have demonstrated the overly conservative predictions generated by the E and $\sqrt{E}$ models, and too optimistic predictions with the $1/E$ model [4]. In addition, as it was mentioned in [4], the breakdown event depends on the formation of the conducting path of traps connecting the two electrodes (metal lines). However, all proposed TDDB models fail to describe the kinetics of conduction path generation. Majority of currently employed TDDB assessment approaches are based on calculations of the across-layout electrostatic fields and, thus, cannot provide any kind of the interconnect lifetime assessment.

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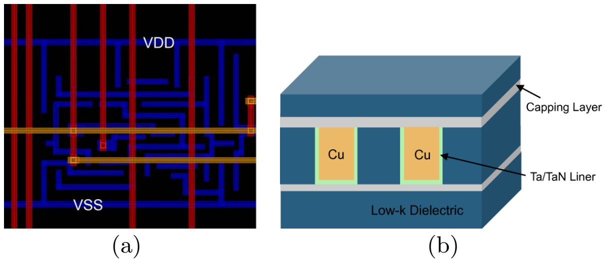


(a) (b)

Figure 1: Layout of on-chip interconnects (blue line: M1, red line: M2, and yellow lines: M3), (a), and cross section of copper/low-k dielectric structure, (b).

Therefore, the development of the backend low-k interconnect TDDB time to failure (TTF) assessment flow is still not addressed task.

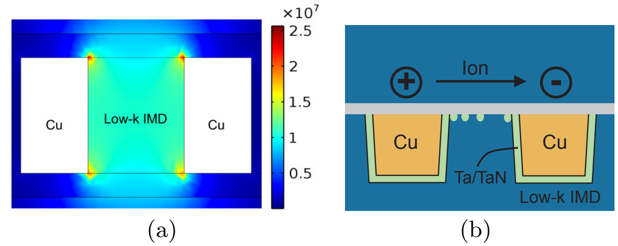
A robust full-chip assessment technique for low-k TDDB is needed for evaluating the amount of the IMD degradation, measured by the leakage current density, and the MTTF during the circuit design. As shown in Fig. 1(a), the copper/low-k dielectric structures are characterized by a wide variety of geometries. The architecture of a metal line, which is comprised of the capping (etch stop) layer, and the diffusion barrier coating the copper bulk shown in Fig. 1(b), may impact the TDDB-induced interconnect lifetime. Distribution of the electric field in IMD gaps effects both the kinetics of the current conducting path generation and the resulting leakage current density. Bashir *et al.*, [10], have assumed a fixed voltage drop between all neighboring metal segments in the proposed full-chip TDDB simulator. However, interconnects in the chip can be categorized as power/ground lines and signal lines. Patterns with the same geometries but different power/ground/signal line combinations, e.g. with the different electric loads, will be characterized by different TDDB activities. Thus, the method proposed in [10] will induce too conservative results. Novel solutions should be developed to mitigate the mentioned problems for full-chip TDDB assessment.

In this work, we propose a novel approach and techniques for physics-based TDDB assessment in backend on-chip interconnects. The development of conduction path in the dielectric between electrodes, which is described by the redistribution of defects (ions), is captured by finite element analysis (FEA)-based solution of a coupled electrostatic and charging particle diffusion problem. The resolved evolution of the minimum ion concentration between metal lines determines the time-to-breakdown of the dielectric. Lookup tables generated from these FEA-based simulations provide a TTF for any kind of interconnect pattern with given geometries and voltages. Groups of interconnect patterns belonging to different frequently used layout pattern shapes are recognized with a pattern-matching tool. The extracted patterns are then identified by different geometries, locations, and types of electric loads. Full-chip TDDB induced lifetime is determined as the minimum TTF of all extracted patterns. This approach can detect the layout locations of the patterns, which are most vulnerable to low-k TDDB failure that can be further used for the TDDB-aware design optimization.

2. PHYSICS-BASED TDDB MODEL FOR LOW-K BEOL STACK

2.1 The model for electric path generation

Inter-layer dielectric (ILD) and inter-metal dielectric (IMD) are the two types of low-k dielectrics, which represent, respectively, the isolation between two metal layers and between metal lines in the same layer. Because the thickness of ILD is generally larger than the metal lines space, we focus on the breakdown of dielectrics between metal lines located in the same layer. Fig. 1(b) shows a cross section of the typical copper/low-k dielectric structure with two parallel metal lines. The experiments demonstrate that TDDB failures take place mostly at the interface between the capping layer and the low-k dielectrics [11,12]. The 3-D simulation of the distribution of electrostatic field in the geometry shown in Fig. 1(b) with the COMSOL Multiphysics FEA tool, demonstrates the electric field enhancement near the cap/IMD interface, Fig. 2(a). Besides, the ions are reported to diffuse much faster at the interface than in the bulk dielectric, as shown in Fig. 2(b), which is possibly due to the defects generated at the surface during CMP process, [12]. Based on these findings, in the following analysis we consider 2D diffusion of the metal ions along the cap/IMD interface between the oppositely charged metal lines.



(a) (b)

Figure 2: Cross section of copper/low-k dielectric structure: Result of 3D FEA simulation for the electric field (V/m) distribution in IMD between parallel metal lines with $spacing = 100nm$ and $V = 1.1V$, (a), and ion migration along the cap/IMD interface, (b).

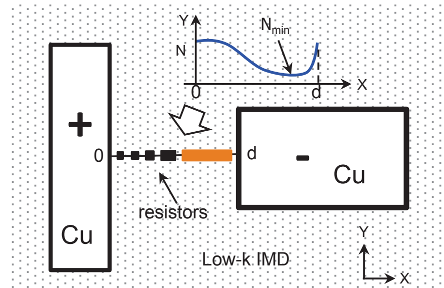


Figure 3: Ion concentrations and the corresponding resistors in IMD along $(0, d)$.

The effect of copper ions on the intra line leakage is debated in the literature. Recently, a number of experimental results have reported that Cu can hardly diffuse out of the Ta/TaN barrier under chip operating conditions [11,13]. Instead, Ta ion diffusion has been observed in the low-k materials. The diffusion of metal ions can generate defects in the dielectric serving as potential centers for localization of the electrons coming from the metal electrodes. An electric conductivity is represented by electron jumps between neighboring centers (hoping conductivity). A local conductivity is proportional to the probability of the electron jumping between the neighbor centers, which exponentially depends on the distance between the centers [14]:

$$\sigma_{ij} \sim \Gamma_{ij} = \gamma_{ij}^{0} exp\left\{-\frac{2r_{ij}}{a} - \frac{\varepsilon_{ij}}{k_B T}\right\} \quad (1)$$

Here, r_{ij} is the distance between i and j centers, a is the radius of electron localization at this type of centers (analog of the Bohr's radius), which can reach 100, ε_{ij} is the energy barrier between centers, $k_B T$ is the thermal energy. All connected centers form the resistors network, with the resistor

between i and j centers equals to

$$R_{ij} = R_{ij}^{0} exp\left\{\frac{2r_{ij}}{a} + \frac{\varepsilon_{ij}}{k_B T}\right\} \quad (2)$$

In a 2D system, the distance r_{ij} is determined by:

$$r_{ij} = N(x,y,t)^{-\frac{1}{2}} \quad (3)$$

where $N(x,y,t)$ is the ion concentration at the considered interface. Fig. 3 shows the schematics of the distribution of ion concentration and corresponding resistor network at an arbitrary instant in time in IMD along a path $(0,d)$ connecting metal electrodes. It is clear that electrons moving from the cathode to anode will meet the biggest resistors at the locations characterized by the largest distances between centers. Since the difference in the distances between centers results an exponentially large difference in the resistors, it is reasonable to conclude that the total resistance of the path $(0,d)$ depends on the largest resistor, i.e. the minimum ion concentration. The distribution of the normalized ion concentration $N_{\text{norm}}(x,y,t) = N(x,y,t)/N_0$ is governed by the diffusion of ions in an electric field [15]:

$$\frac{\partial N_{\text{norm}}}{\partial t} = -\nabla J \quad (4)$$

$$J = -D\nabla N_{\text{norm}} + \frac{qDEN_{\text{norm}}}{k_B T} \quad (5)$$

with boundary conditions:

$$N_{\text{norm}}(x=0) = N_{\text{norm}}(x=d) = 1 \quad (6)$$

Here J is the metal flux, $D = D_0 exp(-Ea/k_B T)$ is the diffusion coefficient, Ea is the activation energy for metal ion diffusion, k_B is the Boltzmann constant, T is the temperature, q is the electric charge and E is the electric field.

Table 1: Parameters used in FEA simulation

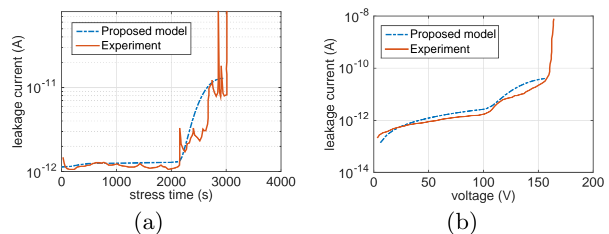
Parameter	Value	Parameter	Value
D_0	$2\times10^{-11}\text{m}^2/\text{s}$	E_a	0.9eV
k	2.9	k_B	$1.38\times10^{-23}\text{J/K}$
T	333K	V_{DD}	1.1V

Metal line structure shown in Fig. 3 is used as an example for simulating the electric path generation. Time-dependent distribution of the metal ions is obtained from the COMSOL-based solution of the coupled electric field and diffusion equations (4)-(6). The employed parameter values are listed in Table 1. Before applying the electric field stressing, the metal atoms are allowed to diffuse into the dielectric for a short period of time at high temperatures (T=400K and t=1e5s in this case). This step should mimic the atomic thermal diffusion, which occurs at the high temperature processing steps including annealing. The simulation results are demonstrated in Fig. 4. Fig. 4(a)-Fig. 4(c) show the contour lines representing the evolution of the concentration field $N_{\text{norm}}(x,y,t)$ at three instances in time: before a continuous chain of ions characterized by the minimum spacing (N_{norm}=1) is formed between metal lines, at the moment when this chain is formed for the first time, and at longer time when the area with N_{norm}=1 is expanded along the anode edge. Evolution of the ion distribution along the fastest diffusion path, which is the path connecting the centers of the neighboring metal lines, is shown in Fig. 4(d). It can be seen that the initial ion distribution, which was resulted by the thermal diffusion, is shifting as a whole with the duration of time toward the anode keeping unchanged the minimum concentration $N_{\text{norm}}^{\text{min}}$, which is determined by the most separated ions. Simultaneously, the increasingly larger area is occupied with the closed packed ions: N_{norm}=1. It lasts until the instance in time when the region with $N_{\text{norm}}^{\text{min}}$=1 reaches the vicinity of anode edge. Starting this moment t_1 the minimum concentration starts to increase drastically. Finally, the ion concentration becomes uniformly distributed with N_{norm}=1 between the electrodes. Based on this observation, we introduce two important time instances $\boldsymbol{t_1}$ and $\boldsymbol{t_2}$, Fig. 4(e):

- $\boldsymbol{t_1}$: The instance in time when $N_{\text{norm}}^{\text{min}}$ starts to increase (drastically).
- $\boldsymbol{t_2}$ (TTF): The instance in time when $N_{\text{norm}}^{\text{min}}$ reached 1 and the resistivity is uniformly distributed between electrodes.

Since the largest resistor, corresponding to $N_{\text{norm}}^{\text{min}}$, dominates the total resistance of the leakage path, the dielectric will start to degrade from t_1, leading to significant increase in leakage current. After the instance in time t_2, other mechanisms governed by excessive Joule heating will generate the catastrophic dielectric failure. Therefore, the instance in time t_2 represents the time-to-failure (TTF) of the low-k dielectric in this particular metal gap.

2.2 Model calibration



(a) (b)

Figure 5: Current-voltage leakage characteristics for constant voltage (TDDB) stress, (a), and ramped voltage stress, (b), with experimental data from [13].

The developed model of the electric path generation and evolution allows to come out with the formalism of the leakage current evolution. As it was mentioned above the neighboring ions characterized by the largest separation provides the largest "resistivity" for the electrons hopping between metal ions. Assuming that the potential barriers between neighboring centers do not depend on the distance between them ($\varepsilon_{ij} = \varepsilon$), and accepting the Poole-Frenkel mechanism of the field-induced barrier lowering, we can derive the expression for the current density evolution:

$$j(t) = j_0 E exp\left\{-\frac{2}{a\sqrt{N_{\text{norm}}^{\text{min}}(t)\cdot N_0}} - \frac{\varepsilon - q\sqrt{qE/(\pi\varepsilon_{\text{perm}})}}{k_B T}\right\} \quad (7)$$

Here, $\varepsilon_{\text{perm}}$ is the dielectric dynamic permittivity.

The total leakage current can be obtained by integration of leakage current density over the whole shape contour. Due to the limited space of the conference paper, the details of the leakage analysis and corresponding calibration of the model will be discussed in the journal version of this paper. For now we just mention that the leakage currents calculated with the calibrated model demonstrate good agreement with experimental results, Fig. 5. It should be mentioned that the model should be calibrated with a set of test structures just once per the technology node and foundry.

3. NEW FULL-CHIP BACKEND LOW-k TDDB ANALYSIS

In this section, we present the proposed new full-chip backend low-k TDDB analysis method based on the developed

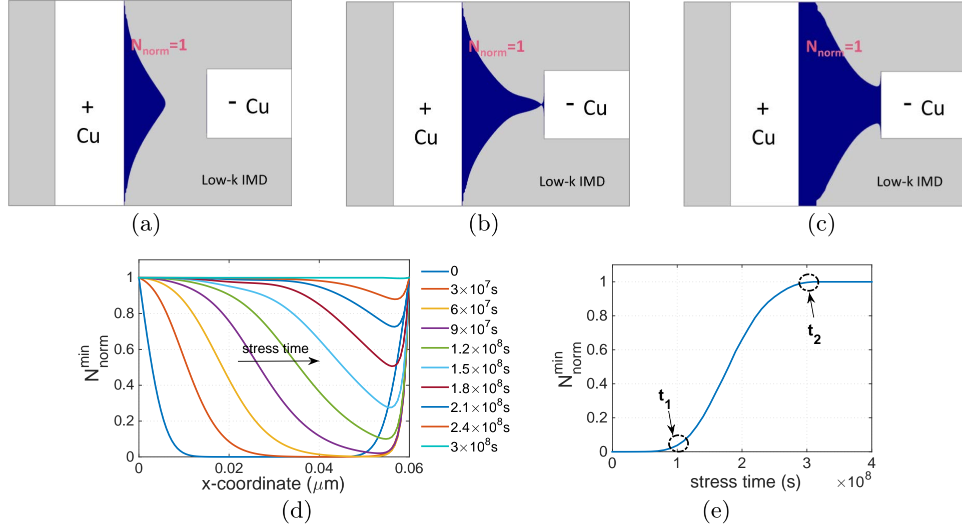


Figure 4: FEA simulation results of contour shapes for normalized ion concentration $N_{\rm norm} = 1$ in IMD between electrodes at different instants in time (a)-(c), changes in ion concentration distribution in IMD along the fastest diffusion path with time, (d), and corresponding time dependent minimum ion concentration, (e), with line spacing $d = 60nm$, $V(x = 0) = V_{\rm DD}$, and $V(x = d) = 0$.

electric path generation model. Fig. 6 illustrates the analysis flow, which can be achieved through two major steps: one is the generation of lookup tables that provide TTF for any interconnect pattern with given geometries and voltages; another is the pattern matching step that extracts all patterns of interest from the layout along with their geometrical and electrical characteristics. The TDDB induced chip lifetime is then determined by the minimum TTF of all analyzed matched patterns. The details are discussed in the following subsections.

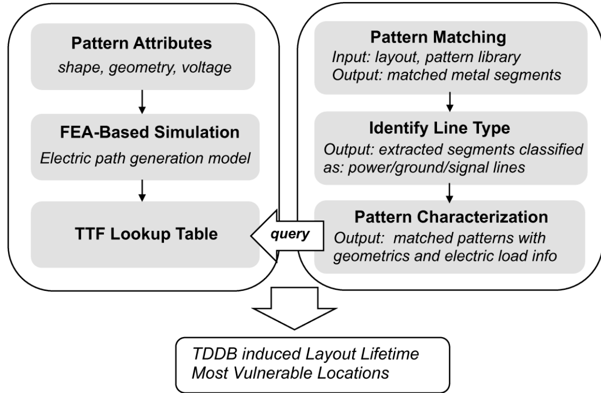


Figure 6: Chip-scale TDDB analysis flow for backend low-k dielectrics.

3.1 Impact of electric load

In this subsection, we discuss the impact of electric loads on low-k dielectric reliability. Interconnects in the integrated circuits are serving as power/ground lines or signal lines. As a result, the interconnect patterns can be characterized by different kind of electric loads according to the following three combinations:

1. **Power, Ground**: As shown in Fig. 7(a) and Fig. 7(e), the dielectric will be stressed with a constant electric field.

2. **Power/Ground, Signal**: Fig. 7(b) and Fig. 7(c) are the schematics of the corresponding voltage waveforms, resulting in a time-dependent electric field in IMD, Fig.7(f).

3. **Signal, Signal**: According to Fig. 7(d), in general cases, the electric fields between neighboring signal lines are time-dependent waveforms similar to Fig. 7(f). A special case that much less likely to happen is the voltage waveforms in Fig. 7(d) are totally opposite, leading to a constant electric field.

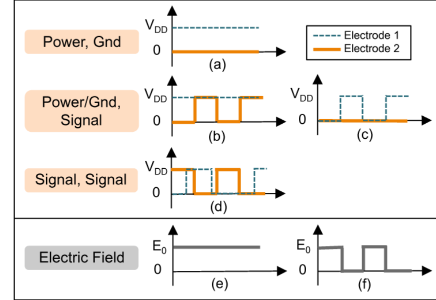


Figure 7: Schematics of different voltage waveforms on two electrodes and the corresponding electric field (assume a uniform field).

Taking, for example, the structure shown in Fig. 3, and selecting line spacing as d=50nm and d=70nm we will analyze the kinetics of $N^{\rm min}_{\rm norm}$ evolution in the IMD gap, loaded with a constant voltage drop or a pulsed voltage drop with a duty cycle=50%. We can observe from Fig. 8 that when the patterns have the same geometries, the flux of metal ions, Eq. (5), is larger in the case of the constant electric stress, which leads to faster $N^{\rm min}_{\rm norm}$ evolution, and thus to a shorter TTF (TTF_1≈3×TTF_2). Besides, when the patterns are stressed with the same voltages, a smaller line spacing results in a shorter TTF (TTF_3≈2×TTF_2). However, under some circumstances, a pattern with a larger spacing and constant electric stress may have a shorter TTF than the pattern with a smaller spacing but loaded with the time-dependent voltage (TTF_1≈1.5×TTF_3). Hence, when analyzing dielectric reliability of IC chips, we need to pay attention to the patterns characterizing by both: the relatively small metal line spacing and constant voltage electric stressing. Note, that the patterns carrying the same voltages, for example

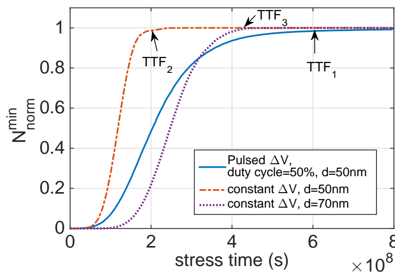


Figure 8: Comparisons of kinetics of $N^{\min}_{\text{norm}}$ evolution in IMD between: 1: line spacing $d = 50nm$, pulsed ΔV with duty cycle = 50% and amplitudes=V_{DD}, 2: $d = 50nm$ and constant $\Delta V = V_{DD}$, 3: $d = 70nm$ and constant $\Delta V = V_{\text{DD}}$

V_{DD}, should be excluded from the analysis. Therefore in the chip-scale low-k TDDB analysis, an attribute of electric loads, in addition to geometries, needs to be added to the extracted patterns. In contrast, existing method assuming a fixed voltage drop between all neighboring metal segments in the layout will generate very conservative results and can probably incorrectly detect the most vulnerable locations.

3.2 Time-to-failure lookup table

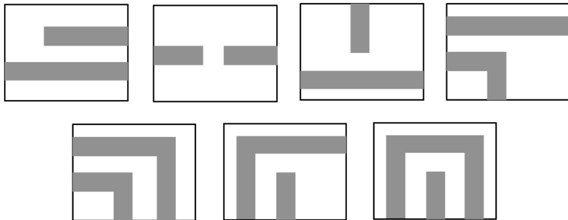


Figure 9: Example of different pattern shapes.

As demonstrated in the Fig. 1(a), the backend interconnects are characterized by a variety of shapes and sizes. In this work, we consider interconnects as groups of patterns belonging to different classes of frequently used layout pattern shapes. Thus, the full-chip reliability analysis can be carried out by independently evaluating the dielectric breakdown of interconnect patterns existed in the layout. The minimum pattern failure time provides the lifetime of the chip due to TDDB, as a short-circuit is generated after the dielectric breakdown. In this case, lookup tables need to be generated, in advance for each technology node, for the TTF of a large number of interconnect patterns with given geometries and voltages, so that a corresponding TTF can be linked to each pattern. Fig 9 shows the example of pattern shapes considered in this work. As it was discussed above, each type of the topologically similar patterns but characterizing by different inter-metal spacing is a subject of the FEA-based extraction of t_1 and t_2 instances in time. The calculated TTF are used for populating the set of corresponding lookup tables.

3.3 Pattern-matching method

This subsection describes the pattern-matching technique followed by the extraction of geometrical and electrical information for each pattern. This process includes following four steps, where the first three steps are carried out by the *Calibre Pattern Matching* integrated with the *Calibre nmDRC*:

1. **Build pattern library:** The pattern library is generated as an input of pattern matching for the frequently used classes of patterns demonstrated in Fig. 9. For each kind of pattern, we vary wire width, length, and spacing within the designed ranges, so that all patterns of interest can be extracted from the layout. Fig. 10 shows the exponential dependence of TTF on spacing when the constant electric stressing is applied, which indicates that the patterns having negligible impact on the chip lifetime can be excluded from analysis in order to reduce database size, as the patterns with the spacing d>$90nm$ in this case.

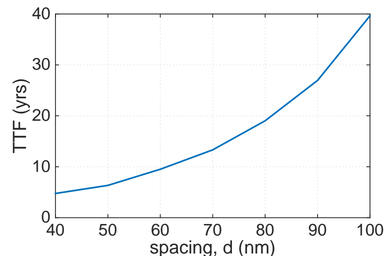


Figure 10: TTF of low-k dielectrics for different line spacing under $\Delta V = V_{\text{DD}}$

2. **Pattern matching:** The *Calibre Pattern Matching* tool is employed to recognize the layout patterns defined in the library. The output is sets of metal segments for matched patterns. Each segment is a group of edges described by pairs of vertices that can reflect the shape and location of the pattern.

3. **Identify line type**: The extracted metal segments are then identified based on their electric functions as *power lines*, *ground lines*, and *signal lines* using the *nmDRC* platform.

4. **Pattern characterization:** As the pattern-matching step generates sets of segments that belong to all recognized patterns, in order to get the information of each pattern, we need to figure out which segments build a pattern. It can be realized by generating the polygons that represent the tightest boundary of each matched pattern during the pattern recognition, so that the interconnect segments locate in the same boundary form a pattern and determine the geometry, location, and voltage load of the pattern.

4. EXPERIMENTAL RESULTS

In our experiments, we use a low power design named *ChipTop* as the test case. *ChipTop* is a processor architecture, which contains cache blocks, I/O standard cells and digital standard cells. It is synthesized using *Synopsys Design Compiler*, and is placed and routed with *Synopsys* 32/28nm *Generic Library* [16] using *Synopsys IC Compiler*. The layout of the chip is shown in Fig. 11.

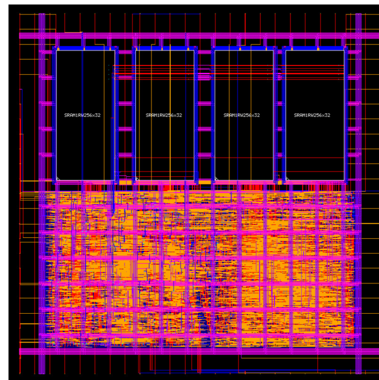
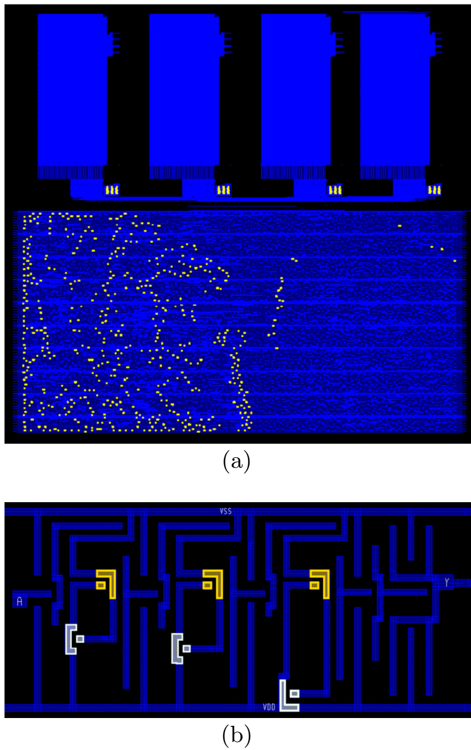


Figure 11: Layout of *ChipTop* architecture.



(a)

(b)

Figure 12: The most vulnerable (yellow dots) locations in M1 layer (blue), (a), and zoom in image of the critical shapes in a delay cell (yellow: worst case; white: TTF comparable to the worst case), (b).

Table 2: Minimum spacing and line types of corresponding interconnect patterns

Metal layer	Spacing	Line type
$M1$	50nm	power/ground/signal
$M2$	64nm	signal
$M3$	67nm	signal

Table 2 lists the minimum spacing for interconnect patterns on M1, M2 and M3 layers and the corresponding electric function of the lines belonging to these minimum spacing patterns. The spacing between interconnects in higher metal layers are much larger than $100nm$, thus according to Fig. 10, these layers can be removed from the TDDB assessment. It can be seen from Table 2 that the M1 metal patterns characterized by the minimum spacing are composed of the power lines, ground lines and signal lines, while the M2 and M3 patterns are composed of signal lines only. We specify the geometries and electric loads of the extracted interconnect patterns and rank their TTFs according to the TTF lookup table. The minimum TTF of these patterns is around 6.5 years, which determines the low-k TDDB induced lifetime of the chip.

The most vulnerable pattern consists of a power line and a ground line, thus, it is stressed by the constant voltage, and has the minimum allowed line spacing of d=$50nm$. Other patterns with minimum line spacing but stressed with the pulsed voltage have the much longer TTFs. All these most critical patterns are located in M1 layer and their distribution is demonstrated in Fig. 12(a). Specifically, we have found that all these shapes come from the delay cells: $DELLN1X2_RVT$, $DELLN2X2_RVT$, and $DELLN3X2_RVT$ in the standard cell library, [16]. Fig. 12(b) shows a zoom-in image of the critical M1 patterns in the $DELLN2X2_RVT$ cell. These detected most leaking paths in the cell indicate the places where one can do optimization, by, for instance, increasing spacing between electrodes.

5. CONCLUSION

In this work, a new physics-based TDDB modeling and assessment method has been proposed and implemented for the copper/low-k interconnects of VLSI chips. The new TDDB model accounts for the kinetics of electric current path generation and evolution in the IMD gap where the evolution of minimum metal ion concentration determines the TTF of the low-k dielectric. The proposed conduction path generation model along with the assumption of the field-based hoping conductivity of the current carriers results in a formalism of the leakage current evolution that can be calibrated with experimental results. For the chip-scale low-k TDDB assessment the FEA-based simulation of the TTF for any layout pattern with different geometries and voltages are employed in order to generate the lookup tables. All patterns of interest are extracted from the layout using pattern-matching technique. Obtained experimental results demonstrate capability of the proposed method to predict the TDDB induced chip lifetime and detect the locations in the layout that are most vulnerable to TDDB failure. The proposed assessment flow can be employed in the reliability-aware circuit design.

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