A Linear Algorithm for Full-Chip Statistical Leakage Power Analysis Considering Weak Spatial Correlation

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ABSTRACT

Full-chip statistical leakage power analysis typically requires quadratic time complexity in the presence of spatial correlation. When spatial correlation are strong (with large spatial correlation length), efficient linear time complexity analysis can be attained as the number of variational variables can be significantly reduced. However this is not the case for circuits where gate leakage currents are weakly correlated. In this paper, we present a linear time algorithm for statistical leakage power analysis in the presence of weak spatial correlation. The new algorithm exploits the fact that gate leakage current can be efficiently computed locally when correlation is weak. We adopt a newly proposed spatial correlation model where a new set of location-dependent uncorrelated variables are defined over virtual grids to represent the original physical random variables via fitting. To compute the leakage current of a gate on the new set of variables, the new method uses the orthogonal polynomials based collocation method, which can be applied to any gate leakage models. The total leakage currents are then computed by simply summing up the resulting orthogonal polynomials (their coefficients) on the new set of variables for all gates. Experimental results show that the proposed method is about two orders of magnitude faster than the recently proposed grid-based method [3] with similar accuracy and many orders of magnitude times over the Monte Carlo method.

Categories and Subject Descriptors

I.6.5 [**Simulation and Modeling**]: Model Development

General Terms

Algorithms

Keywords

dynamic power, statistical analysis, spatial correlation

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1. INTRODUCTION

Leakage power has increased dramatically with the technology scaling and is becoming the dominant part of chip power dissipation [2]. The dominant factors in the leakage currents are the subthreshold leakage current I_{sub} and gate oxide leakage current I_{gate}. The subthreshold leakage current has a rapid increasing rate (about 5X-10X increase per technology generation [5]), and it is highly sensitive to threshold voltage V_{th} variations owing to the exponential relationship between I_{sub} and V_{th}. On the other hand, as gate oxide thickness, T_{ox}, scales down, I_{gate} grows rapidly as I_{gate} has an exponential dependence on T_{ox}.

Both leakage currents are highly sensitive to process variations due to the exponential relation between the leakage current and variational parameters like channel lengths. As process-induced variability becomes large in the deep submicro regime,leakage variations become significant, and traditional worst case and corner based approaches will lead to extremely pessimistic and expensive design solutions. Statistical estimation and analysis of leakage powers considering process variability are critical in various chip design steps to improve design yield and robustness.

Many earlier works have been proposed for full-chip statistical leakage analysis (SLA) considering the process variations such as [9, 13]. When the process-induced variabilities are spatially correlated, the computation cost of the distribution of total leakage of the chip becomes quadratic – $O(n^2)$, where n is number of gates. To mitigate this problem, several approaches have been proposed recently [3, 8, 7, 14]. The work in [3] partitions the whole chip into many grids (the gate variables in a grid are identical.) to reduce the number of variables but at the cost of loosing accuracy. This method works well when correlation is strong. The approach in [14, 15] also explores the strong spatial correlation by reducing the number of variables through principal component analysis (PCA) and applying orthogonal polynomials to represent leakage currents at gate and whole chip levels. The PCA-based approach in [8] only works when random variables are uncorrelated. In [7], a linear time complexity method is proposed, but it assumes symmetric spatial correlation and considers only the channel length variations.

When the spatial correlation is weak, existing approaches like [3, 14] do not work well as the number of correlated variables can't be reduced too much. Recently an efficient method was proposed [18] to address this problem. The method is based on simplified gate leakage models and formulates the major computation task into matrix-vector multiplications via Taylor's expansion. It then applies fast computing methods like Fast Multipole method or pre-corrected

FFT to compute the multiplication. However, this method assumes that the gate leakage currents are purely lognormal, which is not the case as we will show in the paper. Also it can only compute the mean and variances, but not the complete distribution of the leakage.

In this paper, we present a new linear-time algorithm for statistical leakage analysis in the presence of weak spatial correlation. The new algorithm exploits the fact that the leakage current of a gate in the presence of weak spatial correlation is only affected by a few neighboring gates. As a result, the gate leakage current can be efficiently computed by only considering its neighboring gates in a constant time. We adopt a newly proposed spatial correlation model where a new set of location-dependent uncorrelated variables are defined over virtual grids to represent original correlated random variables via fitting. We then compute the statistical leakage current of a gate using this new set of variables. The orthogonal polynomials based collocation method is thus applied and the variational gate leakages and total leakage currents are represented in an analytic form in terms of the random variables, which can give complete distribution. The new method considers both inter-die and intra-die variations and it can work with any spatial correlations. Unlike the existing approaches [3, 7], the new method does not make any assumptions about the distributions of final total leakage currents for both gates and chips. In case of medium and strong correlations, the proposed method can also work in linear time by properly sizing the grid cells so that both correlation locality and accuracy can still be preserved. Experimental results on the PDWorkshop91 benchmarks on a 45nm technology show that the proposed method is about two orders of magnitude faster than the recently proposed method [3] with similar accuracy.

The rest of this paper is organized as follows: Section 2 presents the process variational models and gate leakage models used in this work. Section 3 presents the new spatial correlation models. Section 4 presents our new full-chip statistical leakage power analysis method. Section 5 presents the experimental results and Section 6 concludes this paper.

2. VARITIONAL AND LEAKAGE MODELS

In this section, we present the spatial process variational models and gate leakage models used in this work.

2.1 Spatial variational models

The main process parameter that has big impact on leakage current is the transistor threshold voltage V_{th}. V_{th} is observed to be the most sensitive to effective gate length L and gate oxide thickness T_{ox}. ITRS'08 [2] indicates that the variation of L is a primary factor for device parameter variation, and the number of dopants in channel results in an unacceptably large statistical variation of V_{th}.

Following the existing approaches, we also assume that the process variations of L and T_{ox} follow multivariate normal distributions [16], and both include inter-die and intra-die components. Since T_{ox} is in vertical layout feature dimension, and is caused by chemical mechanical polishing processes, it only depends on local layout density and has no spatial correlation [11]. Therefore, we focus on the spatial correlation of L. In general, the number of process parameters that exhibit spatial correlation can be more than one, and it is understood that this is not a limitation of our approach.

For a gate/module in a chip, we model the variations of L and T_{ox} as the following random variables:

$$\begin{aligned} \Delta L &= \Delta L_{inter} + \Delta L_{intra} \\ &= \sigma_{L,inter}\xi_{L,inter} + \Delta L_{intra}, \end{aligned} \quad (1)$$

$$\begin{aligned} \Delta T_{ox} &= \Delta T_{ox,inter} + \Delta T_{ox,intra} \\ &= \sigma_{ox,inter}\xi_{ox,inter} + \sigma_{ox,intra}\xi_{ox,intra}, \end{aligned} \quad (2)$$

where $\xi_{L,inter}$, $\xi_{ox,inter}$, $\xi_{ox,intra}$ are independent random variables following $N(0,1)$, since ΔL_{inter} and $\Delta T_{ox,inter}$ are the same for all gates in all grids, and T_{ox} has no spatial correlation. On the other hand, ΔL_{intra} is different for each gate, and has spatial correlations. The spatial correlation is modeled by an empirical formulation such as the exponential model [17].

$$\rho(d) = e^{-d^2/\eta^2}, \quad (3)$$

where d is the distance between two grid centers and η is the correlation length. The spatial correlation can be captured by the spatial covariance matrix $\Omega_{n,n}$, where n is the number of gates. The elements in $\Omega_{n,n}$ are modeled as (3), which are only related to d.

As mentioned in Section 1, traditional SLA has $O(n^2)$ complexity in the presence of spatial correlation. There are mainly two kinds of methods proposed to mitigate this problem. The first is the grid-based method [3]. With strong correlation, the number of grids will be much smaller than number of gates, which leads to linear time complexity. But this method will lead to large errors as two gates that are close to each other may belong to different grids. The second approach mitigates this problem using the PCA technique [14]. The errors can be easily controlled during the numerical processes. This method also achieves linear time complexity in case of strong spatial correlation. But the new set of independent variables has no physical meaning. In this paper, we try to address full-chip SLA with weak spatial correlation. At the same time, we introduce a new set of independent variables which has more physical meanings.

2.2 Static leakage modeling

Full-chip leakage current has two major components, I_{sub} and I_{gate}. I_{sub} is exponentially dependent on V_{th}, which is observed to be most sensitive to T_{ox} and L due to short-channel effects. When the change in L or T_{ox} is small, the precise relationship shows exponential dependency on I_{sub}, with the effect of T_{ox} being relatively weak. For I_{gate}, both L and T_{ox} have strong impacts on the leakage currents, which are exponential functions of the two variables.

In our work, we also follow the analytical expressions given in [3], which estimate the subthreshold and gate oxide leakage currents as follows:

$$I_{sub} = e^{a_1+a_2L+a_3L^2+a_4T_{ox}^{-1}+a_5T_{ox}}, \quad (4)$$

$$I_{gate} = e^{a_1+a_2L+a_3L^2+a_4T_{ox}+a_5T_{ox}^2}, \quad (5)$$

where a_1 through a_5 are the fitting parameters for each unique input combination of a gate. Then we use a look-up table to store the fitting parameters. Notice that the exponents of I_{sub} and I_{gate} are not linear functions of L and T_{ox}, which is required by the existing approach [18]. The actually gate leakage currents are taken as the average of the leakage currents from all the states in this work.

3. LOCATION-DEPENDING SPATIAL CORRELATION MODELING

Existing approaches to handle spatial correlation for fast statistical analysis by grids or by PCA-based reduction only work well for strong spatial correlation. In this paper, we introduce a new location-dependent spatial correlation model, which was proposed recently for fast statistical timing analysis [4] to improve the computational efficiency for modeling for weak spatial correlation.

The new modeling is based on the observation that the leakage current of a gate in the presence of weak spatial correlation only correlates to a few neighboring gates. If we can introduce a new set of uncorrelated variables which can catch the localized correlation, computing the leakage current of one gate can be done in a constant time by only considering its neighboring gates. Hence total full-chip statistical leakage currents can then be computed by simply adding all the gate leakage currents together in terms of the new set of variables in linear time. The idea is similar to the PCA-based approach [14] but with different set of new independent variables.

Specifically, the chip area is still divided into a set of grid cells. But in our case, the grid can be very small and every grid can even contain one gate. Then, we introduce a "virtual" random variable for each grid. These virtual random variables are *independent* and will be the basis for statistical leakage current calculation that concern spatial correlation. Then we can express the original physical random variable of a gate in a cell as a linear combination of the virtual random variables of its own cell as well as its nearby neighbors. Since each virtual random variable is defined for each cell, which has specific location in a chip, such location-dependent correlation model still retains the important spatial physical meaning (compared to PCA-based models). We notice that there are many ways to generate the grids such as rectangular grids [3] or hexagonal grids [4]. Hexagonal grids are preferred typically as they have minimum anisotropy for 2-D space. But since we will compare our approach with the approach in [3], we still use rectangular grids in this paper.

Here we define "spatial correlation distance" d_{max} as the minimum distance beyond which the spatial correlation between any two grid cells is sufficiently small (or smaller than a given threshold value) so that we can ignore it. For a fixed chip area, if the spatial correlation distance is relatively small, the correlation matrix will be sparse. The grid model are shown in Fig. 1. In this location-dependent model, grid i is associated with one virtual random variable $\xi_i \sim N(0,1)$, which is independent of all other spatial random variables. $\Delta L_{intra,i}$ can then be expressed as its k closest neighboring grid cells. We introduce the concept of *correlation index neighbor* set $T(i)$ for grid i, which defines a set of the indices of ξ_i to model the spatial correlation of $\Delta L_{intra,i}$ as

$$\Delta L_{intra,i} = \sum_{q \in T(i)} \gamma_q \cdot \xi_q. \quad (6)$$

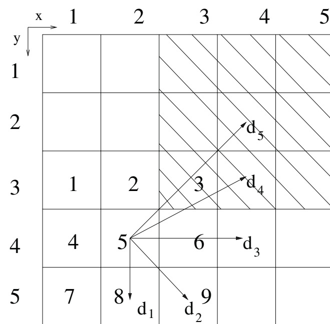

Figure 1: Location-dependent modeling of the spatial correlations with the correlation index defined for each cell as its nine neighboring cells.

For example, if $T(i)$ for each grid cell is defined as its closest $k = 9$ neighboring grid cells, then ΔL located at grid (x_i, y_i) can be represented as a linear combination of nine spatial random variables. The location in $T(i)$ will be

$$T(i) = \{x \in x_i - 1, x_i, x_i + 1; y \in y_i - 1, y_i, y_i + 1\}. \quad (7)$$

Take $\Delta L_{intra,5}$ in Fig. 1 for instance, we have $\Delta L_{intra,5} = \gamma_1\xi_1 + \gamma_2\xi_2 + \ldots + \gamma_9\xi_9$.

This concept of correlation index helps to model the spatial correlation. Two grids close to each other will share more common spatial random variables, which means the correlation is strong. On the other hand, two grids physically far away from each other will share less or no common spatial random variables. In this way, the spatial correlation is modeled as a *homogeneous and isotropic random field* so that the spatial correlation is only related to distance. That is to say, spatial correlation can be fully described by $\rho(d)$ in (3). d_{max} is the distance beyond which $\rho(d)$ becomes small enough to be approximated as zero.

Since $\rho(d)$ is only a function of distance, the number of unique distance values between two correlated grids equals the number of unique element values in $\Omega_{n,n}$. Take the $T(i)$ set in (7) for example. For simplicity of presentation, the length of one grid in Fig 1 is set to be $d_c = 1$. In this case, the spatial correlation distance $d_{max} = 3d_c = 3$ as shown in Fig. 1, and there are only five unique correlation distances d_1 to d_5. Correspondingly, there are only five unique correlation coefficients in $\Omega_{n,n}$, without including 0 for $d \geq d_{max}$ or 1 for distance within one grid.

Furthermore, the same correlation index can be used for all grids and the coefficient γ_k should be the same for the same distance because of the homogeneousness and isotropy of spatial correlation. For the grid marked 5 in Fig. 1, we only have three unique values among the nine coefficients, i.e., we set $p_0 = \gamma_5$, $p_1 = \gamma_2 = \gamma_4 = \gamma_6 = \gamma_8$ and $p_2 = \gamma_1 = \gamma_3 = \gamma_7 = \gamma_9$. In other words, we have $\Delta L_{intra,5} = p_0\xi_5 + p_1(\xi_2+\xi_4+\xi_6+\xi_8) + p_2(\xi_1+\xi_3+\xi_7+\xi_9)$. According to (3), a nonlinear over-determined system can be built to determine the three unique values of p_0, p_1 and p_2 as follows,

$$\begin{aligned}
p_0^2 + 4p_1^2 + 4p_2^2 &= \rho(0) = 1 \\
2p_0p_1 + 4p_1p_2 &= \rho(d_1) = e^{-1/\eta^2} \\
2p_1^2 + 2p_0p_2 &= \rho(d_2) = e^{-2/\eta^2} \\
p_1^2 + 2p_2^2 &= \rho(d_3) = e^{-4/\eta^2} \\
2p_1p_2 &= \rho(d_4) = e^{-5/\eta^2} \\
p_2^2 &= \rho(d_5) = e^{-8/\eta^2}
\end{aligned} \quad (8)$$

This system can be solved by formulating it as a non-linear least square problem. In matrix form, we can rewrite (6) for whole chip as

$$\Delta L_{intra} = P_{N,N} \cdot \vec{\xi}, \quad (9)$$

where N is the number of grid cells, and $\vec{\xi} = [\xi_1, \xi_2, \ldots, \xi_N]$. According to (6), the correlation index set contains only k neighboring spatial random variables, which is a very small fraction of the total spatial random variables. As a result, $P_{N,N}$ is a sparse matrix. Every gate only relates to k virtual random variables, which has specific location information.

Fundamentally, PCA-based method performs a similar process and has a similar new transformation matrix between the original and new set of variables:

$$\Delta L_{intra} = V_{n,n} \cdot \vec{\xi}, \tag{10}$$

where $V_{n,n}$ is the transformation matrix obtained from eigenvalue decomposition of the correlation matrix in PCA. The major difference is that $V_{n,n}$ is a dense matrix even though the original correlation matrix is sparse. This makes a huge difference specially when the spatial correlation is weak as eigen-decomposition will take almost $O(n^3)$ to compute.

We remark that the new independent spatial correlation model also works for medium and strong correlation cases. In case of medium or strong correlation, one can increase the grid cell sizes (reducing number of grids) with high accuracy due to larger correlation length, as demonstrated in the existing grid based method [3]. In this way, a gate will still *see* a few larger neighboring virtual grid cells and linear time complexity can still be attained.

4. THE PROPOSED LEAKAGE POWER ANALYSIS METHOD

In this section, we present the new full-chip statistical leakage analysis method. We first present the overall flow of the proposed method in Fig. 2 and highlight the major computing steps.

Algorithm: NEW FULL-CHIP SLA ALGORITHM.

Input: standard cell lib, netlist, placement information of design, standard deviation of L and T_{ox}.
Output: analytical expression of the full-chip leakage currents in terms of Hermite polynomials.

1. Generate a_{sub} and a_{gate} of I_{sub} and I_{gate} in (4) and (5) for each type of gates (Section 2.2).
2. Solve (8) to determine coefficients in (6).
3. Calculate the coefficients of Hermite polynomials of I_{sub} and I_{gate} for the leakage analytical expression for each gate using (16) and (17).
4. Calculate the analytical expression of the full-chip leakage current by simple polynomial additions and calculate mean value, standard deviation, PDF and CDF of the leakage current if required.

Figure 2: The flow of proposed algorithm.

The new algorithm consists of three major parts. The first part (Step1 and 2) is pre-characterization. Step 1 builds the analytical leakage expressions (4) and (5) for each type of gates, which only needs to be done once for a standard cell library. Step 2 deals with a tiny-size non-linear overdetermined system, which can be solved with any least-square algorithm. The second part (Step 3) generates a small set of independent virtual grid random variables and builds the analytical leakage current expressions and covariances for each gate in terms of the new random variables. The third part (Step 4) computes the final full-chip leakage expressions by simple polynomial additions. From the expression, we can calculate other statistical information (like mean, variance, and even the whole distributions). In the following, we briefly explain some important steps.

4.1 Computing gate leakage by the orthogonal polynomial method

A random variable $x(\vec{\xi})$ with limited variance can be approximated by truncated Hermite Polynomial Chaos expansion as follows [6]:

$$x(\vec{\xi}) = \sum_{q=0}^{P} a_q H_q^z(\vec{\xi}), \tag{11}$$

where $\vec{\xi} = [\xi_1, \xi_2, ..., \xi_z]$ is a vector of independent orthonormal Gaussian random variables with zero mean values, $H_q^z(\vec{\xi})$ is the zth order Hermite polynomial and a_q is the deterministic coefficient. a_q can be determined by (the superscript z is dropped for simple notation)

$$a_q = \frac{< x(\vec{\xi}), H_q(\vec{\xi}) >}{< H_q^2(\vec{\xi}) >} \approx \sum_{i=0}^{P} x(\xi_i) H_i(\xi_i) w_i, \tag{12}$$

where ξ_i and w_i are Gaussian Hermite quadrature abscissas (quadrature points) and weights, respectively. The kernel of this technique is calculating the coefficients of Hermite polynomials efficiently. For multiple random variables, which require multi-dimensional quadrature, Smolyak quadrature [10] is used as an efficient method to reduce the number of quadrature points. For z-dimensional integration, the size of Level-P Smolyak quadrature point set is $O(z^P/(P)!)$.

In our problem, $x(\vec{\xi})$ will be the leakage current for each gate, and eventually for the full chip. For the jth gate, from (6), $\Delta L_{intra,j}$ only relates to k independent virtual random variables in $T(j)$, and from (1) and (2), the corresponding variable vector, $\vec{\xi}_{g,j}$, is defined as

$$\vec{\xi}_{g,j} = [\xi_q, q \in T(j), \;\; \xi_{ox,j}, \xi_{L,inter}, \xi_{ox,inter}], \tag{13}$$

which only includes $z = k + 3$ independent variables. Since $k+3$ is a small number, Step 3 in Fig. 2 can be very efficient.

To compute the gate leakage current, we need to present both I_{sub} and I_{gate} of each gate in second order Hermite polynomials, respectively:

$$I_{sub}(\vec{\xi}_{g,j}) = \sum_{i=0}^{P} I_{sub,i,j} H_i^2(\vec{\xi}_{g,j}), \tag{14}$$

$$I_{gate}(\vec{\xi}_{g,j}) = \sum_{i=0}^{P} I_{gate,i,j} H_i^2(\vec{\xi}_{g,j}), \tag{15}$$

where $H_i^2(\vec{\xi}_{g,j})$ is second order Hermite polynomials. $I_{sub,i,j}$ and $I_{gate,i,j}$ are then computed by the numerical Smolyak quadrature method. Let S be the size of the z-dimensional second order (level-2) quadrature point set Θ_z^2. We have $S \sim O(k^2)$. $I_{sub,i,j}$ and $I_{gate,i,j}$ can be computed as the following:

$$I_{sub,i,j} = \sum_{l=1}^{S} I_{sub}(\vec{\gamma_l}) H_i^2(\vec{\gamma_l}) w_l / < H_i^2(\vec{\xi}_{g,j}) >, \tag{16}$$

$$I_{gate,i,j} = \sum_{l=1}^{S} I_{gate}(\vec{\gamma_l}) H_i^2(\vec{\gamma_l}) w_l / < H_i^2(\vec{\xi}_{g,j}) >, \tag{17}$$

where $\vec{\gamma_l}$ is Smolyak quadrature sample, $I_{sub}(\vec{\gamma_l})$ and $I_{gate}(\vec{\gamma_l})$ are computed using (4) and (5).

As a result, their coefficients for the ith Hermite polynomial at the jth gate can be added directly as

$$I_{leakage,i,j} = \sum I_{sub,i,j} + \sum I_{gate,i,j}. \quad (18)$$

Notice that the time complexity of leakage for a gate is $O(k^2)$. And the number of involved independent random variables k is very small (compared to the total number of gates), which is the case here.

4.2 Computation of full-chip leakage currents

After the leakage currents are calculated for each gate, we can proceed to compute the leakage current for the whole chip as follows:

$$I_{leakage}(\vec{\xi}) = \sum_{j=1}^{n} (I_{sub}(\vec{\xi}_{g,j}) + I_{gate}(\vec{\xi}_{g,j})). \quad (19)$$

The summation is done for each coefficient of Hermite polynomials. Then we obtain the analytic expression of the final leakage currents in terms of $\vec{\xi}$.

We can then obtain the mean value, variance, PDF and CDF of the leakage current easily. For instance, the mean value and variance for the full-chip leakage current are

$$\mu_{leakage} = I_{leakage,0th}, \quad (20)$$

$$\sigma^2_{leakage} = \sum I^2_{leakage,1st} + 2\sum I^2_{leakage,2nd,type1} + \sum I^2_{leakage,2nd,type2}, \quad (21)$$

where $I_{leakage,ith}$ is the leakage coefficient for ith Hermite polynomial of second order defined as follows,

$$H_{0th} = 1, \quad H_{1st} = \xi_i,$$
$$H_{2nd,type1} = \xi_i^2 - 1, \quad H_{2nd,type2} = \xi_i \xi_j, \quad (i \neq j). \quad (22)$$

5. EXPERIMENTAL RESULTS

The proposed method has been implemented in Matlab 7.8.0. Since the leakage model for the method in [18] has to be purely log-normal (linear terms in exponent parts), we did not choose it for comparison purpose. All the experimental results are carried out in a Linux system with quad Intel Xeon CPUs with 2.99Ghz and 16GB memory.

The methods for full-chip SLA were tested on circuits in the PDWorkshop91 benchmark set. The circuits were synthesized with Nangate Open Cell Library and the placement is from MCNC [1]. The technology parameters come from the 45nm FreePDK Base Kit and PTM models [12]. According to [2], L and T_{ox} for high performance logic in 45nm technology will be 18nm and 1.8nm, respectively. And the physical variation should be controlled within +/-12%. So the 3σ values of variations for L and T_{ox} were set to 12% of the nominal values, of which inter-die variations constitute 20% and intra-die variations, 80%. L is modeled as spatially correlated sources of variations, and T_{ox} is modeled as an independent source of variation. The same framework can be easily extended to include other parameters of variations. Both L and T_{ox} are modeled as Gaussian parameters. For the correlated L, the spatial correlation was modeled based on (3). The test cases are given in Table 1 (all length units in μm).

Table 1: Summary of Test cases used in this paper.

Circuit	*Gate #*	*Area*	*Testcase*	d_{max}	d_c	*Grid #*
SC0	125	1459×1350	Case 1	2190	730	2×2
			Case 2	1095	365	4×4
SC1	1888	4892×4874	Case 3	1896	612	8×8
			Case 4	918	328	16×16
SC2	6417	10092×10466	Case 5	984	328	32×31
			Case 6	482	164	64×64

For comparison purposes, we perform Monte Carlo (MC) simulations with 50,000 runs, and compare results from the method in [3] and our proposed approach. Fig. 3 shows the full-chip leakage current distribution (PDF and CDF) of Case 2. It shows that our method fits very well with the MC results, and has almost the same accuracy with [3]. The results of the comparison of mean value and standard deviations of full-chip leakage current are shown in Table 2, where *New* is the proposed method. The average errors for mean and standard variance (σ) values of the new technique are 4.52% and 3.92%, respectively. While for the method in [3], the average errors for mean value and σ are 4.12% and 3.83%, respectively. From Table 2, it is shown that these two algorithms have almost the same accuracy. The results also show that our method can handle both strong and weak spatial correlations by adjusting grid size.

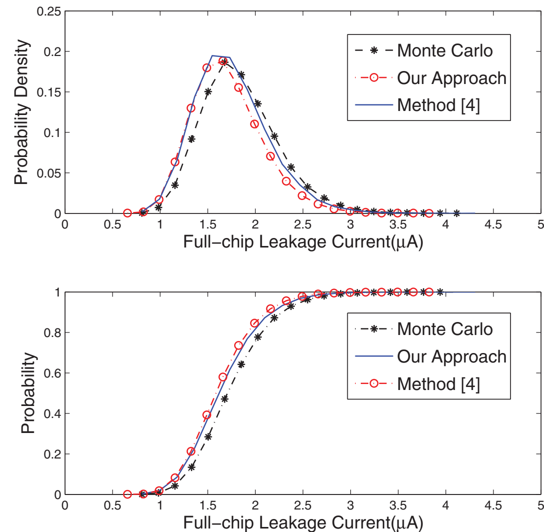

Figure 3: Distribution of full-chip I_{leak} from MC, our approach and method [3] for Case 2.

Table 3 compares the CPU times of the three methods, which shows that the new method, *New*, is much faster than the method in [3] and MC simulation. On average, the proposed technique has about 63X speedup over [3] and many order of magnitudes over the MC method. And the speed of our approach is not affected by the total number of grid cells. If the spatial correlation is strong, which means d_{max} is large, d_c can be increased at the same time without loss of accuracy. So the number of neighboring grids in $T(i)$ will still be much smaller than the number of gates. The new method will be efficient and linear under both cases.

6. CONCLUSION

In this paper, we have presented a linear time method for analyzing the full-chip leakage current distribution of digital circuits in the presence of weak spatial correlation. The

Table 2: SLA accuracy comparison based on Monte Carlo.

Test Case	*Grid #*	*Mean Value (μA)* MC	Method [3]	New	*Errors (%)* Method [3]	New	*Standard Deviation (μA)* *MC*	Method [3]	New	*Errors (%)* Method [3]	New
Case1	2 × 2	1.838	1.751	1.749	-4.76	-4.86	0.4779	0.4628	0.4513	-3.18	-5.56
Case2	4 × 4	1.839	1.751	1.749	-4.79	-4.88	0.3993	0.3679	0.3869	-7.84	-3.10
Case3	8 × 8	29.95	28.88	28.65	-3.57	-4.35	5.674	5.451	5.424	-3.93	-4.44
Case4	16 × 16	29.97	28.88	28.65	-3.63	-4.41	5.390	5.574	5.152	3.41	-4.42
Case5	32 × 32	107.9	103.6	103.2	-3.99	-4.35	20.32	19.86	19.70	-2.26	-3.02
Case6	64 × 64	107.8	103.6	103.2	-3.90	-4.26	20.26	20.74	19.65	2.37	-2.98

Table 3: CPU time comparison.

Test Case	*Computation time(s)* MC	Method [3]	New	*Speedup (%)* Method [3]	New
Case1	83.14	10.39	0.10	8.00	831.4
Case2	87.09	13.16	0.14	6.62	622.1
Case3	828.42	26.24	0.86	31.57	963.3
Case4	869.12	74.50	0.87	11.67	999.0
Case5	7532.77	117.77	8.65	63.96	870.8
Case6	7873.54	490.84	10.67	16.04	737.9

new algorithm exploits the fact that the statistical leakage current of a gate in the presence of weak spatial correlation is affected by a few neighboring gates. As a result, the gate leakage current can be efficiently computed locally in constant time. We adopted a newly proposed spatial correlation model where a new set of location-dependent uncorrelated variables are defined to represent original random variables via fitting. We applied the more general and flexible orthogonal polynomials based collocation method to compute the leakage current of a gate and total leakage power on the new set of variables. The new method can be easily extended for medium and strong correlation while it still maintains the same linear complexity. Experimental results show that the proposed method is about two orders of magnitude faster than the recently proposed grid-based method [3] with similar accuracy and many orders of magnitude over the Monte Carlo method.

7. REFERENCES

[1] "MCNC benchmark circuit placements," http://vlsicad.ucsd.edu/GSRC/bookshelf/Slots/Placement/.

[2] "International technology roadmap for semiconductors (ITRS) 2008 edition," 2008, http://public.itrs.net.

[3] H. Chang and S. S. Sapatnekar, "Full-chip analysis of leakage power under process variations, including spatial correlations," in *Proc. Design Automation Conference (DAC)*, 2005, pp. 523–528.

[4] R. Chen, L. Zhang, V. Zolotov, C. Visweswariah, and J. Xiong, "Static timing: back to our roots," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)*, 2008, pp. 310–315.

[5] V. De and S. Borkar, "Technology and design challenges for low power and high performance," in *Proc. Int. Symp. on Low Power Electronics and Design (ISLPED)*, 1999, pp. 163–168.

[6] R. G. Ghanem and P. D. Spanos, *Stochastic Finite Elements: A Spectral Approach*. Dover Publications, 2003.

[7] K. R. Heloue, N. Azizi, and F. N. Najm, "Modeling and estimation of full-chip leakage current considering within-die correlation," in *Proc. Design Automation Conference (DAC)*, 2007, pp. 93–98.

[8] X. Li, J. Le, and L. T. Pileggi, "Projection-based statistical analysis of full-chip leakage power with non-log-normal distributions," in *Proc. Design Automation Conference (DAC)*, 2006, pp. 103–108.

[9] S. Narendra, V. De, S. Borkar, D. A. Antoniadis, and A. P. Chandrakasan, "Full-chip subthreshold leakage power prediction and reduction techniques for sub-0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, 2004.

[10] E. Novak and K. Ritter, "Simple cubature formulas with high polynomial exactness," *Constructive Approximation*, vol. 15, no. 4, pp. 449–522, Dec 1999.

[11] D. O. Ouma, D. S. Boning, J. E. Chung, W. G. Easter, V. Saxena, S. Misra, and A. Crevasse, "Characterization and modeling of oxide chemical-mechanical polishing using planarization length and pattern density concepts," *IEEE Trans. on Semiconductor Manufacturing*, vol. 15, no. 2, pp. 232–244, May 2002.

[12] "Predictive technology model," http://www.eas.asu.edu/∼ptm/.

[13] R. Rao, A. Srivastava, D. Blaauw, and D. Sylvester, "Statistical analysis of subthreshold leakage current for VLSI circuits," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 2, pp. 131–139, Feb 2004.

[14] R. Shen, N. Mi, S. X.-D. Tan, Y. Cai, and X. Hong, "Statistical modeling and analysis of chip-level leakage power by spectral stochastic method," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)*, 2009, pp. 161–166.

[15] R. Shen, S. X.-D. Tan, N. Mi, and Y. Cai, "Statistical modeling and analysis of chip-level leakage power by spectral stochastic method," *Integration, the VLSI Journal*, vol. 43, no. 1, pp. 156–165, Jan. 2010.

[16] R. Teodorescu, B. Greskamp, J. Nakano, S. R. Sarangi, A. Tiwari, and J. Torrellas, "A model of parameter variation and resulting timing errors for microarchitects," in *Workshop on Architectural Support for Gigascale Integration (ASGI)*, Jun 2007.

[17] J. Xiong, V. Zolotov, and L. He, "Robust extraction of spatial correlation," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 4, 2007.

[18] Z. Ye and Z. Yu, "An efficient algorithm for modeling spatially-correlated process variation in statistical full-chip leakage analysis," in *Proc. Int. Conf. on Computer Aided Design (ICCAD)*, 2009, pp. 295–301.