Symbolic Behavioral Modeling of Low Voltage Amplifiers

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Abstract.- ***We present the generation of symbolic expressions of low voltage amplifiers by using nullors equivalents of the transistors (MOSFETs) which include only the dominant parasitic elements in order to make a simplification before generation. That way, a reduced system of nodal equations is formulated which can be solved easily by determinant decision diagrams. The advantage of the proposed method is that the resulting symbolic behavioral model is reduced to a minimum order and contains just the dominant circuit elements providing a good insight, which is very useful for analog designers.***

1. Introduction

The goal of symbolic analysis is focused on the computation of simplified symbolic expressions which provide a good insight into the behavior of a circuit. The main methods devoted to calculate symbolic expressions can be found in [1]-[2]. The majority of those methods are very useful for symbolic analysis at the circuit level of abstraction, where the analog building blocks are manipulated as a kind of black box, while including the dominant parasitic effects [3].

The symbolic behavioral model of a low voltage amplifier [4], can be generated by applying symbolic analysis at the transistor level of abstraction, where each MOSFET can be modeled by using voltage-controlled current sources (VCCS) or nullors. In the first case, the formulation of the system of equations requires the stamping of every VCCS into the admittance matrix [1]. In the second case, the formulation requires the evaluation of the Cartesian product by applying the nullator and norator properties [5]. We show the application of symbolic analysis for the second case, because the use of the nullor allows us to eliminate many non-dominant parasitic elements, while the main advantage relies on the formulation of a very compacted system of nodal equations.

In section 2, we summarize the formulation by using nullors. In section 3, one stage amplifiers are analyzed. The analyses of the Miller amplifier and of a three stages uncompensated amplifier are shown in section 4. Finally, the conclusions in given in section 5.

2. Formulation by using nullors

The nullor equivalents of several active devices can be found in [1], [3]. For the MOSFET, the nullor equivalent including the parasitic gate-source and gate-drain capacitors, output conductance and trans-conductance, is shown in Fig. 1(a).

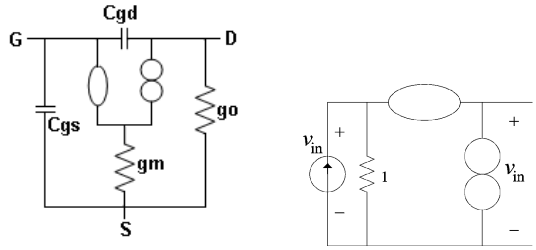

Figure 1. Nullor equivalent of the (a) MOSFET, and (b) independent voltage source.

The nullator and the norator are quite useful to perform symbolic analysis by only applying nodal analysis (NA), as already shown in [5]-[6]. Besides, to apply the symbolic NA method it is required that all circuit elements be modeled by using nullors. In this manner, the independent voltage source, which is a non-compatible NA element, can be transformed to a current source as shown in Fig. 1(b). Since the nullator has the properties that both v=i=0, the current labeled by v_{in} only goes through the 1Ω resistor, then the voltage is the same across the norator, and because each nullator-norator pair reduces the admittance matrix in one order, then the system of equations do not increase at it is done in modified NA (MNA) [1].

The first step in the NA-formulation consists to model all circuit elements (active devices [3], controlled sources and independent voltage sources), by using nullors. In [3] and [6], the modeling processes using nullor equivalents include grounded admittances as much as possible, because they have only one entry in the NA formulation [1], while floating ones may have up to four entries requiring more computational

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work [2]. Henceforth, the NA formulation (***i*** = ***Yv***) is summarized as follows [1], [3], [6]:

Step 1: Describe the interconnection relationships of norators P_j, nullators O_j, and admittances by generating tables including names and nodes (m, n).

Step 2: Calculate indexes associated to set row and column to group grounded and floating admittances:

(a) ROW: Contains all nodes ordered by applying the norator property which nodes (m, n) are virtually short-circuited. These indexes are used to fill vector ***i*** and the admittance matrix ***Y***.

(b) COL: Contains all nodes ordered by applying the nullator property which nodes (m, n) are virtually short-circuited. These indexes are used to fill vector ***v*** and the admittance matrix ***Y***.

(c) Admittances: They are grouped into two tables: Table A includes all nodes (ordered), and in each node is the sum of all admittances connected to it. Table B includes all floating admittances and its nodes (m, n).

Step 3: Use sets ROW and COL to fill vectors ***i*** and ***v***, respectively. To fill ***Y***: if in Table A a node is included in ROW and COL, introduce that admittance(s) in ***Y*** at position (ROW index, COL index). For each admittance in Table B, search node m in ROW and n in COL (do the same but search n in ROW and m in COL), if both nodes exist the admittance is introduced in ***Y*** at position (ROW index, COL index), and it is negative.

The solution of the formulation can be obtained by applying determinant decision diagrams (DDD) [7]-[9]. Elsewhere, the formulation of nullor networks generates a much reduced system of equations than by applying the conventional modified nodal analysis [2]. Another advantage of applying symbolic NA is that the resulting admittance matrix is sparse and it is very suitable for applying sensitivity analysis [10], to obtain knowledge on the variations of the circuit parameters.

3. Symbolic analysis of one stage amplifiers

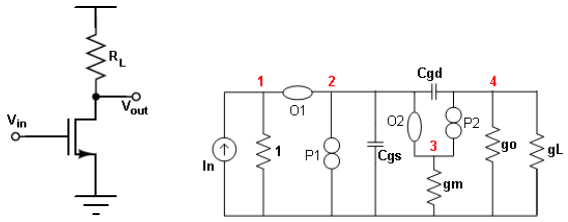
Let's consider the common source amplifier with a resistive load shown in Fig. 2(a). Our goal is to obtain its behavioral model (e.g. the transfer function). The first step consists to obtain the nullor equivalent. This can be done by using Fig. 1, so that the nullor circuit is shown in Fig. 2(b), where the input signal at (In) is the voltage (v_{in}). Now we are able to describe the interconnection relationships of norators P_j, nullators O_j, and admittances.

In the second step, the sets COL and ROW [5]-[6], are: COL ={(1,2,3),(4)}, and ROW={(1),(3,4)}. The indexes of the admittances are given in Table A and B.

According to section 2, the admittance matrix is filled by performing a Cartesian product between COL and ROW sets, leading to the formulation given by (1). The solution for the voltage gain in DC between node 4 (v_{out}) and the input is given by (2). This is a simple symbolic behavioral model indicating that we can manipulate the gain by varying the load resistance or the sizes of the MOSFET to modify its transconductance g_m and output conductance g_o.

$$\begin{bmatrix} v_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ g_m - sC_{gd} & g_L + g_{ds} + sC_{gd} \end{bmatrix} \begin{bmatrix} v_{1,2,3} \\ v_4 \end{bmatrix} \quad (1)$$

$$Av = -\frac{gm}{gL + go} \quad (2)$$



(a) (b)

Figure 2. (a) Common source amplifier with resistive load, and (b) its nullor equivalent.

Table A

Nodes	Admittances
1	1
2	sCgs+sCgd
3	gm
4	sCgd+gL+go

Table B

Floating admittances	Nodes
sCgd	(2,4)

By changing the load resistance in Fig. 1 (R_L), by an active load (using a MOSFET), we obtain the circuit shown in Fig. 3(a). The nullor equivalent is given by Fig. 3(b). The sets COL and ROW are updated to: COL ={(1,2,3),(5)}, and ROW={(1),(3,4,5)}. Besides, the order of the admittance matrix remains 2×2, and the solution for the behavioral model, i.e. the voltage transfer function [11], is given by (3). Now, the DC gain is given by (4). It can be noted that compared to Fig. 1, g_L in (2) was replaced by $g_{m2}+g_{02}$.

$$A_V = -\frac{gm1 - s\,Cgd1}{(Cgd1 + Cgs2)\,s + gm2 + go2 + go1} \quad (3)$$

$$A_{Vdc} = -\frac{gm1}{gm2 + go2 + go1} \quad (4)$$

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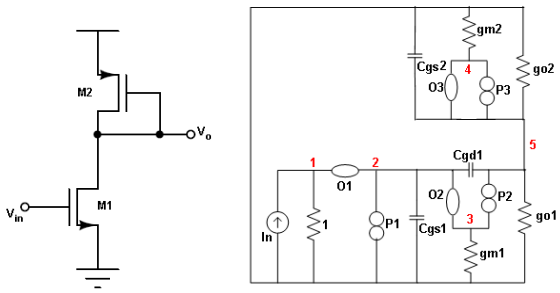
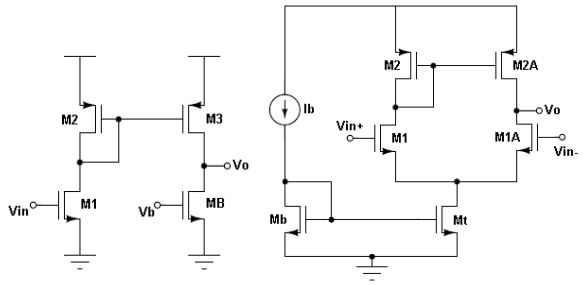


(a) (b)

Figure 3. (a) Common source amplifier with active load, and (b) its nullor equivalent.

Other one stage amplifiers are the non-inverting shown in Fig. 4(a), and the differential pair shown in Fig. 4(b). Their nullor equivalents are shown in Figs. 5 and 6, respectively. From these circuits we can eliminate the output conductance of the MOSFETs not connected at the output port. In this manner, In Figs. 5 and 6, the output conductance is included only at the node (Vo), because in this node the contribution is more relevant, as it is demonstrated in the following section when performing comparisons with HSPICE simulations.

For instance, for the non-inverting amplifier, to formulate the admittance matrix, the sets are: COL={(1),(3,4,5),(6,7,8)}, and ROW={(1,2,3),(4,5,6),(7)}. The formulation is 3×3, as shown by (5). An important thing is that for voltage mode amplifiers (when the input is voltage), the solution to the admittance matrix can be reduced in one order for each input independent-voltage-source, because its nullor equivalent (shown in Fig. 1(b)) generates a unity entry in one row while the rest of the entries are zero, as shown in first row in (1) and (5). Therefore, the application of determinant decision diagrams (DDDs) [7]-[9], becomes reduced. From (5), the symbolic behavioral model, i.e. the DC gain of the non-inverting amplifier is given by (6) [4].



(a) (b)

Figure 4. (a) Noninverting, and (b) differential amplifier.

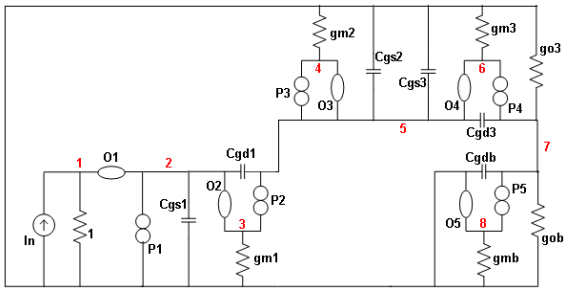


Figure 5. Nullor equivalent from Fig. 4(a).

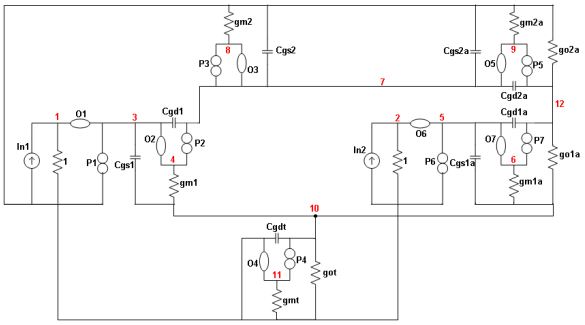


Figure 6. Nullor equivalent from Fig. 4(b).

For the differential stage shown in Fig. 6, the sets are: ROW ={(1),(2),(4,7,8),(6,9,12), (10,11)}, and COL = {(1,3,4),(2,5,6),(7,8,9),(10), (12)}. One can note again that the output conductances of the MOSFETs which are non-connected at the output port are not included. The formulation is 5×5, as shown by (7). However, the solution by applying DDDs can be reduced to solve a 3×3 sub-matrix, because we have two independent-voltage-sources which generate a unity entry in the first and second rows in (7). Again, the advantage of using nullors to generate the symbolic behavioral model is highlighted. The solution of (7), and after applying the simplification procedures provided in [12], the exact DC gain is given by (8). This expression can be simplified, depending on the requirements of the design.

$$\begin{bmatrix} Vin \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ gm1 - s\cdot Cgd1 & gm2 + s\cdot Cgd1 + s\cdot Cgs2 + s\cdot Cgs3 + s\cdot Cgo3 & -s\cdot Cgd3 \\ 0 & gm3 - s\cdot Cgd3 & s\cdot Cgd3 + s\cdot Cgdb + gds3 + gdsb \end{bmatrix} \begin{bmatrix} V_{1,2,3} \\ V_{4,5,6} \\ V_7 \end{bmatrix} \quad (5)$$

$$Av = \frac{gm3\ gm1}{gm2\ gds3\ +\ gm2\ gdsb} \quad (6)$$

$$\begin{bmatrix} Vin \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ gm1 - s\cdot Cgd1 & 0 & s\cdot Cgd1 + s\cdot Cgs2 + s\cdot Cgs2a + s\cdot Cgd2a + gm2 & -gm1 & 0 \\ 0 & gm1a - s\cdot Cgd1a & gm2a - s\cdot Cgd2a & -gm1a - go1a & go1a + go2a + s\cdot Cgd1a + s\cdot Cgd2a \\ -gm1 & -sCgs1a - gm1a & 0 & gm1 + go1a + gm1a + got + sCgs1 + sCgs1a + sCgdt & -go1 \end{bmatrix} \begin{bmatrix} V_{1,3,4} \\ V_{2,5,6} \\ V_{7,8,9} \\ V_{10} \\ V_{12} \end{bmatrix} \quad (7)$$

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$$Av := (gm1\ gm2a\ gm1a + go1a\ gm1\ gm2 + gm1\ gm2a\ got + gm1a\ gm1\ gm2 + go1a\ gm1\ gm2a)/(got\ go1a\ gm2 + gm1a\ go2a\ gm2 + go1a\ gm1\ gm2a + go1a\ go2a\ gm2 + go1a\ gm1\ gm2 + gm1\ go2a\ gm2 + got\ go2a\ gm2) \quad (8)$$

4. The Miller and 3 stages amplifiers

The Miller amplifier is very known in integrated circuit design, its topology is shown in Fig. 7, and the nullor equivalent is shown in Fig. 8.

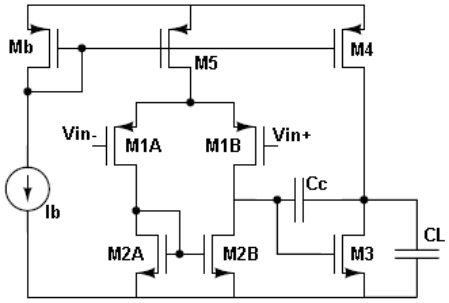

Figure 7. Miller amplifier.

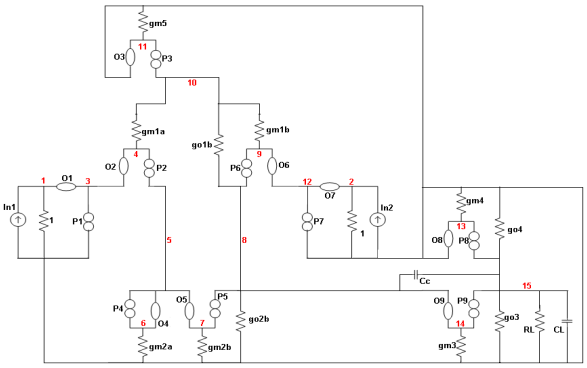

Figure 8. Nullor equivalent of the Miller amplifier in Fig. 7.

In Fig. 8, it can be seen that all parasitic capacitors were taken away, because the contribution provided for the compensation and load capacitor is greater than what was given for parasitic capacitors [4]. Also many output conductances were taken away, considering just those contributing at the output stages, which are given by nodes 8 and 15. In fact, from the inputs to node 8 we can identify the differential amplifier, and between nodes 8 and 15 we can identify a common source stage with an active load and a compensation capacitor. The formulation is given by (9). It is a 6×6 admittance matrix. However, the solution by applying DDDs can be reduced to solve a 4×4 sub-matrix, because again we have two independent-voltage-sources which generate a unity entry in the first and second rows in (9). The advantage of using nullors remains highlighted to generate compact system of equations compared to the modified nodal analysis. For the Miller amplifier, the symbolic behavioral model after applying the simplification procedures provided in [12], it is given by (10). As one sees, the order of the behavioral model is two, i.e. it is very compact. To demonstrate the validity of this symbolic behavioral equation, in Fig. 9 we show the comparison between the responses obtained by our proposed symbolic formulation method and HSPICE.

$$\begin{bmatrix} Vin1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ gm1a & 0 & go1a + gm2a & 0 & -gm1a & 0 \\ 0 & gm1a & gm2a & go1a + go2a + s\,Cc & -go1a - gm1a & -s\,Cc \\ -gm1a & -gm1a & 0 & -go1a & go1a + 2\,gm1a & 0 \\ 0 & 0 & 0 & gm3 - s\,Cc & 0 & go3 + go4 + s\,Cc + s\,CL + gL \end{bmatrix} \begin{bmatrix} V_{1,3,4} \\ V_{2,9,12} \\ V_{5,6,7} \\ V_{8,14} \\ V_{10} \\ V_{15} \end{bmatrix} \quad (9)$$

$$A_V = \frac{gm1a\cdot(Cc\,s - gm3)}{Cc\,CL\,s^2 + (gm3\,Cc + (go1a + go2a)\,CL)\,s + (go3 + go4)\,(go2a + go1a)} \quad (10)$$

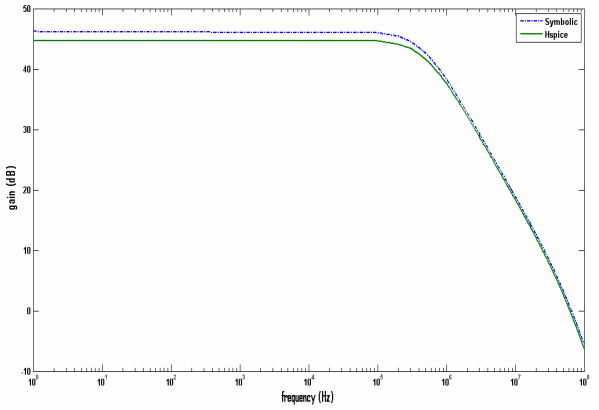

Figure 9. Responses of evaluating (10) and HSPICE.

Our last example is the three stages uncompensated amplifier shown in Fig. 10. Its nullor equivalent is shown in Fig. 11. Again, we included the output conductances only of those MOSFETs connected at the outputs of every stage (the circuit can be seen as a three stages amplifier [4]). In this manner, the dominant output conductances are go2, go4, go5, go6, go7, go8 and go9. All parasitic capacitors were taken away, because the contribution to poles is mainly given by the capacitors C_{p1}, C_{p2} and C_L. The formulation is 7×7, and since we have only one independent-voltage source (as the input signal), the solution can be performed by solving a sub-matrix of order 6×6 because it generates a unity entry in one row. As a result, the simplified symbolic behavioral model is given by (11). It has an order three, however, we can apply model order reduction techniques [1] in order to obtain the poles of the model.

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$$A_V = -\frac{gm8\ gm6\ gm1}{Cp1\ Cp2\ CL\ s^3 + Cp1\ Cp2\ gm8\ s^2 + (Cp1\ go6 + Cp1\ go7 + go4\ Cp2 + go2\ Cp2)\ gm8\ s + (go2\ go7 + go4\ go7 + go2\ go6 + go4\ go6)\ gm8} \quad (11)$$

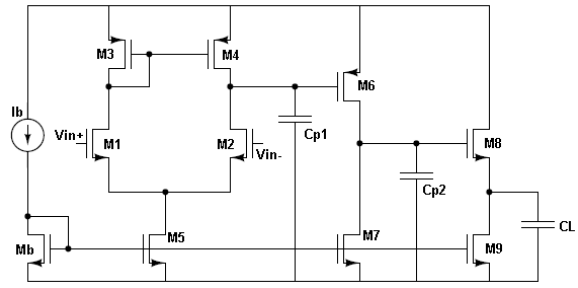

Figure 10. Three stages uncompensated amplifier.

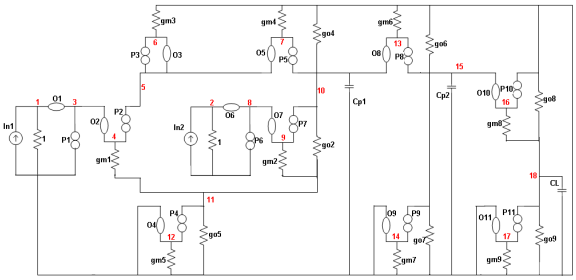

Figure 11. Nullor equivalent of Fig. 10.

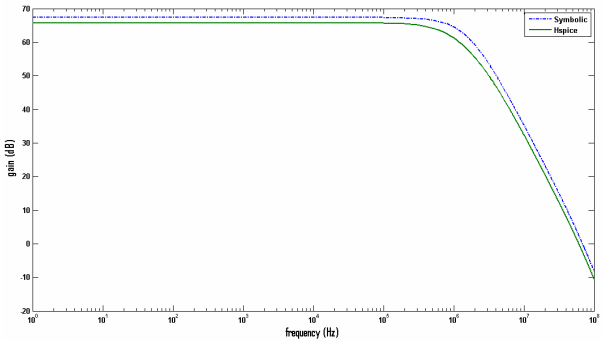

Figure 12. Responses of evaluating (11) and HSPICE.

5. Conclusion

It was shown the usefulness of using nullor equivalents to calculate simplified symbolic behavioral models of low voltage amplifiers. The proposed approach can be implemented within an environment of design automation for analog integrated circuits in order to get an insight on the dominant circuit elements. As it can be appreciated, the order of the admittance matrices is low, so that one is able to compute other symbolic expressions and sensitivities in low computational cost. It is worthy to mention that the reduced formulation depends on the inclusion of those dominant parasitic elements, which is a future work.

The suitability of the proposed symbolic method was demonstrated by comparing the generated symbolic expressions with HSPICE simulations, were it can be appreciated a low error due to the elimination of non-dominant parasitic.

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