

# Fast Electromigration Stress Analysis Considering Spatial Joule Heating Effects

Mohammadmir Kavousi, Liang Chen and Sheldon X.-D. Tan

Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521 USA  
mkavo003@ucr.edu, lianchen@ucr.edu, stan@ece.ucr.edu

**Abstract**— Temperature gradient due to Joule heating has huge impacts on the electromigration (EM) induced failure effects. However, Joule heating and related thermomigration (TM) effects were less investigated in the past for physics-based EM analysis for VLSI chip design. In this work, we propose a new spatial temperature aware transient EM induced stress analysis method. The new method consists of two new contributions: First, we propose a new TM-aware void saturation volume estimation method for fast immortality check in the post-voiding phase for the first time. We derive the analytic formula to estimate the void saturation in the presence of spatial temperature gradients due to Joule heating. Second, we develop a fast numerical solution for EM-induced stress analysis for multi-segment interconnect trees considering TM effect. The new method first transforms the coupled EM-TM partial differential equations into linear time-invariant ordinary differential equations (ODEs). Then extended Krylov subspace-based reduction technique is employed to reduce the size of the original system matrices so that they can be efficiently simulated in the time domain. The proposed method can perform the simulation process for both void nucleation and void growth phases under time-varying input currents and position-dependent temperatures. The numerical results show that, compared to the recently proposed semi-analytic EM-TM method, the proposed method can lead to about 28x speedup on average for the interconnect with up to 1000 branches for both void nucleation and growth phases with negligible errors.

## I. INTRODUCTION

Electromigration (EM) is the top reliability killer for copper-based interconnects of current integrated circuits (ICs) in 7 nm technology and below. The EM crisis becomes even worse as technology advances. It is critical to develop more accurate EM models and less conservative EM sign-off and assessment techniques for more EM-aware design and run-time management. Therefore, it is important to accurately predict aging and failure effects in interconnect trees for fast sign-off analysis for today's chip design. Recently, a number of physics-based EM models and assessment techniques have been proposed for finding transient hydrostatic stress [1]–[8].

The crux of those EM modeling problems primarily focuses on solving the partial differential equation (PDE) (called Korhonen's equation) of hydrostatic stress evolution in the confined multi-segment wires subject to blocking material boundary or zero-stress conditions. However, most of those methods did not consider the spatial temperature gradients due to Joule heating. Recent studies [7], [9] show that the thermomigration (TM) (due to Joule heating) effects can be quite significant (almost in the same magnitude as electromigration) due to the Joule heating effects. This situation will become even worse as technology advances to smaller features and 3D stacked integration, in which higher power density, more Joule heating, and larger thermal resistances due to stacking will lead to even higher temperature and temperature gradients across chip [10].

In this work, we try to address this issue to explicitly consider the impacts of thermomigration (spatial thermal gradient) effect. Our key contributions are as follows:

- First, we propose a new TM-aware void saturation volume estimation method for fast immortality check in the post-void phase for the first time. We derive the analytic formula to estimate the void saturation in the presence of spatial temperature gradients due to Joule heating.
- Second, we develop a fast numerical solution for EM-induced stress analysis for multi-segment interconnect trees considering TM effect. The new method first transform the coupled EM-TM partial differential equations into linear time-invariant ordinary differential equations (ODEs). Then extended Krylov subspace-based reduction technique is employed to reduce the size of the original system matrices so that they can be efficiently simulated in the time domain.
- Third, our numerical results show that compared to a recently proposed semi-analytic TM-EM analysis method, the proposed TM-EM method achieves about 28x speedup on average for the interconnect with up to 1000 branches, which cover the majority of typically power grid networks.

## II. REVIEW OF RELATED WORK

Metal under high current density induces an inhomogeneous temperature distribution that leads to temperature gradients. These temperature gradients result in metal atoms' migration. This effect is called Thermomigration (TM). We remark that in this work, the spatial temperature impacts on metal migration are simply referred as thermomigration or TM.

Studies show that the large temperature gradients  $|dT/dx|$  can cause significant TM, which can be in the same magnitude as EM [7], [11], [12]. In addition, experimental data shows that thermal gradient has remarkable impacts on the EM-induced time to failure (TTF) for power electronics due to temperature gradients effects  $|dT/dx|$  [13]. This article also highlights that the temperature gradient of  $0.19K/\mu m$  leads to 50% TTF reduction. As a result, the temperature gradient effects can be quite significant due to the Joule heating effects. However, many existing EM methods do not consider thermal effect [14]–[19] or only consider the transient thermal effects when solving the Korhonen's equation or derive analytic models to estimate transient EM stress under time-varying temperature [3]–[5], [20], [21]. Those works fail to consider the spatial temperature or TM impacts on the multisegments. Cook *et al.* proposed a fast solution to find transient hydrostatic stress [22]. However, it also did not consider the gradient temperature impacts caused by the Joule heating. Recently, some researchers investigated TM impacts on EM stress analysis and showed that TM indeed can have the same impacts on the EM and the TM effect will become more significant as technology scale [9], [23].

## III. PROPOSED NEW SATURATION-VOLUME ESTIMATION CONSIDERING TM EFFECTS

This section presents how to compute the void saturation volume for multi-segment interconnects considering TM effects and the resulting EM immortality check formula. To

This work is supported in part by NSF grants under No. CCF-1816361, in part by NSF grant under No. CCF-2007135 and No. OISE-1854276.

estimate the steady-state stress of post-voiding phase, we first illustrate the relationship between nucleation and post-voiding phases. We assume that the void size will be much smaller than the wire length so that the effective width length essentially does not change. This is typically true for most interconnect wires.

Fig. 1 shows the EM stress evolution considering TM effect on a single wire in nucleation phase and post-voiding phase. In nucleation phase, the stress at the cathode node increases over time. We usually check steady-state stress for nucleation phase to see whether the interconnect is an immortal wire. This work is done before the saturation volume estimation.

Therefore, we can get the steady stress  $\sigma_n(x, \infty)$  (blue bold dash line) with zero atom flux at the block terminals, which is the boundary condition of nucleation phase. We also have the atom conservation,

$$\int_0^L \sigma_n(x, \infty) dV = wh \int_0^L \sigma_n(x, \infty) dx = wh \int_0^L \sigma_0 dx \quad (1)$$

Where  $\sigma_0$  is the initial stress,  $w$ ,  $h$  and  $L$  are the width, thickness and length of the wire, respectively.

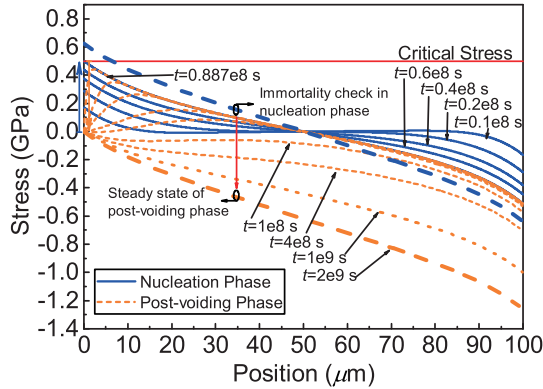


Fig. 1. EM stress evolution considering TM effect in nucleation phase and post-voiding phases.

When the stress reaches the critical value  $\sigma_{crit} (\approx 500 \text{ MPa})$ , the void is formed and starts to grow, which is the post-voiding phase, as shown in Fig. 1. In the meantime, the boundary conditions at the cathode node ( $x = 0 \mu\text{m}$ ) change, which is given by

$$\left. \frac{\partial \sigma}{\partial x} \right|_{x=0} = \frac{\sigma(0, t)}{\delta} \quad (2)$$

where  $\delta$  is the effective thickness of the void interface. Once the void is formed, the stress at ( $x = 0 \mu\text{m}$ ) is released to zero. Fig. 1 shows that all steady-state stress  $\sigma_p(x, \infty)$  (orange bold dash line) values for post-voiding phase on the interconnect becomes negative. As we can see, the only difference between nucleation phase and post-voiding phase is the boundary condition at block node  $x = 0 \mu\text{m}$ .

Specifically, we have the following proposition without proof for the relationship between *pseudo* steady-state stress<sup>1</sup> in the nucleation phase and the steady-state stress in the post-voiding phase:

*Proposition 1: Let's define  $\sigma_n(x, t)$  and  $\sigma_p(x, t)$  as the stresses at location  $x$  at time  $t$  in the nucleation phase and in the post-voiding phases respectively, then we have*

$$\sigma_p(x, \infty) = \sigma_n(x, \infty) - \sigma_n(0, \infty), \quad (3)$$

<sup>1</sup>*pseudo* means void will not form even the critical stress is reached

where  $\sigma_n(0, \infty)$  is the *pseudo* steady-state maximum stress at location  $x = 0$  (the cathode node) for nucleation phase. This can be easily observed from Fig. 1 as the current densities in all the segments of interconnect wires do not change in both nucleation and post-voiding phases. Therefore, the maximum steady stress  $\sigma_n(0, \infty)$  for nucleation phase at  $x = 0 \mu\text{m}$  is the offset of steady-state stress in nucleation phase to steady stress in post-voiding phase.

Next, based on the steady-stress in post-voiding phase, we estimate the void volume. Specifically, based on physics, the void volume  $V_v(t)$  with initial condition  $\sigma_0$  meets the atom conservation equation [24]

$$V_v = - \int_{\Omega_L} \frac{\sigma(x, t)}{B} dV + \int_{\Omega_L} \frac{\sigma_0}{B} dV \quad (4)$$

where  $\sigma(x, t)$  is the stress over time and position,  $B$  is the effective bulk elasticity modulus, and  $\Omega_L$  is the volume of the remaining interconnect wire. This equation (4) works for both nucleation phase and post-voiding phase. In nucleation phase, void size  $V_v$  is always zero since no void is formed. Once it enters post-voiding phase, the void size  $V_v$  starts to increase. After all stresses are released, the void reaches saturation volume, which is the steady-state of post-voiding phase. Based on (4), the steady-state saturation volume  $V_{sat}$  of void is expressed as

$$\begin{aligned} V_{sat} &= -wh \int_0^L \frac{\sigma_p(x, \infty)}{B} dx + wh \int_0^L \frac{\sigma_0}{B} dx \\ &= -wh \int_0^L \frac{\sigma_n(x, \infty) - \sigma_n(0, \infty)}{B} dx + wh \int_0^L \frac{\sigma_0}{B} dx \end{aligned} \quad (5)$$

By substituting (1) into (5), the saturation volume can be calculated by

$$V_{sat} = \frac{whL\sigma_n(0, \infty)}{B} \quad (6)$$

Actually,  $\sigma_n(0, \infty)$  is the steady stress at cathode node with zero atom flux, which is the maximum steady stress in nucleation phase. For the TM-aware immortality check in nucleation phase, the maximum effective EM voltage  $\mathcal{V}_{eff,g}^T$  on the ground node  $g$  is calculated to be compared with the critical stress  $\mathcal{V}_{crit,EM}^T$  [25].  $\mathcal{V}_{eff,g}^T$  is given by

$$\mathcal{V}_{eff,g}^T = \mathcal{V}_E^T - U_g^T \quad (7)$$

where  $\mathcal{V}_E^T$  is EM voltage considering spatial temperature effect,  $U_g^T = U_g - \frac{Q}{eZ} \ln(T_g)$ ,  $T_g$  and  $U_g$  are the temperature and voltage at the node  $g$  with maximum stress.  $Q$  is the specific heat of transport,  $e$  is the electron charge, and  $Z$  is the effective charge number. To estimate the temperature on the interconnects, an analytical solution is given by [7]

$$\begin{aligned} T(x) &= \left( \frac{T_i + T_j}{2} - T_m - T_0 \right) \text{sech}\left(\frac{L}{2\Gamma}\right) \cosh\left(\frac{x}{\Gamma}\right) \\ &\quad + T_n \text{csch}\left(\frac{L}{2\Gamma}\right) \sinh\left(\frac{x}{\Gamma}\right) + T_m + T_0 \end{aligned} \quad (8)$$

where  $T_i$  and  $T_j$  are the temperatures at node  $i$  and  $j$  of the branch  $ij$ .  $\Gamma$  is effective thermal length.  $T_0$  is the ambient temperature.  $T_m$  and  $T_n$  are respectively represented by

$$T_m = \frac{j^2 \rho \Gamma^2}{\kappa_{Cu}}, \quad T_n = \frac{T_i - T_j}{2} \quad (9)$$

where  $\rho$  is the resistivity and  $\kappa_{Cu}$  is the thermal conductivity of the copper. With  $\mathcal{V}_{eff,g}^T = \frac{\Omega}{eZ} \sigma_g$ , we have

$$\sigma_g = \frac{eZ}{\Omega} \mathcal{V}_{eff,g}^T = \frac{eZ}{\Omega} (\mathcal{V}_E^T - U_g^T) \quad (10)$$

Based on (6) and (10), the saturation volume can be calculated by

$$V_{\text{sat}}^T = \frac{whL}{B} \sigma_g = \frac{whL}{B} \frac{eZ}{\Omega} (\mathcal{V}_E^T - U_g^T) \quad (11)$$

where  $\Omega$  is the atomic lattice volume.

To extend one single wire to a general multisegment interconnect, the total void saturation volume is calculated by

$$V_{\text{sat, total}}^T = \sum_{ij} \frac{w_{ij} h_{ij} L_{ij}}{B} \frac{eZ}{\Omega} (\mathcal{V}_E^T - U_g^T) \quad (12)$$

When the void is formed in interior junction node, each segment connected with this node has the void. To estimate the void saturation volume for each segment separately, based on (5), we need to calculate the integral of the stress, which is given by [9], [25]

$$\begin{aligned} \sum_{ij} \int_{x_i}^{x_j} \sigma(x) w_{ij} h_{ij} dx &= \sum_{ij} w_{ij} h_{ij} \left[ \left( \frac{\sigma_i + \sigma_j}{2} \right) L_{ij} \right. \\ &+ \frac{Q}{\Omega} \left( \ln \left( \frac{T_0 + T_{m,ij}}{\sqrt{T_i T_j}} \right) L_{ij} \right. \\ &\left. \left. + \frac{(T_i + T_j - 2(T_0 + T_{m,ij})) \Gamma}{T_0 + T_{m,ij}} \tanh \left( \frac{L_{ij}}{2\Gamma} \right) \right) \right] \end{aligned} \quad (13)$$

Then, the  $k$ th void saturation volume on the segment which has  $N_k$  branches is estimated by

$$\begin{aligned} V_{\text{sat, k}}^T &= -\frac{1}{B} \sum_{ij}^{N_k} w_{ij} h_{ij} \left[ \left( \frac{\sigma_i + \sigma_j}{2} \right) L_{ij} \right. \\ &+ \frac{Q}{\Omega} \left( \ln \left( \frac{T_0 + T_{m,ij}}{\sqrt{T_i T_j}} \right) L_{ij} \right. \\ &+ \left. \left. \frac{(T_i + T_j - 2(T_0 + T_{m,ij})) \Gamma}{T_0 + T_{m,ij}} \tanh \left( \frac{L_{ij}}{2\Gamma} \right) \right) \right] \quad (14) \\ &+ \sum_{ij}^{N_k} \frac{w_{ij} h_{ij} L_{ij}}{B} \frac{eZ}{\Omega} (\mathcal{V}_E^T - U_g^T) \\ &+ \sum_{ij}^{N_k} \int_{x_i}^{x_j} w_{ij} h_{ij} \frac{\sigma_0}{B} dx \end{aligned}$$

The relationship between the total saturation volume and the void volumes for each segment satisfies

$$V_{\text{sat, total}}^T = \sum_{k=1}^{N_v} V_{\text{sat, k}}^T \quad (15)$$

where  $N_v$  is the total number of segments which have the void.

Once  $V_{\text{sat, k}}^T$  is calculated for the  $k$ th void, then the EM immortality check considering void saturation volume can be simply given as

$$V_{\text{sat, k}}^T < V_{\text{sat, crit}}^T \quad (16)$$

where  $V_{\text{sat, crit}}^T$  is the given critical void volume before resistance change can happen for the wire.

#### IV. THE PROPOSED TM-AWARE EM ANALYSIS

In this section, we present the proposed TM-aware transient analysis method.

##### A. Void nucleation phase

The failure process consists of two phases, nucleation and post-voiding phase. In the first phase, void nucleation occurs near the cathode end. For a general interconnect wire, transient hydrostatic stress evolution  $\sigma(x, t)$  along the wire is described by the Korhonen equation [26]

$$PDE : \frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[ \kappa(x) \left( \frac{\partial \sigma}{\partial x} - S - M \right) \right], \quad t > 0 \quad (17)$$

$$BC : \kappa(x_b) \left( \frac{\partial \sigma}{\partial x} \Big|_{x=x_b} - S - M \right) = 0, \quad 0 < t < t_{nuc} \quad (18)$$

$$IC : \sigma(x, 0) = \sigma_T \quad (19)$$

where  $\kappa(x) = D_a(T(x))B\Omega/(k_b T(x))$  is a position-dependent diffusivity due to non-uniform temperature, and  $D_a = D_0 \exp(-E_a/(k_b T(x)))$  is atomic diffusion coefficient.  $D_0$  is a constant and  $E_a$  is the EM activation energy.  $S = \frac{eZ\rho j}{\Omega}$  is EM flux and  $M = \frac{Q}{\Omega T} \frac{\partial T}{\partial x}$  is for TM flux.  $x_b$  represents block terminals and  $\sigma_T$  is the initial thermal-induced residual stress. For TM flux, following the similar work in [25], we first find analytical temperature distribution for a general multi-segment wire.

To solve the (17), we apply the finite difference method (FDM). Specifically, to discretize the equation  $(\kappa(x)\sigma'(x))'$  along spatial variable  $x$ , we can apply the chain rule to rewrite as  $\kappa(x)\sigma''(x) + \kappa'(x)\sigma'(x)$ . However, our study shows such different scheme leads to large errors. Instead, we discretize the second-order term directly:

$$\begin{aligned} (\kappa(x)\sigma'(x))' &= \frac{\kappa(x + \frac{1}{2}\Delta x) \left( \frac{\sigma(x+\Delta x) - \sigma(x)}{\Delta x} \right)}{\Delta x} \\ &\quad - \frac{\kappa(x - \frac{1}{2}\Delta x) \left( \frac{\sigma(x) - \sigma(x-\Delta x)}{\Delta x} \right)}{\Delta x} \end{aligned} \quad (20)$$

As a result, the PDE in (17) can be written into the following finite difference form:

$$\begin{aligned} \frac{\partial \sigma}{\partial t} &= \\ &\frac{\kappa(x + \frac{1}{2}\Delta x) \left( \frac{\sigma(x+\Delta x) - \sigma(x)}{\Delta x} - S(x + \frac{1}{2}\Delta x) - \frac{Q}{\Omega T} \frac{T(x+\Delta x) - T(x)}{\Delta x} \right)}{\Delta x} \\ &\quad - \frac{\kappa(x - \frac{1}{2}\Delta x) \left( \frac{\sigma(x) - \sigma(x-\Delta x)}{\Delta x} - S(x - \frac{1}{2}\Delta x) - \frac{Q}{\Omega T} \frac{T(x) - T(x-\Delta x)}{\Delta x} \right)}{\Delta x} \end{aligned} \quad (21)$$

To illustrate the proposed method, we use a two-segment wire with total length  $L$  as an example shown in Fig. 2, in which  $j_1, j_2$  are current densities of each segment. The wire is discretized into five nodes with two terminal boundary nodes at each end of the wire, one junction node at the middle of the wire, and two non-boundary nodes, each between the junction and a terminal node.

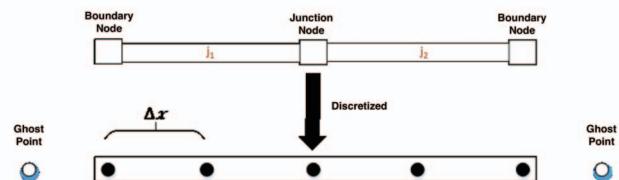


Fig. 2. Discretization of the two-segment wire.



## V. NUMERICAL RESULTS AND DISCUSSION

In this section, we first present the results for the proposed spatial temperature aware void saturation volume estimation method. Then we compare our proposed transient EM-TM analysis method against finite element based COMSOL and a few state of art methods on a number of interconnect trees.

### A. Saturation volume estimation

In this sub-section, we use two examples from power network benchmarks to demonstrate the accuracy of analytical solution of the void saturation volume. The initial stress  $\sigma_0$  is set to 10 MPa.

In the first example, the maximum stress is located at the terminal end of the straight-line multisegment interconnect, as shown in Fig. 3 (a) and (b). The saturation void size of TM-aware immortality check is smaller than that of EM immortality check. Fig. 4(a) shows steady-stress in void nucleation phase and post-voiding phase. Once the void is formed, the maximum stress is released to zero.

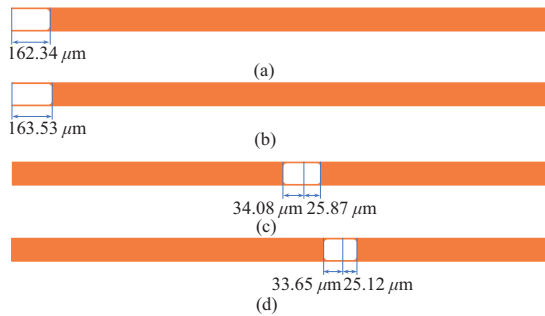


Fig. 3. The length of voids for (a) TM-aware and (b) EM saturation volume estimation for the first example with terminal void. The length of voids for (c) TM-aware and (d) EM saturation volume estimation for the second example with interior void.

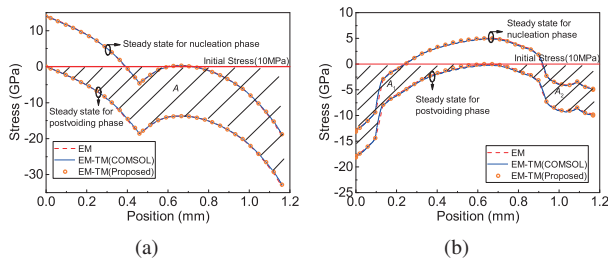


Fig. 4. Steady state stress for TM-aware and EM analysis with (a) terminal void and (b) interior void.

In the second example, the maximum stress is placed at the mid part of the straight-line multisegment interconnect, as shown in Fig. 3 (c) and (d). Both location and size of the voids for TM-aware and EM immortality check are different. Fig. 4(b) shows steady stress in void nucleation phase and post-voiding phase. Once the void is formed, one interconnect is divided into two sub-wires. By calculating areas  $A_1$  and  $A_2$  in Fig. 4(b), we can estimate the saturation volume of two sub-wires separately.

From two examples, considering Joule heating effects is very important for the accurate prediction of EM reliability. To validate the accuracy of the analytical solution, commercial software COMSOL is also employed to calculate the saturation volume. As shown in Table. I, the analytical results agree well with that of COMSOL.

TABLE I  
ACCURACY OF SATURATION VOLUME ESTIMATION

|   | EM( $\mu\text{m}^3$ ) |       | EM-TM( $\mu\text{m}^3$ ) |       |          |       | Rel. Err. (%) |
|---|-----------------------|-------|--------------------------|-------|----------|-------|---------------|
|   |                       |       | COMSOL                   |       | Proposed |       |               |
| 1 | 64.756                |       | 64.291                   |       | 64.286   |       | 0.008         |
| 2 | 3.461                 | 2.584 | 3.507                    | 2.662 | 3.505    | 2.661 | 0.049         |

### B. Straight line interconnect case

Now we consider the straight line example, which typically is used in the on-chip power grid networks. The line can have many vias connecting the standard cells with blocking terminals on both sides. For a real application, a straight line is selected from a realistic IBMPG1 benchmark. Its size and current densities obtained by SPICE circuits simulation for IBMPG1 benchmark. Figs. 5(a) and 5(b) show that there exists a very good agreement between the proposed method and COMSOL results at different time points. We will see that TM effects lead to decreasing of void nucleation time.

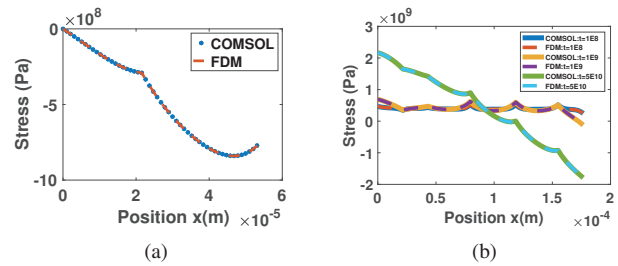


Fig. 5. (a) Growth stage validation for two segments wire at  $t=1E9$ . (b) Nucleation stage validation for nine segments wire.

### C. Results for MOR-accelerated TM-EM analysis

The recently proposed fast EM analysis, FastEM [22], does not consider the temperature gradient impacts on the metal migration process. However, Fig. 6(a) shows that the temperature gradient effects can be quite significant due to the Joule heating effects. This figure compares our reduced analytical solution with FastEM at steady-state stress and shows that our results agree well with COMSOL. To further validate the proposed MOR method, the six-segment case is simulated and compared with the FDM. Each simulation is conducted using five poles for reduction ( $q = 5$ ). In Fig. 6(c), the nucleation stage stress under nonuniform current density distribution for three time steps is shown. The results show agreement between both methods.

Table II shows the performance comparison between our proposed MOR-accelerated TM-EM analysis method and recently proposed TM-aware EM analysis method [9], which is a semi-analytic method by using separation of variables method and a fast numerical method for finding the eigenvalues for the analytical solution. As we can see, the proposed MOR-accelerated method can achieve about 28x speedup on average for all the examples in this table.

In Fig. 6(b) we compare our proposed method with the recently proposed semi-analytic EM-TM analysis method [9] at  $t = 1E13$ . As you can see in that figure, both methods agree well with COMSOL.

## VI. CONCLUSION

In this article, we have proposed a new thermomigration-aware transient EM stress analysis method for multi-segment interconnects. The new method consists of two contributions: First, the new analytic TM-aware void saturation volume

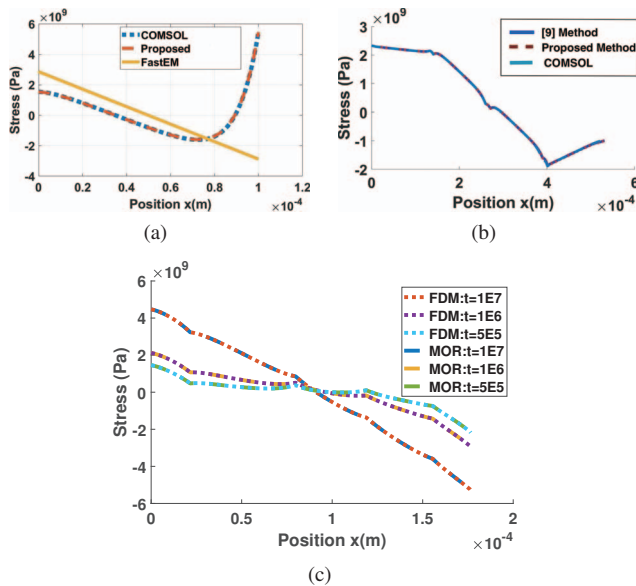


Fig. 6. (a) Steady-state stress comparison between the new method, FastEM [22] and COMSOL. (b) Steady-state stress comparison between the proposed method and the semi-analytical method [9], (c) MOR validation for 6 wire segments with  $q=5$ .

TABLE II  
THE CPU TIME COMPARISON WITH THE SEMI-ANALYTIC METHOD

| #branch | Method in [9] (s) | New TM-EM (s) | Speed-up |
|---------|-------------------|---------------|----------|
| 20      | 6.4451            | 0.0469        | 137.42×  |
| 50      | 16.3721           | 0.4681        | 34.98×   |
| 100     | 35.2561           | 1.3651        | 25.83×   |
| 200     | 83.5570           | 6.7356        | 12.41×   |
| 400     | 224.0334          | 40.5487       | 5.53×    |
| 500     | 324.1820          | 72.3226       | 4.48×    |
| 700     | 604.5640          | 190.4173      | 3.17×    |
| 1000    | 1307.7429         | 572.2694      | 2.29×    |

estimation formula for fast EM immortality check was proposed and second, a fast numerical frequency domain analysis technique for solving the partial differential equations for both nucleation and post-voiding phases were presented. Compared to the recently proposed semi-analytic EM-TM analysis method, the proposed TM-EM method achieves about 28x speedup on average for the interconnect with up to 1000 branches, which cover the majority of typically power grid networks.

## REFERENCES

- [1] Xin Huang, Tan Yu, Valeriy Sukharev, and Sheldon X.-D. Tan. Physics-based Electromigration Assessment for Power Grid Networks. In *Proceedings of the 51st Design Automation Conference, DAC '14*, pages 1–6, New York, NY, Jun. 2014. ACM Press.
- [2] V. Sukharev, X. Huang, H.-B. Chen, and S. X.-D. Tan. IR-drop based electromigration assessment: parametric failure chip-scale analysis. In *Proc. Int. Conf. on Computer Aided Design (ICCAD)*, pages 428–433. IEEE, Nov. 2014.
- [3] V. Mishra and S. S. Sapatnekar. Predicting Electromigration Mortality Under Temperature and Product Lifetime Specifications. In *Proc. Design Automation Conf. (DAC)*, pages 1–6, Jun. 2016.
- [4] X. Huang, V. Sukharev, T. Kim, and S. X.-D. Tan. Electromigration recovery modeling and analysis under time-dependent current and temperature stressing. In *Proc. Asia South Pacific Design Automation Conf. (ASPAC)*, pages 244–249. IEEE, Jan. 2016.
- [5] X. Huang, V. Sukharev, and S. X.-D. Tan. Dynamic electromigration modeling for transient stress evolution and recovery under time-dependent current and temperature stressing. *Integration, the VLSI Journal*, 55:307–315, September 2016.
- [6] S. Chatterjee, V. Sukharev, and F. N. Najm. Power grid electromigration checking using physics-based models. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(7):1317–1330, July 2018.

- [7] Ali Abbasinasab and Malgorzata Marek-Sadowska. RAIN: A tool for reliability assessment of interconnect networks—physics to software. In *Proc. Design Automation Conf. (DAC)*, pages 133:1–133:6, New York, NY, USA, 2018. ACM.
- [8] Sheldon X.-D. Tan, Mehdi Tahoori, Taeyoung Kim, Shengcheng Wang, Zeyu Sun, and Saman Kiamehr. *VLSI Systems Long-Term Reliability – Modeling, Simulation and Optimization*. Springer Publishing, 2019.
- [9] Liang Chen, Sheldon X.-D. Tan, Zeyu Sun, Shaoyi Peng, Min Tang, and Junfa Mao. A fast semi-analytic approach for combined electromigration and thermomigration analysis for general multisegment interconnects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(2):350–363, 2021.
- [10] A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, and A. Virazel. A study of tapered 3-d TSVs for power and thermal integrity. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 21(2):306–319, Feb 2013.
- [11] Guo Weiling, Li Zhiguo, Zhou Tianyi, Cheng Yaohai, Chan Changhua, and Sheng Guangdi. The electromigration and reliability of VLSI metallization under temperature gradient conditions. In *1998 5th International Conference on Solid-State and Integrated Circuit Technology. Proceedings (Cat. No.98EX105)*, pages 226–229, Oct 1998.
- [12] K. N. Tu and A. M. Gusak. A unified model of mean-time-to-failure for electromigration, thermomigration, and stress-migration based on entropy production. *Journal of Applied Physics*, 126(7):075109, 2019.
- [13] H. V. Nguyen, C. Salm, B. Krabbenborg, K. Weide-Zaage, J. Bisschop, A. J. Mouthaan, and F. G. Kuper. Effect of thermal gradients on the electromigration life-time in power electronics. In *2004 IEEE International Reliability Physics Symposium. Proceedings*, pages 619–620, April 2004.
- [14] Xiaoyi Wang, Shaobin Ma, Sheldon X.-D. Tan, Chase Cook, Liang Chen, Jianlei Yang, and Wenjian Yu. Fast physics-based electromigration analysis for full-chip networks by efficient eigenfunction-based solution. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 40(3):507–520, 2021.
- [15] Wentian Jin, Sheriff Sadiqbacha, Zeyu Sun, Han Zhou, and Sheldon X.-D. Tan. Em-gan: Data-driven fast stress analysis for multi-segment interconnects. In *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, pages 296–303, Oct. 2020.
- [16] H. Zhou, W. Jin, and S. X.-D. Tan. GridNet: Fast Data-Driven EM-Induced IR Drop Prediction and Localized Fixing for On-Chip Power Grid Networks. In *Proceedings of the 39th International Conference on Computer-Aided Design, ICCAD '20*, pages 1–9, November 2020.
- [17] Han Zhou, Shuyuan Yu, Zeyu Sun, and Sheldon X.-D. Tan. Reliable power grid network design framework considering EM immortalities for multi-segment wires. In *Proc. Asia South Pacific Design Automation Conf. (ASPAC)*, pages 1–6, Jan. 2020.
- [18] Han Zhou, Yijing Sun, Zeyu Sun, Hengyang Zhao, and Sheldon X.-D. Tan. Electromigration-Lifetime Constrained Power Grid Optimization Considering Multi-Segment Interconnect Wires. In *Proceedings of the 23rd Asia and South Pacific Design Automation Conference, ASP-DAC '18*, pages 399–404, New York, NY, Jan. 2018. IEEE Press.
- [19] Z. Sun, S. Yu, H. Zhou, Y. Liu, and S. X.-D. Tan. EMSpice: Physics-Based Electromigration Check Using Coupled Electronic and Stress Simulation. *IEEE Transactions on Device and Materials Reliability*, 20(2):376–389, June 2020.
- [20] Z. Lu, W. Huang, M. R. Stan, K. Skadron, and J. Lach. Interconnect Lifetime Prediction for Reliability-Aware Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 15(2):159–172, Feb 2007.
- [21] H.-B. Chen, S. X.-D. Tan, J. Peng, T. Kim, and J. Chen. Analytical modeling of electromigration failure for vlsi interconnect tree considering temperature and segment length effects. *IEEE Transaction on Device and Materials Reliability (T-DMR)*, 17(4):653–666, 2017.
- [22] Chase Cook, Zeyu Sun, Ertugrul Demircan, Mehul D. Shroff, and Sheldon X.-D. Tan. Fast Electromigration Stress Evolution Analysis for Interconnect Trees Using Krylov Subspace Method. *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, 26(5):969–980, May 2018.
- [23] Ali Abbasinasab and Malgorzata Marek-Sadowska. Non-uniform temperature distribution in interconnects and its impact on electromigration. In *Proceedings of the 2019 on Great Lakes Symposium on VLSI, GLSVLSI '19*, pages 117–122, New York, NY, USA, 2019. ACM.
- [24] M A Korhonen, P Borgesen, D D Brown, and Che-Yu Li. Microstructure based statistical model of electromigration damage in confined line metallizations in the presence of thermally induced stresses. *Journal of Applied Physics*, 74(8):4995–11, 1993.
- [25] M. Kavousi, L. Chen, and S. X.-D. Tan. Electromigration Immortality Check considering Joule Heating Effect for Multisegment Wires. In *Proc. Int. Conf. on Computer Aided Design (ICCAD)*, pages 1–8, 2020.
- [26] M. A. Korhonen, P. Borgesen, K. N. Tu, and C.-Y. Li. Stress evolution due to electromigration in confined metal lines. *Journal of Applied Physics*, 73(8):3790–3799, 1993.
- [27] V. Sukharev, A. Kteyan, and X. Huang. Postvoiding stress evolution in confined metal lines. *IEEE Transactions on Device and Materials Reliability*, 16(1):50–60, 2016.