Accelerating Electromigration Aging for Fast Failure Detection for Nanometer ICs

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***Abstract*—For practical testing and detection of electromigration (EM) induced failures in dual damascene copper interconnects in today's and future sub-10nm ICs, one critical issue is how to create stressing conditions so that the chip will fail exclusively under EM in a very short period of time so that EM signoff and validation can be carried out efficiently. In this work, we propose novel EM wearout-acceleration techniques for practical VLSI chips. We will first review the recently proposed three-phase physics-based EM models and discuss the important factors contributing to the EM aging process. Then we propose a new formula for fast estimation of the void's saturation volume for general multi-segment interconnect wires, which is important for EM mortality check. We then investigate two strategies to accelerate the EM failure process: reservoir-enhanced acceleration and temperature-based acceleration. First we show that multi-segment interconnects with reservoir structures and their stressing currents can be exploited to significantly speedup the EM wearout process. Such configurable reservoir-based wires are very flexible and can achieve various EM accelerations at the costs of some routing resources. Additionally, we show that further acceleration can be achieved by increasing temperature. On average, 10% increase in temperature yields about 10X wearout acceleration. However, purely temperature based acceleration is not possible since practical VLSI chips have temperature limitations which must be strictly enforced to ensure the chip only fails under EM, and not due to other reliability effects. In this study, we show that it is possible to achieve significantly high acceleration while staying within the feasible operating zones by combining the two acceleration techniques. Experimental results show that by combining temperature and reservoir accelerations, we can reduce the EM lifetime of a chip from 10 years down to a few hours (about 10^5 acceleration) under the $150^{\circ}C$ temperature limit, which is sufficient for practical EM testing of typical nanometer CMOS ICs.**

I. Introduction

Electromigration (EM) is the top reliability concern of copper based back-end-of-the-line (BEOL) interconnects, both for current and future ICs in 10 nm technology and below. 2015 ITRS interconnect predicts that EM lifetime of interconnects in VLSI chips will be reduced by half for each generation of nodes [1]. This is primarily due to increasing current densities and shrinking wire line cross sections, which determine the critical sizes for EM effects. On the other hand, many applications ranging from automatic electronics, to medical devices and aerospace equipment require a very long lifetime and have very demanding reliability requirements. As a result, testing and verification of reliability, specially EM-reliability, of VLSI chips used in those applications becomes critical.

For many practical applications, such as automatic electronics, reliability of 10 years or more is typically expected [2]. However, one cannot wait for 10 years to test the IC's used on those applications. As a result, accelerated testing and stressing is required such that the testing processes can be completed within a few hours. From 10 years to 1 hour requires about 10^5X (0.87×10^5 exactly) acceleration of time-to-failure (TTF). However it is challenging to achieve such acceleration in practical VLSI chips.

There are two main challenges. First, we need to have scalable EM models which are accurate both across the high stress conditions used during testing, as well as the normal use conditions. The model data from these acceleration conditions can then be used to predict the actual TTF when the chip is subjected to a normal workload. Existing Black and Blech's based EM models [3], [4], which are empirically based models, are considered too conservative. Moreover, they do not fit well over a wide range of stressing conditions as the activation energy and current exponents are stress condition dependent [5]. This will make it difficult to apply the results obtained at the high stressing condition to the normal use conditions. Second, once we have an accurate EM model, we need to find realistic EM stressing conditions and other accelerating techniques to achieve the desired wearout acceleration. This has to be done while ensuring that the chip only fails under EM, not other reliability effects.

Recently, a number of physics-based EM models and assessment techniques have been proposed [6]–[14]. These EM models are primarily based on the hydro-static stress diffusion kinetics in the confined metal wires and therefore have a more accurate time to failure estimation for general interconnect wires over a wide range of stress conditions. Furthermore, all these models consider a multi-phase EM process. Recently a very accurate 3-phase EM model was proposed [14], which better described the post-voiding wire resistance change behaviors of copper dual damascene interconnects. However, in the post-voiding phase, the void will grow into the so-called saturated-volume in the steady state. Although methods exist for fast saturation-volume estimation of two-segment wires [15]), no such methods exists for general multi-segment interconnect structures such as the one shown in Fig. 1. The saturation-volume estimation of a void is important for determining the immortality of multi-segment interconnect wires (especially with reservoirs) in the steady state.

To accelerate the EM failure process, raising temperature is the most effective method as the EM effects are exponentially dependent on temperature. However, elevated temperature will lead to other failures very quickly as well and there exist some thermal upper limit for practical MOSFET-based microprocessors [16]. Increasing the current density is another way to accelerate EM wearout. However, it is well known that the impacts of current density is reversely proportional to the time-to-failure of EM with current exponent between 1 and 2 [17]. This limits the impacts of current density on acceleration. Furthermore, very high current densities can lead to thermal runaway due to excessive Joule heating [18]. Hence a method

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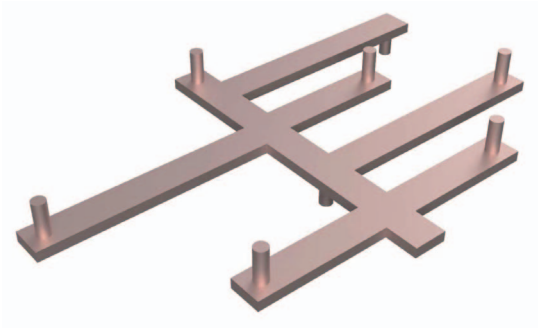


Fig. 1. Illustration of a multi-segment Interconnect wire structure

that combines the effects of current density and temperature might yield better results while staying within the previously discussed constraints.

In this work, we investigate the EM stressing conditions to accelerate the EM failures based on the recently proposed three-phase physics-based EM models. Our new contributions lies in the follow aspects: (1) first, we propose a new formula for fast estimation of the saturation volume of voids for general multi-segment interconnects, which is critical for EM mortality check; (2) second, we propose two strategies to accelerate the EM failure process: the temperature-based acceleration and reservoir-enhanced acceleration. First, we show how the multi-segment interconnect wires with reservoir structures can be exploited to speedup the EM wearout significantly. Such configurable reservoir-based wires are very flexible and can achieve various EM accelerations at the cost of some routing resources. Second, we show that 10% increase in temperature can achieve about $10X$ acceleration in general. But on-chip temperature has an upper limit for the working operations of typical CMOS circuits. Experimental results show that by combining temperature and reservoir accelerations, we can reduce the EM lifetime from 10 years down to a few hours (about 10^5 acceleration) under the $150°C$ temperature limit, which is sufficient for practical EM stressing and validation of typical nanometer CMOS ICs.

II. Review of EM physics and 3-phase EM model

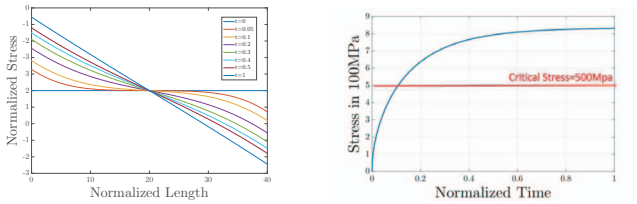
A. Review of EM physics and stress modeling

EM is a physical phenomenon of the migration of mental atoms along the direction of the applied electrical field. Atoms (ether lattice atoms or defects / impurities) migrate along the trajectory of conducting electrons. During the migration process, hydrostatic stress is generated inside the embedded metal wire due to momentum exchange between lattice atoms. Overtime, void and hillock formation is caused by conducting electrons at the opposite ends of the wire. Indeed, when metal wire is passivated into a rigid confinement, which is the case for copper dual damascene structure, the wire volume changes (induced by the atom depletion and accumulation due to migration) , and creates tension at the cathode end and compression at the anode end of the line.

Mathematically, transient hydrostatic stress evolution due to EM effects in confined metal $\sigma(x,t)$ before void is formed can be described by Korhonens equation [19]:

$$\begin{aligned} &\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma}{\partial x} + G\right)\right], \ \texttt{at } 0 < t < t_{nuc} \\ &BC: \frac{\partial \sigma}{\partial x}(0,t) = G, \ \texttt{at } 0 < t < t_{nuc} \\ &BC: \frac{\partial \sigma}{\partial x}(L,t) = -G, \ \texttt{at } 0 < t < t_{nuc} \end{aligned} \tag{1}$$

where, $\kappa = D_a B\Omega/kT$, T is the absolute temperature, k is the Boltzmann constant, B is the effective bulk elasticity modulus and $G = \frac{eZ\rho j}{\Omega}$, where e is the electron charge, eZ is the effective charge of the migrating atoms, Ω is atomic volume, ρ is the wire electrical resistivity, and j is the current density.



(a) (b)

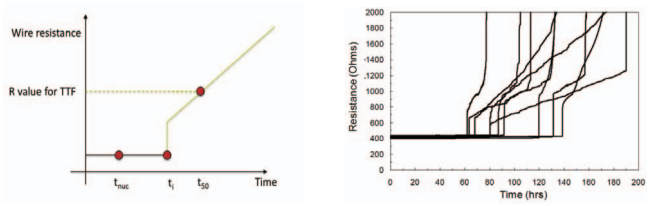
Fig. 2. (a) EM-stress distribution change over time in a simple metal wire. (b) EM-stress evaluation versus time.

Fig. 2(a) shows stress development over time in a metal line with Korhonens equation. Over time, tensile (positive) stress will develop at the cathode (left) node and compressive (negative) stress will develop at the anode (right) node. The stress changes polarity in the middle of the wire. The built-up stress (its gradient) will serve as the counter force for atomic flux. Fig. 2(b) shows stress evolution on the cathode, which reaches a steady-state over time. If the highest stress at the cathode node exceeds the critical stress, voids will be created. The time to reach the critical stress is called nucleation time(t_{nuc}). After the void is nucleated, it will begin to grow, consequently raising the wire resistance.

B. The 3-phase physics-based compact EM model for multi-segment wires

As mentioned above, the EM failure process in general can be viewed as two phases: the nucleation phase, in which void is generated after the critical stress is reached, and the growth phase, in which void starts to grow. Existing compact EM models are also versed in terms of the two phases, where each phase is described by time-to-failure as a function of current density and other parameters [9], [20]. However, such a simple EM model ignores the fact that when the void is nucleated or formed, it will not change the wire resistance immediately. It is observed experimentally that there exists a so-called *critical void size* [21], [22], which is typically the via-diameter or cross section area of the interconnect wire. Since the conductivity of Cu is much higher than the barrier layers, resistance of the wire does not change until the void grows to a point where its volume equals or becomes larger than the cross-section of the via or wire. Only then will all the current start to flow over the thin barrier layer, which will lead to a very high current density and consequent joule heating. The joule heating in turn will lead to a small resistance jump, indicating the end of this phase. Fig. 3(b) shows the experimentally measured resistance change over time. The

small resistance jumps are obviously visible. Also, sometimes the barrier layers are not very stable, due to manufacturing process variations, causing the barrier layer to quickly burn out causing an open circuit as is shown in Fig. 3(b) [22].



(a) (b)

Fig. 3. (a) The proposed 3-phase EM model and the resulting resistance change over time, courtesy of [14]. (b) Measured resistance change, courtesy of [22].

Based on these observations, a three phase EM model has been proposed for a single segment wire [14]. In the new model, we have three phases as shown in Fig. 3(a): (1) the *nucleation phase* from $t = 0$ to t_{nuc}; (2) the *incubation phase* from t_{nuc} to the t_i; and (3) the *growth phase* starting from t_i to t_{50}, t_{50} together indicate the time-to-failure in statistical term (50% of the samples fail). In this paper, we extended this 3-phase EM model to consider multi-segment wires.

In the **nucleation phase**, a void is not formed until time t_{nuc}, hence the resistance does not increase. Here, the stress can be modeled by Korhonen's equation in (1) and the nucleation time can be estimated by solving the Korhonen's equation based on finite element or finite difference methods [23].

In the **incubation phase**, which is defined by the time period from t_{nuc} to the t_i, the void is nucleated, but its size is not significant. Hence the resistance will remain almost the same. The incubation time($t_i - t_{nuc}$) can be estimated as

$$t_i - t_{nuc} = \frac{\Delta L_{crit}}{v_d} \tag{2}$$

Here ΔL_{crit} is the length of critical void size and v_d is the void's growth rate. For a single segment wire, v_d is related to automic flux (J) as $v = \Omega J$ [24], where Ω is atomic volume. Automic flux J is the number of atoms crossing a unit area per unit time. Thus, the atoms crossing per unit length can be expressed as JW. $J = \frac{D_a f}{\Omega k T}$, where f is electron wind force per atom: $f = eZ\rho j$.

For a multi-segment tree, all segments connected with the void can contribute to the void growth. Electron wind at each segment can accelerate or slow down the void growth based on their directions. So total atom flux can also be expressed as a combination of all the fluxs on the segments. For multi-segment wires, the effective atomic flux per unit length $v_d W_m$ is the void growth rate on the main segment which can be expressed as

$$v_d = \Omega J_m^* = \Omega \frac{1}{W_m} \sum_i J_i W_i = \frac{D_a e Z \rho}{k T W_m} \sum_i j_i W_i \tag{3}$$

Here j_i and W_i are the current density and width of the ith segment. W_m is the width of the main segment where the void is formed and J_m is the total flux impact on the main segment. Here, we use $J_m^* = \frac{1}{W_m} \sum_i J_i W_i$ to compute the effective atomic flux J_m on the main segment. Note if we only have one segment, then $v_d = \frac{D_a e Z \rho j}{kT}$ as shown in [21].

Finally, in the **growth phase**, defined by time period from t_i to t_{50}, the void reaches its critical size and blocks the cross section above the via, forcing the current to flow through the liner or barrier layers. Since this liner is very thin, and its resistivity is much larger than copper, the current density and resistance on the linear will be very high. At this point, resistance of the wire will continue to increase over time after a small resistance jump due to joule heating [25]. Hence, given incubation time t_i and v_d in (3), the time and the resistance change can be expressed as [6]:

$$t - t_i = \frac{\Delta R(t)}{v_d [\frac{\rho_{Ta}}{h_{Ta}(2H + W_m)} - \frac{\rho_{Cu}}{HW_m}]} \tag{4}$$

where ρ_{Ta} and ρ_{Cu} are the resistivities of the (barrier) liner material (Ta for instance) and copper respectively, W_m is the line width of the segment where void is formed (main segment), H is the copper thickness, and h_{Ta} is the liner layer thickness.

One important aspect in both incubation and growth phases is that the void volume will saturate in steady state. If saturation happens before critical void size is reached, the wire can still be rendered as immortal. As a result, determining the void's saturation volume is critical. While there are methods of determining the saturation volume, they are limited to 2-segment wires, which is not practical for real interconnect structures. In the following section, we propose a new method of computing the void saturation volume for general multi-segment interconnects.

III. The New Void Saturation Volume Estimation for General Multi-Segment Wire

As previously mentioned, computing the saturation void volume at steady state is critical for the immortality check of a wire. After a void is formed in a segment, the tensile (positive) stress around the void will gradually reduce to zero and the stress distribution will become compressive (negative) as shown in Fig. 4.

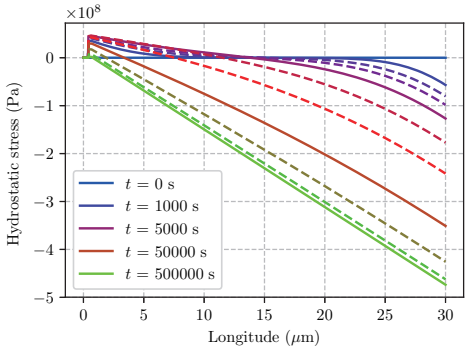


Fig. 4. The typical stress evolution on a 30 μm copper wire computed by finite element analysis.

From the physics perspective, once a void is formed, the void volume $V_v(t)$ in a multi-segment wire will satisfy the following atom conservation equation [26].

$$V_v(t) = A \int_{\Omega_L} \frac{\sigma(V,t)}{B} dV \tag{5}$$

where Ω_L is the volume of the remaining interconnect wire and A is its cross section area. For the one dimensional, single

segment case with wire length L, the steady state saturation volume of the void becomes

$$V_{sat} = A\int_0^L \frac{\sigma(x)}{B}dx = \frac{A\sigma_{max}L}{2B} \tag{6}$$

where σ_{max} is the maximum stress in steady state. Note that V_{sat} represents the void volume per unit cross-section area. Since length of the void is much smaller than the length of the wire (smaller than 1% of the segment), total length L is used here instead of the length of the remaining interconnect. Going back to Korhonens equation, in the steady state, we have

$$\begin{aligned}\frac{\partial\sigma}{\partial x} &= \frac{\sigma_{max}}{L} = \frac{j\rho eZ^*}{2\Omega} \\ \sigma_{max} &= \frac{j\rho eZ^*L}{2\Omega} = \frac{VeZ^*L}{2\Omega}\end{aligned} \tag{7}$$

where V is the voltage between cathode and anode of the wire. Using (6) and (7), we get

$$V_{sat} = \frac{Aj\rho eZ^*L^2}{2\Omega B} = \frac{AVeZ^*L}{2\Omega B} \tag{8}$$

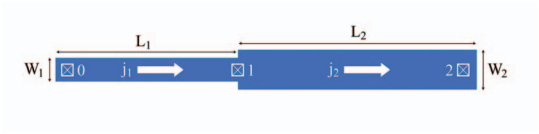
If we have the initial stress distribution, then

$$V_{init} = \frac{A\sigma_{init}L}{B} \tag{9}$$

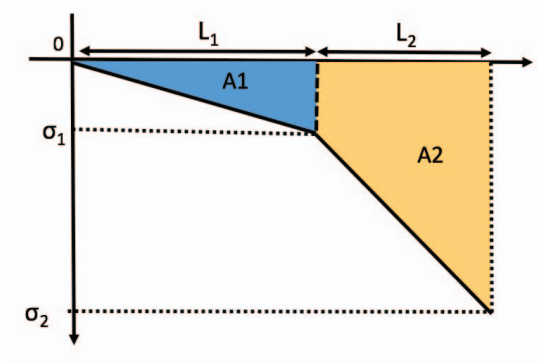
Therefore, void saturation volume, V_{sat}, for a single wire can be expressed as

$$V_{sat} = A(\frac{\sigma_{init}L}{B} + \frac{j\rho eZ^*L^2}{2\Omega B}) = A(\frac{\sigma_{init}L}{B} + \frac{VeZ^*L}{2\Omega B}) \tag{10}$$

which agrees exactly with [27]. However, this method only works for one dimensional single wires.



(a)



(b)

Fig. 5. (a) A two-segment wire and the direction indicate electron flow (b) Stress integration area of a two-segment wire

In this paper, we propose a formula to estimate the saturation volume for general multi-segment interconnect wires where each wire segment may have different widths. For a single segment (such as $L_1$from Fig. 5(a)), the stress between cathode and anode can be expressed as

$$\sigma_c - \sigma_a = \frac{(V_a - V_c)eZ}{\Omega} = \frac{jL\rho eZ}{\Omega} \tag{11}$$

where σ_c and σ_a represent stress on cathode and anode respectively, and V_c and V_a represent voltages on cathode and anode respectively. At the steady state , the stress is linearly distributed on the mental wire as shown by the shaded areas in Fig. 5(b). Since we need to consider the width of each segment, the problem becomes a 2D stress-area integration problem. The void volume, $A_{sat,i}$, for a segment i, which is the void volume per unit height of the wire or the essentially *saturation area* of the void, can be computed by stress and area integration as:

$$\begin{aligned}A_{sat,i} &= ((-\sigma_{c,i}) + (-\sigma_{a,i})) \times \frac{L_iW_i}{2B} \\ &= (-2\sigma_{c,i} + \frac{V_ieZ}{\Omega}) \times \frac{L_iW_i}{2B} \\ &= (-2\sigma_{c,i} + \frac{j_iL_i\rho eZ}{\Omega}) \times \frac{L_iW_i}{2B}\end{aligned} \tag{12}$$

where V_i,j_i,L_i,W_i are the voltage difference between anode and cathode, current density, length, and width of the segment respectively. $\sigma_{c,i}$ is the steady state stress on the cathode of the segment i, which becomes 0 where the void is nucleated. Except for the segment with the void, steady-state stress on cathode of other segments are the same as the anode of the segment connected to them. With this, we have the following results:

Proposition 1. *For a general multi-segment wire, assume that a void is formed in the cathode node of one of the segments and all the initial stress' are zero. Here, the saturation volume of the void V_{sat} can be computed as*

$$\begin{aligned}A_{sat} = \sum_i A_{sat,i} &= \sum_i (-2\sigma_{c,i} + \frac{V_ieZ}{\Omega}) \times \frac{L_iW_i}{2B} \\ &= \sum_i (-2\sigma_{c,i} + \frac{j_iL_i\rho eZ}{\Omega}) \times \frac{L_iW_i}{2B}\end{aligned} \tag{13}$$

where $A_{sat,i}$, $\sigma_{c,i}$, j_i, L_i and W_i represent the void area, stress at the cathode, current density, length and width of the ith segment respectively. If A_{sat} is smaller than the area of via, resistance will never increase. The interconnect tree can be considered as immortal in this case. If a non-zero initial stress is considered, we can add the initial stress contributions as shown in (10). □

In the following, we go through a few example to illustrate the new formula (13) The first example is a three terminal wire shown in Fig. 5. Here, stress at node 1 and node 2 can be expressed as

$$\begin{aligned}\sigma_1 &= 0 - \frac{(V_1 - 0)eZ}{\Omega} = -\frac{j_1L_1\rho eZ}{\Omega} \\ \sigma_2 &= -\sigma_1 - \frac{(V_2 - V_1)eZ}{\Omega} = -\frac{(j_1L_1 + j_2L_2)\rho eZ}{\Omega}\end{aligned} \tag{14}$$

Fig. 6 shows calculated stress at steady state during growth phase. The stress estimation agrees with the results in Eq. (14). As a result the void saturation can be computed as:

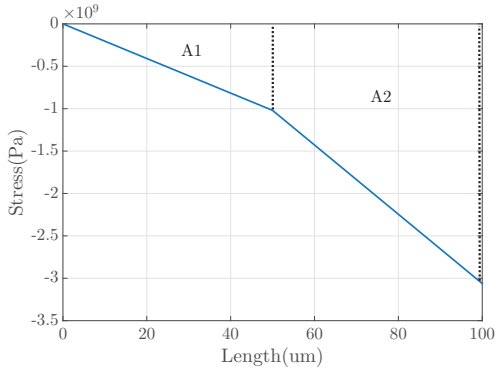


Fig. 6. Stress distribution for two-segment wire at steady state

$$A_{sat,2seg} = \frac{-\sigma_1 L_1 W_1 + (-\sigma_1 - \sigma_2) W_2 L_2}{2B} = \frac{j_1 L_1^2 W_1 \rho e Z}{2B\Omega} + \frac{(2j_1 L_1 + j_2 L_2) L_2 W_2 \rho e Z}{2B\Omega} \quad (15)$$

For a two-segment wire structure, the saturation void volume estimation was proposed in [15] where segment 2 is treated as a reservoir ($j_2 = 0$). However, in this work, the problem is still considered as 1D where all wire segments are assumed to have the same width. The saturation void volume, V_{max}, computed using this method is given below:

$$V_{max}/wh = L_1 + L_2 - \frac{B}{K}[\sqrt{(\frac{Kp}{B} + 1)^2 + \frac{2L_1 K}{B}} - 1] \quad (16)$$

where $K = eZ\rho j/\Omega$. Note, V_{max}/wh is actually the saturation length and V_{max}/w is the saturation area. This work considers the void size formulated in the cathode of the L_1 segment and its impacts on the stress distributions. However, our analysis shows that the void size can be small compared to the segment length and therefore negligible. Comparison of the void volume calculated using this method and the method that we propose is shown in Table. I. Where A_1

TABLE I
COMPARISON OF VOID AREA OF TWO METHODS (WIRE WIDTH = $1um$)

L_1 (um)	L_2 (um)	j (A/m^2)	A_1 (um^2)	A_2 um^2
10	10	10^{10}	0.0609	0.0614
20	10	10^{10}	0.1616	0.1636
10	20	10^{10}	0.1010	0.1023
10	10	5×10^9	0.0306	0.0307

is the saturation area calculated using [15] and A_2 is the saturation area calculated using the proposed method. Note, the difference of these two methods are very small. Among the four test cases in Table. I, the maximum difference is only 1.28%. In our future work, we will also consider the impact of our void volume calculation on the stress distributions.

For the last example we will consider the T-intersection shown in Fig. 7 In this case a void will be formed at node 0, stress at other nodes can be calculated as:

$$\sigma_1 = -\frac{V_1 eZ}{\Omega} = -\frac{j_1 L_1 \rho e Z}{\Omega}$$
$$\sigma_2 = \sigma_1 - \frac{(V_2 - V_1) eZ}{\Omega} = -\frac{(j_1 L_1 + j_2 L_2)\rho e Z}{\Omega} \quad (17)$$
$$\sigma_3 = \sigma_1 - \frac{(V_3 - V_1) eZ}{\Omega} = -\frac{(j_1 L_1 + j_3 L_3)\rho e Z}{\Omega}$$

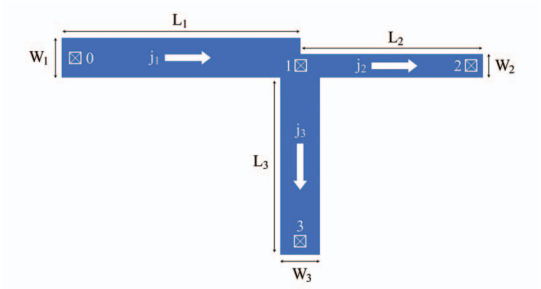
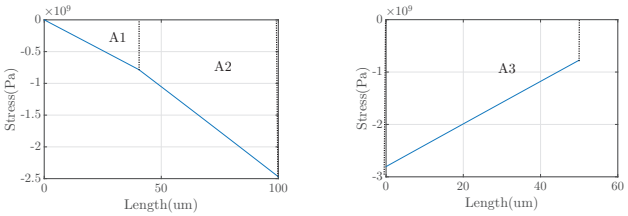


Fig. 7. A T-shaped wire (Arrows indicate electron flow)



(a) (b)

Fig. 8. (a) Stress on horizontal segment 0-2; (b) Stress on vertical segment 1-3

Fig. 8 shows stress at steady state during the growth phase.

Here, the saturation void area then can be calculated as

$$A_{sat,3seg} = \frac{-\sigma_1 L_1 W_1 + (-\sigma_1 - \sigma_2) L_2 W_2 + (-\sigma_1 - \sigma_3) L_3 W_3}{2B} = \frac{j_1 L_1^2 W_1 \rho e Z}{2B\Omega} + \frac{(2j_1 L_1 + j_2 L_2) L_2 W_2 \rho e Z}{2B\Omega} + \frac{(2j_1 L_1 + j_3 L_3) L_3 W_3 \rho e Z}{2B\Omega} \quad (18)$$

IV. ACCELERATION FOR STRUCTURE WITH RESERVOIR

In this section we discuss two techniques of accelerating the EM wearout process based on the new 3-phase model. The first is a novel reservoir-enhanced acceleration technique and the second is a temperature-based technique. We will show the combination of the two acceleration mechanisms in the experimental section.

Before we discuss the two techniques, we will conduct some preliminary analysis on the two-segment interconnect structure shown in Fig. 9. Here one of the segments is an active current-carrying wire (main branch), while the other is a passive reservoir with zero current; the two segments can have different widths. It is known that adding a reservoir to the cathode node reduces stress and increases lifetime [28], [29]. By adjusting the sizes (area) or locations of the reservoirs, one can configure the desired TTF of the EM wires [29]. Note, in our numerical simulation, the time-to-failure (TTF) is defined as 10% resistance changes, which is applied to all experimental results as well.

We did some studies on how the different widths and lengths of the reservoirs will affect the TTF of the reservoir-enabled wires. Fig 10 shows the results. As we can see, increasing the length and width of the reservoir will benefit the lifetime. Doubling the length increases lifetime by around 13.7%, while doubling the width increases lifetime by 89.5%.

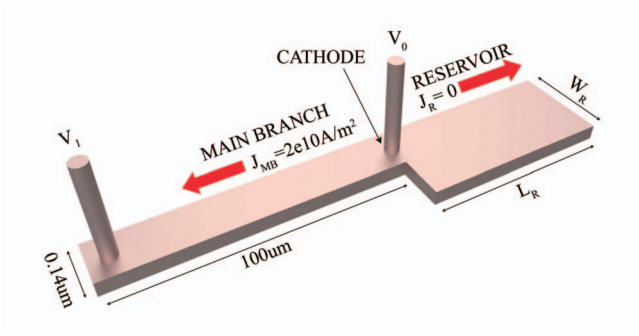
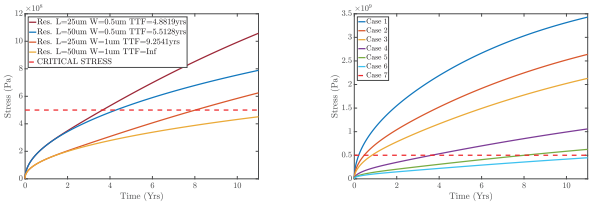


Fig. 9. A two-segment wire structure with a passive reservoir



(a) Length impact on TTF (b) Width impact on TTF

Case	L_R (um)	W_R (um)	TTF (hrs.)
1	0	0	1.26×10^4
2	25	0.07	1.49×10^4
3	25	0.14	1.81×10^4
4	25	0.5	4.28×10^4
5	25	1	8.11×10^4
6	25	1.5	9.64×10^4+
7	CRITICAL STRESS		

Fig. 10. (a) Reservoir length impact on TTF of the wire; (b) reservoir width impact on TTF.

A. *Configurable reservoir based EM failure acceleration*

As we know, adding a reservoir to the cathode node can extend the lifetime of a wire. Bear in mind, the reservoir is also a wire segment but with zero current density. Thus, if we can control the current density in the reservoir segment, we can effectively control the EM lifetime of the wire. Zero current density will yield the longest lifetime, while increasing the current density will reduce lifetime by some factor. For instance, let us consider the structures shown in Fig. 11. The two structures (top and bottom) are identical, except for the current density in their reservoir segment. The top shows a two segment wire with a passive reservoir, while the bottom shows the same structure but with the reservoir disabled (current flowing through the reservoir). If we can instantaneously disable the reservoir in this way, the stress at the cathode will increase significantly and lead to an accelerated nucleation phase. Additionally, the new atom flux generated from the reservoir segment will also contribute to accelerating the void growth phase. As a result, the TTF of the wire will be reduced significantly. This is the key observation, which is the basis for our reservoir-based EM acceleration design.

Specifically, we start with an interconnect structure designed for an EM lifetime of more than 10 years, which is required by many electronic application. As Fig. 10(a) and Fig. 10(b) show, this can be easily accomplished by configuring the size of the reservoir segment. To achieve EM wearout acceleration, we propose a novel design shown in Fig. 12. The structure consists of a two segment wire (one reservoir and one main branch), one MOSFET device (switch to disable the reservoir)

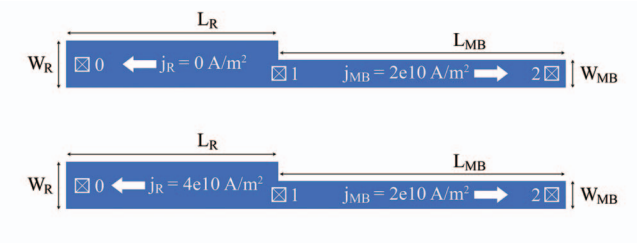


Fig. 11. Structure with passive reservoir (top) and with disabled reservoir(bottom).

and two resistors R_1 and R_2 to control the currents in two wire segments. The bottom figure Fig. 12 shows the 3D view of this layout of this design. In the normal use, the reservoir will remain passive (zero current density) until $Acc.Signal$ is triggered. Once acceleration is triggered, the current density in the reservoir will become non-zero, thus disabling the reservoir and accelerating failure.

As we will show later, the desired accelerated TTF can be configured by adjusting the reservoirs geometry (W_R and L_R) and it's current density j_R. The resistors, $R1$ and $R2$, in the circuit are used to set the current densities j_R and $j_M B$, respectively, based on $R = \frac{V_1 - V_0}{I}$ and $I = (H * W)j$, where I is current in amps, W is the width of the wire segment in meters, and H is the height of the wire segment in meters. Note that H depends on the layer of metalization. For a 32nm process, H is typically 100nm on metal layer 1.

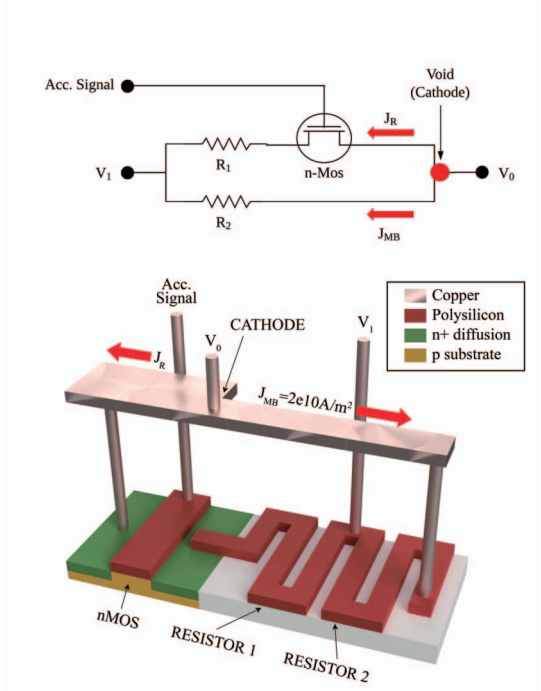


Fig. 12. The proposed configurable reservoir-based EM wearout acceleration circuit.

Using the proposed method, the structure in Fig. 12 can be configured for a TTF of 10+ years but, at the same time, be made to fail quickly (within few days) when $Acc.Signal$ is triggered. TTFs for both normal ($j_R = 0A/m^2$) and accelerated ($j_R = 4e10A/m^2$) cases for the structure shown in Fig. 12 with various reservoir configurations are given in

TABLE II
NORMAL VERSUS ACCELERATED TTF UNDER DIFFERENT CONFIGURATION

L_R (um)	W_R (um)	TTF (hrs.)	Acc. TTF (hrs.)	Acc.
25	0.7	5.76×10^4	1.58×10^3	37.52X
25	0.8	6.53×10^4	1.40×10^3	46.91X
25	0.9	7.32×10^4	1.31×10^3	56.09X
25	1	8.10×10^4	1.23×10^3	65.63X
25	1.5	9.64×10^4+	9.64×10^2	98.21X+
25	2	9.64×10^4+	8.76×10^2	111.11X+
50	0.7	7.52×10^4	1.53×10^3	49.02X
50	0.8	9.16×10^4	1.39×10^3	65.76X
50	0.9	9.64×10^4+	1.31×10^3	73.83X+
50	1	9.64×10^4+	1.23×10^3	78.01X+
50	1.5	9.64×10^4+	9.64×10^2	98.21X+
50	2	9.64×10^4+	8.76×10^2	111.11X+

Table. II. The Impact of various j_R for accelerated cases is shown separately in Table. III where $L_R = 25um$ and $W_R = 1um$.

TABLE III
IMPACT OF j_R ON EM FAILURE ACCELERATION

$j_R(A/m^2)$	Acc. TTF (hrs.)	Acc.
0	8.10×10^4	baseline
0.5e10	3.23×10^4	3.5X
1.0e10	8.67×10^3	9.4X
1.5e10	4.73×10^3	17.3X
2.0e10	3.15×10^3	25.7X
2.5e10	2.37×10^3	34.7X
3e10	1.84×10^3	44.8X
3.5e10	1.49×10^3	55.3X
4.0e10	1.23×10^3	65.7X

B. Temperature-based EM failure acceleration

The second technique uses temperature to accelerate the EM effects. In this section we will study the TTF acceleration achieved by raising the temperature of the two-segment structure shown in Fig. 9. But we need to bear in mind the temperature limits of practical VLSI chips. We want to ensure that the chip only fails under EM wearout, not other factors. Therefore, we should not use temperatures above 150C for EM acceleration.

Using the proposed multi-segment 3-phase EM model, we see an exponential relationship between temperature and EM induced time-to-failure (Fig. 13) for the structure shown in Fig. 9 with $L_R = 30um$ and $W_R = 1um$. A 10% increase in temperature yields almost 10x decrease in TTF (Table. IV). This is no surprise, since it indeed agrees with Black's equation. Similar to the reservoir-based acceleration technique, this method also reduces lifetime from 10+years to a few days (under 150C limit).

Table. IV shows some example points we picked from Fig. 13. As can be seen, when temperature increase 61%(increase 10% every time, increase 61% after 5 steps $(1.1^5 - 1)$, the TTF decrease 1.39×10^5times.

TABLE IV
IMPACT OF TEMPERATURE ON TTF

Temp. (K)/(C)	TTF (hrs.)	Temp. (K)/(C)	TTF (hrs.)
318K / 44.9C	2.06×10^6	423.2K / 150.1C	8.81×10^2
349.8K / 76.7C	1.19×10^5	465.6K / 192.5C	1.01×10^2
384.8K / 111.7C	9.04×10^3	512.2K / 239.1C	15.6

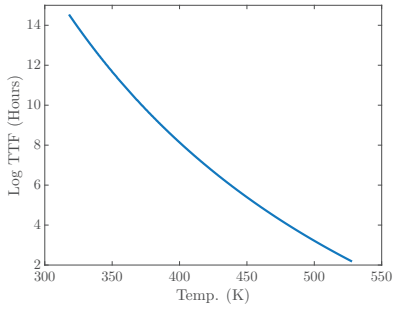


Fig. 13. Impact of temperature on TTF

V. NUMERICAL RESULTS AND DISCUSSIONS

In this section, we validate the proposed saturation area EM model by comparing it against the finite element method (FEM) simulation from COMSOL for the post-voiding process [14], [23]. We compare the two methods on the 13-segment interconnect wire shown in Fig. 14. Here, the width

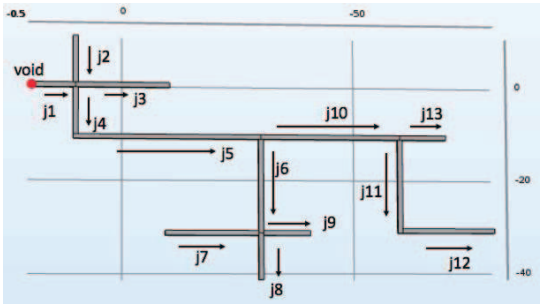


Fig. 14. Complex multi-segment structure.

of all the wires are 0.2 um, the current densities and lengths of all the segment are given in Table. V, where $Brch$ is branch index, J is current density, Lth is the length of the wire. As shown in the figure, the void is formed on $segment1$.

TABLE V
PARAMETERS FOR THE 13-SETMENT INTERCONNECT WIRE

Brch#	CD (A/m^2)	Lth (um)	Brch#	J (A/m^2)	Lth (um)
1	10×10^9	10	8	15×10^9	10
2	5×10^9	10	9	5×10^9	10
3	5×10^9	20	10	10×10^9	30
4	5×10^9	10	11	5×10^9	20
5	$10 \times e^9$	40	12	5×10^9	20
6	5×10^9	20	13	5×10^9	10
7	5×10^9	20	–	–	–

Fig. 15 compares the saturation area calculated using the proposed model and the void area computed using COMSOL. As we can see, the results are almost identical (0.3% difference).

We now present the numerical results from combining the two acceleration techniques discussed earlier. Again we use the structure shown in Fig. 11 with $L_{MB} = 100um$, $W_{MB} = 0.14um$, $j_{MB} = 2 \times 10^4 A/m^2$, $L_R = 50um$, and $W_R = 2um$. Table VI shows the acceleration results and the stressing conditions in terms of reservoir current densities and temperatures. As we can see, in the final configuration, the lifetime changes from about 11 years (9.63×10^4 hours) down

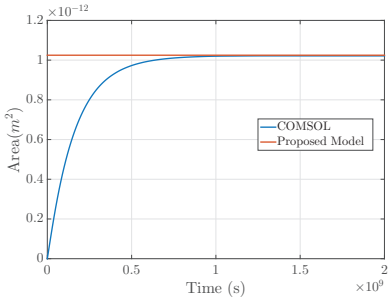


Fig. 15. Compare saturation volume with COMSOL result for 13-segment wire

to about 1.9 hours under the $150°C$ temperature limit. This represents about 5×10^4 acceleration that was achieved under the working temperature range for typical CMOS ICs.

TABLE VI
TOTAL ACCELERATION BY COMBINED RESERVOIR-BASED AND TEMPERATURE-BASED ACCELERATION

$j_R(A/m^2)$	Temp. (K/C)	TTF (hrs.)	Acc.
0	353.00K/79.85C	9.63×10^4	baseline
7e10	367.03K/93.88C	1.27×10^2	761.02X
8e10	381.16K/108.01C	38.79	2484.15X
9e10	395.09K/121.94C	13.14	7333.33X
10e10	409.12K/135.97C	4.83	19950.31X
11e10	423.15K/150.00C	1.92	50187.50X

VI. CONCLUSION

In this paper, we proposed two EM acceleration techniques for fast failure testing. We first proposed a new formula for fast estimation of the saturation volume of voids for general multi-segment interconnect wires. Then we investigated two strategies to accelerate the EM failure process: the temperature-based acceleration and the novel reservoir-enhanced acceleration. First, we showed how multi-segment interconnect structures with reservoirs can be exploited to speedup EM wearout significantly. We showed that both techniques yielded TTF acceleration from 10+ years to a few days. While, combining the two techniques yielded even better results. Our numerical results showed that it is possible to reduce the EM lifetime from 10+ years down to a few hours (about 10^5 acceleration) under $150°C$ temperature limit, which is sufficient for practical EM stressing and testing of typical nanometer CMOS ICs.

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