Electromigration-Lifetime Constrained Power Grid Optimization Considering Multi-Segment Interconnect Wires

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***Abstract*—Electromigration (EM) remains the top killer of copper-based damascene interconnects in 10nm and beyond technologies. On-chip power/ground (P/G) networks are most vulnerable to EM failures due to large and unidirectional current flows, thus proper sizing and even routing of power grid networks are critical for the full-chip EM sign-off. In this paper, we propose a new P/G network sizing technique based on recently proposed fast EM immortality check method for general multi-segment interconnect wires and physics-based EM assessment technique for fast time to failure analysis. We first show that the new P/G optimization problem subjected to voltage IR drop and new EM constraints can still be formulated as a sequence of linear programming (SLP) problem. The new optimization will ensure that all the wires will not fail if all the constraints are satisfied. To consider EM-induced aging effects on power supply networks for the target lifetime and mitigate the over-conservation of the first optimization formulation, we further propose an aging-aware P/G optimization method, which allows some short-lived wires to fail or to age and optimizes the rest of the wires considering resistance increase of those failed wire segments. In this way, the P/G networks can be optimized more effectively and become more robust and aging-aware. Numerical results on a number of IBM and self-generated power supply networks show that the new approach can effectively reduce the area of the network while ensuring immortality or improving target lifetime of all the wires, which is not the case for the existing current density constrained optimization method.**

I. INTRODUCTION

Power supply or power/ground (P/G) networks provide the power to the circuit function modules in a chip from the external power supplies. Fig. 1 shows the typical mesh-structured power supply networks with multi-layer power grids. Since they experience the largest current flows on a chip, P/G networks are more susceptible to long-term reliability issues and functional failures. These reliability issues and failures typically come from metal electromigration (EM), excessive IR drops and ΔI (Ldi/dt) noise along with recently emerging back end of line time dependent dielectric breakdowns (TDDB) [1], [2], [3], [4]. As technology scales into smaller features with increasing current density, EM-induced reliability deteriorates (the EM lifetime was projected to be reduced by half for each new technology node by ITRS 2015 [5]). This puts more challenges for designing robust power supply networks to satisfy the demanding design requirements.

One important step for power supply synthesis is to size wire width of the power grid stripes after determining the topology such that the minimum amount of chip area can be occupied. Many works have been proposed for optimizing the power supply network based on nonlinear or sequence of linear programming methods (SLP) [6], [7], [8], [9], [10], [11], [12] have been proposed. To satisfy the EM reliability, all the existing methods use the current density of individual wires as the constraint, which is mainly based on the Black's EM model [1]. However, recently studies show that the time to failure (TTF) predicted by the Black's EM model is too conservative, thus, more accurate physics-based EM models have been proposed [13], [14]. More importantly, practical VLSI interconnects have many multi-segment wires as shown in Fig. 1. A multi-segment interconnect wire consists of continuously connected high-conductivity metal within one layer of metallization. Studies and experimental data show that the current-induced stress developed in those segments are not independent [15], [16]. Furthermore, existing power supply optimization methods do not take aging effects (the target lifetime) into consideration.

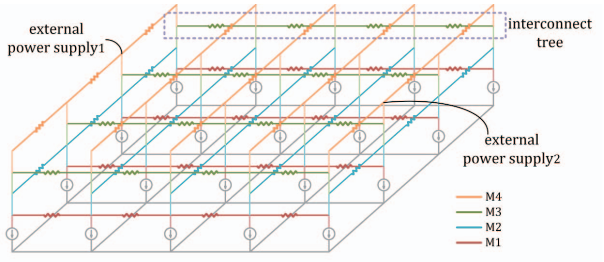

Fig. 1. A small portion of typical power grid circuits.

In this paper, we investigate on-chip power grid network optimization. We overcome the difficulties discussed above and propose a new P/G network sizing technique considering aging effects. The paper is organized as follows: Section II reviews the recently proposed voltage-based EM immortality check method and fast EM lifetime estimation method adopted in this work. Section III introduces our first EM immortality constrained P/G network optimization problem and its programming-based solution. Section IV presents our second EM-lifetime constrained P/G optimization method, which considers the EM-induced aging effects. Section V summarizes the experimental results on some P/G networks and compares them with the current density constrained method. Section VI concludes the paper.

II. REVIEW OF ELECTROMIGRATION FUNDAMENTAL AND EXISTING MODELS

EM is a physical phenomenon of the migration of metal atoms along the direction of the applied electrical field due to electron wind force. During the migration process, hydrostatic stress is generated inside the embedded metal wire on account of momentum exchange between lattice atoms. Voids and hillocks are formed by conducting electrons at the opposite ends of the wire. Once a void is formed, it can cause either early failure or late failure of the wire [17].

A. Steady-state EM-induced stress modeling

Steady-state EM-induced stress modeling helps to find mortality information of the interconnect wire quickly as no complex calculations are required. If the stress of the cathode at steady state σ_{steady} is lower than the critical stress σ_{crit}, the wire is considered to be immortal. One of the well-known steady state analysis methods is

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This work is supported in part by NSF grant under No.CCF-1527324, in part by DARPA grant under No.HR0011-16-2-0009 and in part by UC-Mexus grant under CN 16-161.

978-1-5090-0602-1/18/$31.00 ©2018 IEEE

Blech product [18], but it is only suitable for one-segment wire. Recently, a voltage-based EM immortality analysis method for multi-segment interconnect structure has been proposed [19]. An *EM voltage* (V_E) which is proportional to stress at the ground node (σ_g) is calculated as

$$V_E = \frac{1}{2A}\sum_{k\neq g} a_k V_k \tag{1}$$

where V_k is the normal nodal voltage (with respect to the cathode node g) at node k of the wire and a_k is the total area of branches connected to node k. With voltage of node i (V_i), steady-state stress at that node (σ_i) can be calculated as $\sigma_i = \beta(V_E - V_i)$, where $\beta = \frac{eZ}{\Omega}$, e is elementary charge, Z is effective charge number and Ω is the atomic lattice volume. A critical EM voltage $V_{crit,EM}$ is defined by

$$V_{crit,EM} = \frac{1}{\beta}(\sigma_{crit} - \sigma_{init}) \tag{2}$$

where σ_{init} is the initial stress. Since generally the cathode node has the lowest voltage within an interconnect wire, we may just check the cathode node instead of all the nodes, which means

$$V_{crit,EM} > V_E - V_{cat} \tag{3}$$

where V_{cat} is the voltage at cathode. Note that (3) can be applied to both power and ground networks.

B. Transient EM-induced stress estimation

Sometimes the steady-state EM-induced methods are conservative, therefore more complete models of transient hydrostatic stress evolution are needed. In general, the failure process is divided into nucleation phase and growth phase. In the nucleation phase, the stress at cathode increases. When it reaches critical stress, a void will be nucleated. The time to reach the critical stress is called nucleation time (t_{nuc}). After the nucleation phase, the void starts to grow and eventually leads to wire failure after a period of time (t_{growth}). The TTF or lifetime of the wire can be described as:

$$TTF = t_{life} = t_{nuc} + t_{growth} \tag{4}$$

1) Nucleation phase modeling: It is well-known that the nucleation phase was well modeled by Korhonen's equation [20]:

$$\frac{\partial\sigma(x,t)}{\partial t} = \frac{\partial}{\partial x}[\kappa(\frac{\partial\sigma(x,t)}{\partial x} + \Gamma)] \tag{5}$$

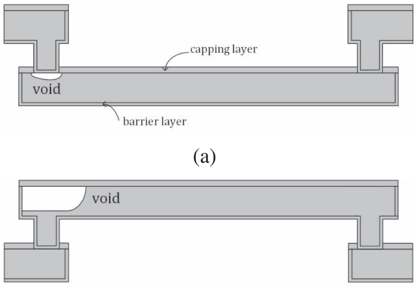
where $\kappa = \frac{D_a B\Omega}{k_B T}$, $D_a = D_0 exp(-\frac{E_a}{k_B T})$, and $\Gamma = \frac{eZ}{\Omega}\rho j$. B is effective bulk elasticity modulus, Ω is atomic lattice volume, k_B is Boltzmann constant, T is temperature, E_a is activation energy, e is elementary charge, Z is effective charge number, x is coordinate along the line, t is time, and j is current density.

Korhonen's equation describes the stress distribution accurately, however, this PDE-based model is hard to solve directly using numerical methods and has very low efficiency for tree-based EM assessment analysis. In this work, an integral transformation method for a straight multi-segment wire [21] is employed. Suppose we have n segments in a multi-segment wire, after discretizing Korhonen's equation, the stress can be expressed as:

$$\sigma(x,t) = \sum_{m=1}^{\infty}\frac{\psi_m(x)}{N(\lambda_m)}\bar{\sigma}(\lambda_m,t) \tag{6}$$

where the norm of eigenfunctions $N(\lambda_m)$ is

$$N(\lambda_m) = \int_{\chi=0}^{L}[\psi_m(\chi)]^2 d\chi \tag{7}$$



(a)

(b)

Fig. 2. Side-view of void formation: (a) void in a via-above line; (b) void in a via-below line.

and $\bar{\sigma}(\lambda_m,t)$ is transformed solution of stress, which is

$$\begin{aligned}\bar{\sigma}(\lambda_m,t) =& \bar{F}(\lambda_m)e^{-\kappa\lambda_m^2 t} + \frac{1}{\lambda_m^2}(1-e^{\kappa\lambda_m^2 t}) \\ &\cdot\sum_{k=1}^{n}\Gamma_k\cdot\left(cos\frac{x_{k-1}}{L}m\pi - cos\frac{x_k}{L}m\pi\right)\end{aligned} \tag{8}$$

λ_m and $\psi_m(x)$ are eigenvalues and eigenfunctions which are the solutions of the Sturm-Liouville problem corresponding to the diffusion equation (5) and the boundary conditions.

With equation (6), given critical stress σ_{crit}, the nucleation time t_{nuc} can be obtained quickly by non-linear equation solving methods such as Newton's method or bisection method.

2) Growth phase modeling: After the void is nucleated, the growth phase starts. Early failure typically happens in a via-to-via structure as shown in Fig. 2(a). When the void forms in a via-above line and reaches *critical size* (ΔL_{crit}) [22], [23] which equals the via's diameter, the via is blocked by the void and thus the connection to the upper layer is also blocked (capping layer is fabricated with dielectrics such as Si_3N_4 which does not shunt current flow). In contrast, late failure occurs in a so-called via-below structure as shown in Fig. 2(b). When the void reaches *critical size*, current can still go through the barrier layer (barrier layer is fabricated with Ta whose resistivity is much higher than Cu) and the resistance will increase over time. Although sometimes early failure can happen in via-below structure and late failure can happen in via-up structure, the possibility is very low.

Void growth rate v_d is given by the mobility ($D_a/k_B T$) times the electromigration driving force F_e, then we have [22]

$$v_d = \frac{D_a}{k_B T}F_e = \frac{D_a}{k_B T}eZ\rho j \tag{9}$$

For early failure mode, the growth time can be expressed as:

$$t_{growth} = \frac{\Delta L_{crit}}{v_d} \tag{10}$$

For late failure mode, there will be no open circuit. When the resistance increases to the critical level, the interconnect wire will be considered to be failed. The growth time is:

$$t_{growth} = \frac{\Delta L_{crit}}{v_d} + \frac{\Delta r(t)}{v_d\left[\frac{\rho_{Ta}}{h_{Ta}(2H+W)} - \frac{\rho_{Cu}}{HW}\right]} \tag{11}$$

where ρ_{Ta} and ρ_{Cu} are the resistivity of tantalum (the barrier liner material) and copper, respectively, W is the line width, H is the copper thickness, and h_{Ta} is the liner layer thickness.

However, the void may saturate before reaching the *critical void length*. The saturation length is expressed in [14] as

$$L_{ss} = L_{line} \times \left[\frac{\sigma_T}{B} + \frac{eZ\rho jL}{2B\Omega} \right] \tag{12}$$

where L_{ss} is the void saturated length, $L_{line}$is the total length of the wire and σ_T is thermal stress. Void growth may stop before the calculated t_{growth} because the void is saturated. In this case, we can treat the wire as immortal or its lifetime is larger than the target lifetime.

III. PROPOSED EM-IMMORTALITY CONSTRAINED POWER SUPPLY OPTIMIZATION METHOD

In this section, we propose a programming-based power grid wire sizing optimization problem subjected to the voltage-based EM reliability constraints. We notice that the new EM constraint will ensure the wire EM immortal, so we call this method EM-immortal power supply optimization (we will discuss the EM mortal optimization later).

Before optimization, we first describe the modeling assumptions. Firstly, we focus on the DC problem, which means we are only interested in the resistance of the power grid networks. Secondly, the P/G network is composed of several orthogonal meshes of wires and contains multiple segments/branches. Thirdly, the wires are quite long, there must be some wiring resources (usually 10%) used for power distribution. Lastly, to simplify the problem, the circuits are modeled with shorted vias, that is, via resistance can be ignored.

A. Problem formulation

Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, ..., n\}$ and b branches $B = \{1, ..., b\}$. Each branch i connects two nodes i_1 and i_2 with current flowing from i_1 to i_2. l_i and w_i are the length and width of branch i, respectively. ρ is the sheet resistivity. The resistance of branch i is $r_i = \frac{V_{i_1} - V_{i_2}}{I_i} = \rho \frac{l_i}{w_i}$.

1) Objective function: The total routing area of a P/G network can be expressed in terms of voltages, currents and lengths of the branches:

$$f\left(V, I\right) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i1} - V_{i2}} \tag{13}$$

The objective function is linear for branch current variables I and nonlinear for nodal voltage variables V.

2) Constraints: The constraints that need to be satisfied for a reliably working P/G network are listed as follows.

a) Voltage IR drop constraints: To ensure proper logic operations, the IR drop from the P/G pads to the nodes should be restricted. For each node, we must specify a threshold voltage:

$$\begin{aligned} &V_j > V_{min} \text{ for power network} \\ &V_j < V_{max} \text{ for ground network} \end{aligned} \tag{14}$$

b) Minimum width constraints: The widths of the P/G segments are technologically limited to the minimum width allowed of the layer where the segment lies. Thus, we have

$$w_i = \rho \frac{l_i I_i}{V_{i1} - V_{i2}} \geq w_{i,min} \tag{15}$$

c) Electromigration constraints: As described before,for a multi-segment interconnect m, the EM constraint should be satisfied

$$V_{crit,EM} > V_{E,m} - V_{cat,m} \tag{16}$$

where $V_{E,m}$ is the *EM voltage* for the mth interconnect tree, computed using equation (1). $V_{cat,m}$ is the cathode nodal voltage of that tree. Different from the previous method, where all the branch currents are monitored (become constraints), in our new method, we only need to monitor the cathode node for an interconenct tree, which can lead to signficant reductions of constraints.

d) Equal width constraints: For typical chip layout designs, certain tree branches should have the same width. The constraint can be written as $w_i = w_k$ for branch i and k. In terms of nodal voltages and branch currents, we have

$$\frac{V_{i1} - V_{i2}}{l_i I_i} = \frac{V_{k1} - V_{k2}}{l_k I_k} \tag{17}$$

e) Kirchoff's current law (KCL): For each node j, we have

$$\sum_{k \in B(j)} I_k = 0 \tag{18}$$

where $B(j)$ is the set of branches incident on node j.

The P/G optimization aims to minimize the objective function (13) subjected to constraints (14)-(18). It will be referred as problem *P*. Problem *P* is a constrained nonlinear optimization problem.

B. Relaxed two-step sequence of linear programming solution

To solve the mentioned nonlinear optimization problem, we notice that the newly added EM constraint (16) is still linear in terms of nodal voltage. As a result, we can follow the relaxed two phases iterative optimization process [8], [10] and apply the sequence of linear programming technique [10] to solve the relaxed problem.

1) P-V optimization phase: In this phase, we assume that all branch currents are fixed, then the objective function can be rewritten as

$$f(V) = \sum_{i \in B} \frac{\alpha_i}{V_{i1} - V_{i2}} \tag{19}$$

where $\alpha_i = \rho I_i l_i^2$, subjected to constraints (14), (16) and (17). We further restrict the changes of nodal voltages such that their current directions do not change during the optimization process:

$$\frac{V_{i1} - V_{i2}}{I_i} \geq 0 \tag{20}$$

Problem *P-V* is nonlinear, however, it can be converted to a sequence of linear programming problem[10]. By taking the first-order Taylor's expansion of equation (19) around the initial solution V^0, the linearized objective function can be written as

$$g\left(V\right) = \sum_{i \in B} \frac{2\alpha_i}{V_{i1}^0 - V_{i2}^0} - \sum_{i \in B} \frac{\alpha_i}{\left(V_{i1}^0 - V_{i2}^0\right)^2} \left(V_{i1} - V_{i2}\right) \tag{21}$$

Here, an additional constraint should be added [10]

$$\xi I_i \left(V_{i1}^0 - V_{i2}^0\right) \leq I_i \left(V_{i1} - V_{i2}\right) \tag{22}$$

where $\xi \in (0, 1)$ is a restriction factor, which will be selected by some trials and experience.

2) P-I optimization phase: In this phase, we assume that all nodal voltages are fixed, so the objective function becomes

$$f(I) = \sum_{i \in B} \beta_i I_i \tag{23}$$

where $\beta_i = \frac{\rho l_i^2}{V_{i1} - V_{i2}}$, subjected to constraints (15), (17) and (18). Similarly, we restrict the changes of current directions during the optimization process:

$$\frac{I_i}{V_{i1} - V_{i2}} \geq 0 \tag{24}$$

Problem *P-I* is a linear programming problem.

C. New EM-immortality constrained P/G optimization

Solving problem *P* is to start with an initial feasible solution, then iteratively solve *P-V*, then *P-I*. The procedure for solving problem in *P-V* phase can be transformed to the problem of choosing ξ and solving a linear programming problem, and then repeating this process until the optimal solution is found. We summarize the entire EM-immortality constrained power supply network optimization procedure as Algorithm 1.

Algorithm 1 New EM-immortality-constrained P/G wire-sizing algorithm

```
Input: Spice netlist containing a P/G network.
Output: Optimized P/G network parameters.
/*Problem Setup*/
Compute the initial $V^k$, $I^k$ for $k = 0$.
while $\left| f\left(V^{k+1}, I^{k+1}\right) - f\left(V^k, I^k\right)\right| < \varepsilon$ do
    /*P-V Phase*/
    Construct constraints (15), (16), (17), (20) and (22) with $I^k$.
    Compute $V_l^k = \arg\min g\left(V^k\right)$ for $l = 0$ subjected to constraints (14), (15), (16), (17), (20) and (22).
    repeat
        Increase $\xi$.
        $l = l + 1$.
        Construct constraint (22) with $V_l^k$.
        Compute $V_l^k = \arg\min g\left(V^k\right)$.
    until $f\left(V_l^k\right) < f\left(V_{l-1}^k\right)$
    Let $V^{k+1} = V_l^k$.
    /*P-I Phase*/
    Construct constraints (15), (17) and (24) with $V^{k+1}$.
    Compute $I^{k+1} = \arg\min f\left(I^k\right)$ subjected to constraints (15), (17), (18), and (24).
    $k = k + 1$.
end while
Return $f(V, I)$.
```

IV. EM-LIFETIME CONSTRAINED POWER SUPPLY OPTIMIZATION

In the previous section, we discussed the power supply sizing optimization ensuring all the EM interconnect trees do not fail based on the voltage-based EM immortality check. However, such EM constraints may be conservative because some wires can have EM failures as long as the power grid networks can still work (its IR drop is still less than the given threshold) in the target lifetime (such as 10 years). In addition, the immortality requirement can be restrictive for some P/G network designs, making it impossible to find a feasible solution from Algorithm 1.

A. New EM-lifetime constrained optimization flow

In this section, we propose a new EM lifetime constrained P/G wire sizing optimization method in which some segments of the multi-segment interconnect wires will be allowed to fail or to age. The impact of these segments in terms of resistance change or even wire openings will be explicitly considered and modeled. Such aging-aware EM optimization essentially takes into account the EM aging-induced impacts or guard bands so that the designed P/G networks can work in the target lifetime.

The new optimization flow is shown in Fig. 3. In this new flow, we first check whether a given power supply network can be optimized using the EM-immortal P/G optimization given in Algorithm 1. If the optimization is unsuccessful, it means the EM condition may be over-constrained (perhaps this is due to the IR drop over the constraint, in this case, topology change will be required and it falls out of the scope of this paper).

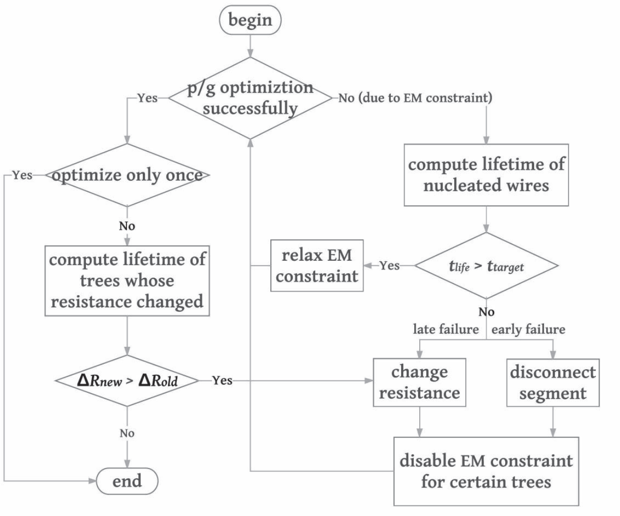


Fig. 3. Flowchart of the EM-lifetime constrained P/G optimization process.

We have several scenarios to discuss before we perform the optimization again. Let's define $t_{life,m}$ as the lifetime of the mth interconnect tree and t_{target} as the target lifetime.

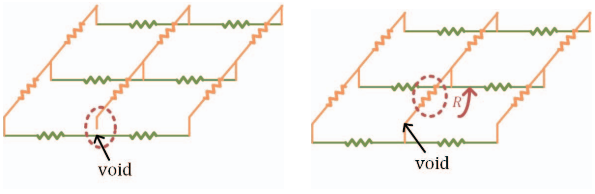
a) If $\boldsymbol{V_{E,m} - V_{cat,m} > V_{crit,EM}}$ *and* $\boldsymbol{t_{life,m} < t_{target}}$*:* The mth interconnect wire will be marked as a *failed wire* and its EM constraint will be disabled. If it is an early failure case, the cathode node of the wire segment connected by the failed via will be disconnected, which is called *wire disconnection*. The failure cases will depend on the current directions around the cathode node. If it is a late failure case, the wire segment associated with the cathode node will have a *resistance change*.

b) If $\boldsymbol{V_{E,m} - V_{cat,m} > V_{crit,EM}}$ *and* $\boldsymbol{t_{life,m} > t_{target}}$*:* The lifetime of interconnect wire still meets the target lifetime even though it will have void nucleation and resistance change. In this case, we use the existing $V_{E,m} - V_{cat,m}$ value as the new EM constraint (defined as $V_{E,m,prev} - V_{cat,m,prev}$) for this wire only: $V_{E,m} - V_{cat,m} < V_{E,m,prev} - V_{cat,m,prev}$. This is called *constraint relaxation*. The rationale behind this is that we hope the EM status of this wire becomes worse during the next round of optimization soo its lifetime will not change too much and still meet the given lifetime after the follow-up optimizations.

After the wire segment *resistance change*, or *wire disconnection*, or *constraint relaxation*, a new round of SLP programming optimization similar to Algorithm 1 is performed.

When the P/G optimization is successfully finished, it is necessary to check to see whether all the wires, especially those marked as failed, meet their failure conditions. For instance, if a failed wire (its failed segment) has 20% resistance change at the targeted 10-year lifetime before the optimization, however, after the optimization, it has 30% resistance change at 10 years, then the final IR drop condition may be not satisfied at 10 years. As a result, more iterations need to be carried out until such process is converged.

Another way to avoid such iteration is to set up some guard bands. Specifically, we can increase the target lifetime from 10 years to 15 years when computing the resistance changes for the failed wires. After optimization, we check whether all the failure conditions are satisfied against the real 10-year target. In this way, we may just need



(a) (b)

Fig. 4. The electrical impact of different failure mechanisms on the interconnect wires: (a) early failure mode; (b) late failure mode.

one iteration at the cost of more routing area used for the power supply networks.

B. Lifetime and resistance change analysis for a multi-segment interconnect wire

One important aspect of the proposed lifetime constrained power supply network optimization is to calculate the lifetime of a given mortal wire and its segment resistance change.

For those mortal wires, we start with time $t = 1000$ years and use bisection method to find t_{nuc}. The transient hydrostatic stress will be computed by equation (6) at the given time. Once the stress of one segment hits the critical stress, the wire is deemed as nucleated.

To determined the failure mode of the wire, we need to look at the current direction in the cathode node based on the patterns in Fig. 2(a) and 2(b) .

a) If the wire is void growth phase immortal: that is, the void growth saturation length is less than the critical length (described in Section II-B2). Then $t_{life} = \infty$ and its resistance remains unchanged.

b) If the wire is in early failure mode: we can simply use equation (10) to compute t_{growth}. In this case, the whole interconnect tree will be disconnected with another interconnect wire (connected by the failed via) as shown in Fig.4(a), thus $\Delta R = \infty$.

c) If the wire is in late failure mode: we have another solution. As shown in Fig. 4(b), t_{growth} will be computed using equation (11), assuming $\Delta R = 10\% R$. If t_{life} is greater than the target lifetime t_{target} (10 years), then we use the calculated t_{life} and $\Delta R = 10\% R$. Otherwise, t_{life} is set to t_{target} and we recalculate ΔR at the target lifetime.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. Experimental setup

Proposed EM-lifetime constrained power grid optimization is implemented in C/C++. Both IBM power grid networks [24] and self-generated networks are tested for our work. In the IBM power grid benchmarks, there are power networks and ground networks. Only power networks are used to test our method and their current source values are scaled to make sure that the initial voltage drop for each node is small enough. Our optimizer can work for both power and ground networks. The maximum allowable IR drop is set to $10\% V_{dd}$ and the minimum allowable width is set to $0.1\mu m$. The important parameters used in the optimization process are listed in Table I.

TABLE I
PARAMETERS USED IN THE OPTIMIZATION PROCESS

parameter	value	parameter	value
σ_{crit}	500MPa	Ω	$1.182 \times 10^{-29}\mathrm{m}^3$
V_{crit}	3.69×10^{-3}V	E_a	0.8eV
T	373K	D_0	$5.55 \times 10^{-8}\mathrm{m}^2/\mathrm{s}$
B	140GPa	ρ_{Cu}	$1.9 \times 10^{-8}\Omega \cdot \mathrm{m}$
Z	10	ρ_{Ta}	$1.35 \times 10^{-7}\Omega \cdot \mathrm{m}$

B. Experimental results and discussion

1) EM-immortality constrained P/G optimization: Table II compares the results of the new optimization method using immortal EM constraint with the existing P/G optimization method that uses current density as the only EM constraint [10]. In the proposed method, we assume all the branches have the same width in one tree, but different trees can have different widths. For fair comparison, we only allow the difference in EM constraints.

As we can see, for *ibmpg2*, which has 61797 nodes, 120 voltage sources and 18963 current sources, the original area is 60.38mm^2, after 2 iterations, the area can be reduced to 13.55mm^2, a 77.55% reduction. We stress that the area reduction depends on the initial P/G design and many other factors. However, the proposed method can indeed find a better or even optimal trade-off between area and IR drop and EM constraints. Although the previous work [10] has about 91.35% reduction, our detailed analysis shows that many mortal wires exist. For instance, ibmpg2-ibmpg4 have wires with a lifetime of less than 10 years, which obviously violates the EM constraint. In contrast, the new work will ensure that all the wires will not fail. Essentially, the current based EM optimization trade lifetime for better area reduction. For other cases, we see a similar pattern: the new method typically leads to less area reduction compared to the current density based method, but most of the resulting networks from the latter method have many mortal wires.

2) EM-lifetime constrained P/G optimization: Table III shows the lifetime-constrained P/G optimization of our self-generated P/G networks. In this table, column 3 is the number of nucleated trees (# nucleated wires) that stall the optimization process. Note that nucleated wires can be failed wires or potential failed wires whose final lifetimes may be longer than the target lifetime even though their $V_E - V_{cathode}$ are larger than the critical voltage. The number of iterations (# iter) in column 7 represents the whole optimization operation number which is different from that in Table II. If we have to relax the EM constraint, then the maximum V_{crit} will be presented in column 6 as $V_{crit,max}$, meanwhile, the shortest lifetime after optimization is presented in column 5 as $t_{life,min}$.

From Table III, we can see if there is no violation in the initial P/G networks, the optimization can be easily carried on. Sometimes, even with some violations, after a few *P-V* and *P-I* iterations, the violations can be eliminated and we can still obtain an EM immortal solution. Note that the area improvement strongly depends on the original layout, thus the absolute value of reduced area is not that important. There are several nucleated wires in each case, which means we need make some changes on these wires during the optimization process. For *pg30×50*, before optimization, the shortest lifetime $t_{life,min}$ is 5.53 years, which violates the lifetime constraint. After optimization, the lifetime is increased to 19.88 years. For other cases, even though they have a few nucleated wires, their lifetime may be very long. After optimization, this is still the case. In most situations, if $V_E - V_i \gg V_{crit}$ is in the initial condition, it is difficult to optimize successfully for the first time. With our lifetime-constrained optimization flow, the optimization results can always be achieved after several iterations so the lifetime targeted can be met.

VI. CONCLUSION

In this paper, we presented a new P/G network sizing technique based on the recently proposed voltage-based EM immortality check method for general multi-segment interconnect wires and physics-based EM assessment technique for fast time to failure analysis. We first showed that the new P/G optimization problem with voltage IR drop and the new EM constraint can still be formulated as an efficient

TABLE II
IMMORTALITY-CONSTRAINED P/G OPTIMIZATION RESULTS FOR IBM P/G NETWORKS

ckt	# node	# bch	# tree	max # tree bch	area (mm^2)	voltage-based EM constraint		current density EM constraint		
						# iter	area reduced (%)	# iter	area reduced (%)	$t_{life,min}$ (yrs)
ibmpg1	11572	5580	689	30	158.43	2	35.66	2	72.29	13.57
ibmpg2	61797	61143	462	192	60.38	2	77.55	2	91.35	8.16
ibmpg3	407279	399201	7388	965	697.71	2	22.60	2	57.98	9.64
ibmpg4	474836	384709	9358	571	210.44	2	18.42	2	29.70	7.61

TABLE III
LIFETIME-CONSTRAINED P/G OPTIMIZATION RESULTS FOR SELF-GENERATED P/G NETWORKS

ckt	# tree	# nucleated wires	before optimization	after optimization		# iter	area reduced (%)
			$t_{life,min}$ (yrs)	$t_{life,min}$ (yrs)	$V_{crit,max}$ (V)		
pg5×10	15	1	-	immortal	-	1	76.51
pg10×10	20	5	80.68	77.39	4.307×10^{-3}	2	38.29
pg30×50	80	11	5.53	19.88	5.61×10^{-2}	5	26.68
pg20×100	120	8	> 100	> 100	7.22×10^{-2}	3	46.62

SLP problem. The new optimization will ensure that all the wires will not fail if all the constraints are met. To further consider EM-induced aging effects on power supply networks for the target lifetime and mitigate the over-conservation of the first optimization formulation, we proposed a second P/G optimization method that can allow some short lifetime wires to fail and optimize the remaining wires in the presence of the wire resistance increase of the failed wire segments. In this way, the P/G networks can be optimized so that the lifetime of the entire power grids can be used as constraints, and the resulting P/G networks will become more robust and aging-aware over the expected lifetime of chips. Numerical results of a number of IBM and self-generated power supply networks showed that the new method can effectively reduce the area of the P/G networks while ensuring reliability in terms of immortality or target lifetime, which is not the case with the existing current density constrained P/G optimization methods.

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