Performance Bound and Yield Analysis for Analog Circuits under Process Variations

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***Abstract*—Yield estimation for analog integrated circuits are crucial for analog circuit design and optimization in the presence of process variations. In this paper, we present a novel analog yield estimation method based on performance bound analysis technique in frequency domain. The new method first derives the transfer functions of linear (or linearized) analog circuits via a graph-based symbolic analysis method. Then frequency response bounds of the transfer functions in terms of magnitude and phase are obtained by a nonlinear constrained optimization technique. To predict yield rate, bound information are employed to calculate Gaussian distribution functions. Experimental results show that the new method can achieve similar accuracy while delivers 20 times speedup over Monte Carlo simulation of HSPICE on some typical analog circuits.**

1. Introduction

At the nano-scale, circuit parameters are no longer truly deterministic and most of the quantities of practical interests present themselves as probability distributions. Circuit designers must now contend with these variations and uncertainties to ensure the robustness of their circuit designs. Traditional corner-based verification can't meet the accuracy requirements. For statistical analysis of digital and analog integrated circuits under process variations, Monte-Carlo (MC) based statistical simulation and yield estimation methods are the most popular methods due to their advantage of generality and high accuracy [1], [2]. However, simple MC method is expensive and slow and their inefficiency will lead to the bottleneck of analog circuit optimization. Many fast Monte Carlo methods have been proposed to improve the efficiency of classical Monte Carlo methods. Existing approaches include importance sampling [3], Latin hypercube sampling based method [4], [5], and quasi Monte Carlo based method [2], [6]. However, the importance sampling method is circuit specific, Latin hypercube sampling does not work for all the circuits, and quasi Monte Carlo method suffers the high-dimensional problems [5].

On the other hand, some efforts have been made using non Monte Carlo methods for statistical analysis. Among them, performance bound analysis methods emerged as attractive techniques for statistical analysis and yield estimation. Bounding or worse case analysis of analog circuits under parameter variations has been studied in the past for fault-driven testing and tolerance analysis of analog circuits [7]–[9]. Recently, some frequency domain performance bound methods were proposed in [10]–[12] to compute the lower and upper bounds of transfer function's magnitude and phase. The work in [10] applied a control-based method [13] to obtain the performance bounds in frequency domain, and [11] applied an optimization based method to compute the bounds. However, no systematic method was proposed to obtain variational performance objective functions. This method has been improved by [12] where symbolic analysis approach was applied to derive exact transfer functions and affine interval method was used to compute variational transfer functions. However, the affine interval method can lead to over conservative results.

In this paper, we present a novel non Monte-Carlo yield estimation method based on performance bound analysis technique in frequency domain. The new method first derives the exact transfer functions of linear (linearized) analog circuits via a graph-based symbolic analysis method. Then frequency response bounds of the transfer functions in terms of magnitude and phase are obtained by a nonlinear constrained optimization technique. Since the symbolic expression of the transfer function is available, the optimization can be run on different frequency points independently, and when implemented in parallel, a further speedup can be expected. The most important virtue of the optimization based searching method is that it ensures the more accurate bounds for transfer functions and also resolves the device correlation issues seen in the previous methods. The proposed method can be easily extended to the time domain bound and yield estimation and even for nonlinear circuits. Experimental results show that the new evaluation algorithm can achieve about one to two order of magnitudes speedup over Monte Carlo simulation of HSPICE on benchmark analog circuits.

This paper is organized as follows. We present the new frequency domain bound computation method using nonlinear constrained optimization in Section 2. The yield estimation based on the performance bounds is discussed in Section 3. The effectiveness and accuracy of proposed flow are demonstrated by several numerical examples in Section 4. Last, Section 5 concludes the paper.

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2. Computation of frequency domain bounds

In this section, we first review a graph-based symbolic analysis for obtaining the exact symbolic transfer functions of analog circuits. This step is basis for our newly proposed method.

A. Review of Symbolic Analysis for Analog Circuits

Graph-based symbolic technique is a viable tool for calculating the behavior or characteristic of analog circuits [14]. The introduction of determinant decision diagrams based symbolic analysis technique (DDD) allows exact symbolic analysis of much larger analog circuits than all the other existing approaches [15], [16]. Furthermore, with hierarchical symbolic representations [17], exact symbolic analysis via DDD graphs essentially allows the analysis of arbitrary large analog circuits.

To obtain the transfer function $H(s)$, we can build the s-expanded DDD [16] and use it to generate the symbolic transfer function as follows:

$$H(s, p_1, \ldots, p_m) = \frac{\sum_{i=0}^{m} a_i(p_1, \ldots, p_m) s^i}{\sum_{j=0}^{n} b_j(p_1, \ldots, p_m) s^j} \tag{1}$$

where coefficients $a_i(p_1, \ldots, p_m)$ and $b_j(p_1, \ldots, p_m)$ are represented by each root in s-expanded DDD graphs and $p_1, \ldots, p_m$ are m circuit variables. Notice that $H(s, p_1, \ldots, p_m)$ describes nonlinear functions of $p_1, \ldots, p_m$.

Once the small-signal characteristics of circuits are presented by DDDs, evaluation of DDDs, whose CPU time is proportional to the size of DDDs, will give exact numerical values.

B. Variational bound analysis

The evaluation of the transfer function gives a complex valued result, $H(j\omega) = H(\omega)e^{j\theta(\omega)}$, where the magnitude $H(\omega) = |H(j\omega)|$ and the phase angle $\theta(\omega) = \angle H(j\omega)$ are real values. Our first goal here is to calculate the bounds of magnitude and phase of $H(j\omega) = H(\omega)e^{j\theta(\omega)}$ considering the variations, i.e.,

$$H_l(\omega) \le H(\omega) \le H_u(\omega) \tag{2}$$

$$\theta_l(\omega) \le \theta(\omega) \le \theta_u(\omega). \tag{3}$$

To find the bounds, we formulate the bound computing problem into a nonlinear constrained optimization problem. To obtain the two performance bounds for magnitude or phase at one frequency point, two evaluation processes, or optimization runs, of the transfer function are needed: one for $H(\omega)$, and the other for $\theta(\omega)$. The designer determines the range of frequency sweep and number of frequency points freely. We use the lower bound of the magnitude response $|H(j\omega)|$ at frequency ω for an example. The magnitude of the transfer function, which can be evaluated from the available symbolic transfer function, is used as the nonlinear objective function to be minimized:

$$\begin{array}{ll} \text{minimize} & |(H(j\omega, \mathbf{x})| \\ \text{subject to} & \mathbf{x}_{\text{lower}} \le \mathbf{x} \le \mathbf{x}_{\text{upper}}, \end{array} \tag{4}$$

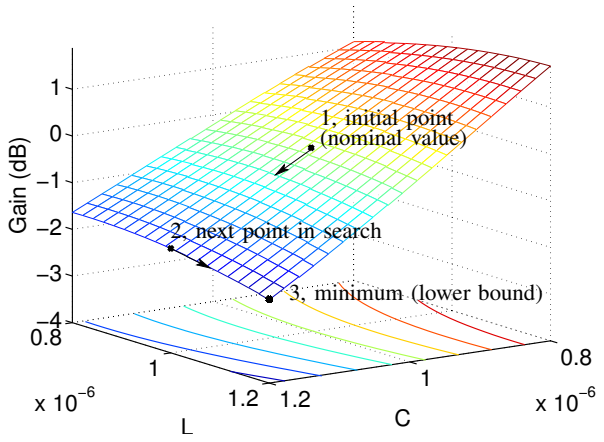


Fig. 1. Optimization space searching for a RLC circuit, where both C and L have 20% variation in this illustration. This surface shows the magnitude variations at frequency $f = 10^6$ Hz.

where $\mathbf{x} = [p_1, \ldots, p_m]$ represents the circuit parameter variable vector, which is subjected to the optimization constraints $[\mathbf{x}_{\text{lower}}, \mathbf{x}_{\text{upper}}]$. In circuit design, foundries and cell library vendors supply these constraints. Hence, after (4) is solved by an optimization engine, the lower bound of the magnitude response at ω, i.e., $|H_l(j\omega)|$, is returned and a parameter set at which the minimum is attained will also be saved as a by-product. The iterative search procedure in the constrained minimization is illustrated in Fig. 1.

The nonlinear optimization problem with simple upper and lower bounds given in (4) can be efficiently solved by several methods such as active-set, interior-point, and trust-region algorithms [18]–[20]. All those methods are iterative approaches starting with an initial feasible solution. In this work, we use the active-set method [20], as it turns to be the most robust nonlinear optimization method for our application. Active-set method is a two-phase iterative method that provides an estimate of the active set (which is the set of constraints that are satisfied with equality) at the solution. In the first phase, the objective is ignored while a feasible point is found for the constraints. In the second phase, the objective is minimized while feasibility is maintained. In this phase, starting from the feasible initial point $\mathbf{x}_0$, the method computes a sequence of feasible iterates $\{\mathbf{x}_k\}$ such that $\mathbf{x}_{k+1} = \mathbf{x}_k + \alpha_k \mathbf{d}_k$ and $H(\mathbf{x}_{k+1}) \le H(\mathbf{x}_k)$ via methods like quadratic programming, where $\mathbf{d}_k$ is a nonzero search direction and α_k is a non-negative step length.

Since the responses at two neighboring frequency points are usually close to each other, the starting point $\mathbf{x}$ for frequency point ω_{i+1} can be set using the solution at the previous frequency point ω_i. This strategy tends to reduce the time required by the optimization to search its minimal or maximal point in the whole variable space, and thus speedup the calculation time of the bound analysis. However, it is not trivial to note that since different frequencies' response can be computed independently and in parallel, the parallel

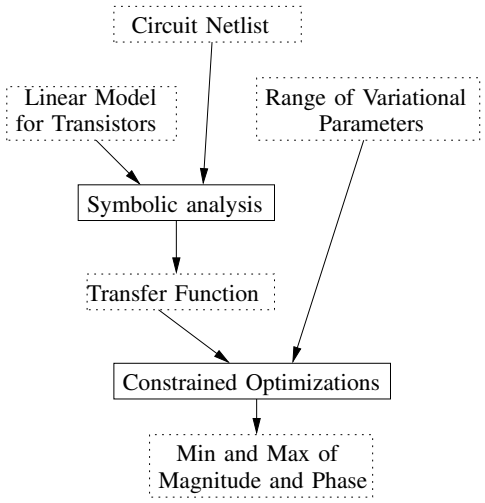


Fig. 2. The flowchart of frequency domain performance bound calculation.

Algorithm 1 Calculation of frequency response bounds via symbolic analysis and constrained optimization

1: Read circuit netlist.
2: Set bounds on process variation affected parameters.
3: Generate symbolic expression of transfer functions.
4: **for** each ω_i **do**
5: Run nonlinear constrained optimization (4) which uses transfer function as objective to find magnitude and phase bounds on ω_i.
6: **end for**
7: Save bound information for future statistical and yield analysis.

acceleration power would possibly make the aforementioned starting point strategy less useful. We plan as our future work to implement the optimization on different frequency points in parallel. Fig. 2 summarizes the flow of the performance bound calculation.

3. Yield estimation based on frequency domain bounds

In nanometer level of VLSI technology, designer shall not stop at making the circuits to meet a specification target. It is also critical to accurately predict the behavior of the circuits under a range of expected and unexpected conditions, including the process variations among the components. Yield analysis helps designers get an insight into the important statistical features [21]–[23]. In this section, we present a circuit yield analysis based on the performance bounds we derived earlier in this work.

A. Calculation of mean and standard deviation

The characteristic parameters of Gaussian distribution are its mean μ and standard deviation σ. In the variation aware circuit analysis, the mean value is usually its nominal performance metrics, while the deviation needs to be estimated by statistical

Algorithm 2 Yield estimation based on frequency response bounds

1: Apply Algorithm 1 on the circuit and obtain the magnitude and phase bounds.
2: At the interested frequencies, the nominal response from the DDD evaluation will be the mean μ in yield estimation, while the lower and upper bounds, together with the calibration ratio r, are used to estimate standard deviation σ_{ω_i}:
$$\sigma_{\omega_i} = (u_{\omega_i} - l_{\omega_i})/r.$$
3: The estimated distribution is characterized by μ and σ.

method. Since our proposed method calculates accurately the bounds of the variational transfer function, the estimation of σ does not pose additional burdens. We first derive the bounds of magnitude and phase using $\pm 3\sigma$ intervals for all circuit parameters as the input of the bound analysis in Section 2. The selection of 3-sigma here is because 99.7% coverage of the distribution space is attained within $\pm 3\sigma$, and no overestimation of the magnitude or phase bounds is incurred.

Now we show the estimation of the standard deviation of response magnitude at different frequencies using the bounds. Since the variational transfer function is a general nonlinear function of random variables, we cannot get the analytical result of its deviation even if we know the distribution of the input random variables and the expression of transfer function. In other words, the distance between the lower bound and the upper bound does not tell how many sigma's are included, and thus this ratio must be estimated. To calculate this ratio, we use Monte Carlo on one single frequency ω_i, and get the standard deviation $\sigma_{\omega_i,\mathrm{MC}}$ from the samples. Meanwhile, the bound analysis on frequency ω_i gives l_{ω_i} and u_{ω_i}. We define the ratio as $r = (u_{\omega_i} - l_{\omega_i})/\sigma_{\omega_i,\mathrm{MC}}$. Experiments verified that if this ratio is calibrated on one frequency, it is also accurate on other frequencies for the same transfer function and random variable settings. Hence, we only do Monte Carlo on one frequency, but we can get accurate estimation of the distribution on all frequency range using bound analysis. Also we observed that the ratio typically $r \geq 6$ for using 3-sigma circuit parameter variations.

B. Yield estimation

Yield rate is the proportion of circuits on the wafer found to perform properly. Although the successful circuits have to meet several specifications, we just use some simple rules for the demonstration here. For example, frequency response specifications, such as open-loop gain of an op-amp or attenuation ratio of an active filter, can be enumerated for our yield estimation. Those outliers of op-amps and filters, whose gain or attenuation levels exceed the specification interval are counted as failed circuits. Fig. 4 represents the scheme of yield estimation using the two Gaussian statistics, i.e., mean and standard deviation, both obtained from our bound analysis. The number of successful circuits, as denoted by the shaded

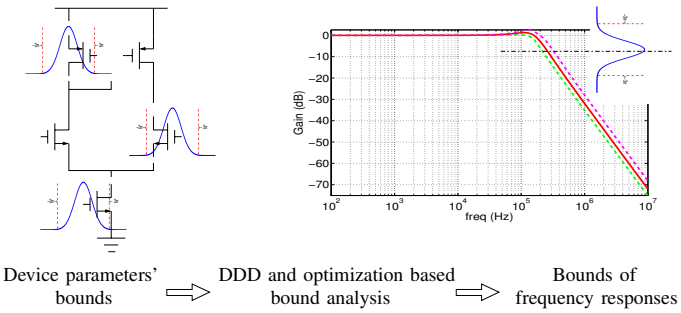


Fig. 3. The calculation of yield bounds of frequency response using device parameter bounds.

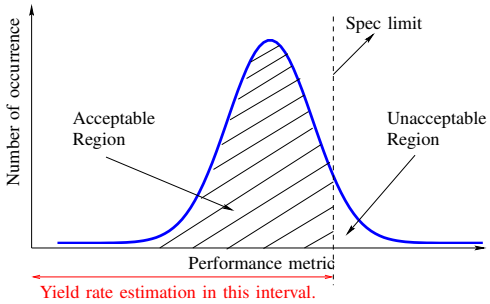


Fig. 4. Yield estimation using estimated mean and standard deviation from bound analysis.

area, is the part of the whole distribution within the preset specification limit.

Using the mean and standard deviation calculated from the bound analysis, the Gaussian distribution of the transfer function can be characterized by probability density function (PDF) and cumulative distribution function (CDF). Hence, the yield rate p is the fraction of the distribution which are within the performance specification,

$$\begin{aligned} p &= \mathrm{normcdf}(Y_{\mathrm{u,spec}}, \mu, \sigma) - \mathrm{normcdf}(Y_{\mathrm{l,spec}}, \mu, \sigma) \\ &= \frac{1}{\sigma\sqrt{2\pi}} \int_{Y_{\mathrm{l,spec}}}^{Y_{\mathrm{u,spec}}} e^{-\frac{(t-\mu)^2}{2\sigma^2}} \mathrm{d}t, \end{aligned} \tag{5}$$

where $Y_{\mathrm{l,spec}}$ and $Y_{\mathrm{u,spec}}$ are specification limits set by designers. Therefore, with a integration of the Gaussian probability density function in the successful interval, the yield rate in Eq. (5) is calculated. Most numerical computation tools provide ready-to-use functions for Gaussian PDF and CDF [24], [25]. The procedure for yield prediction is listed in Algorithm 2.

4. Experimental results

In this section, we show experimental results of the proposed method on several industrial benchmark circuit netlists. The DDD symbolic tool generates the exact transfer function expressions first [15], and all the follow-up optimization based bound calculation and yield estimation are done in MATLAB. The nonlinear constrained optimizations are solved by the *fmincon* function in MATLAB's Optimization Toolbox [26].

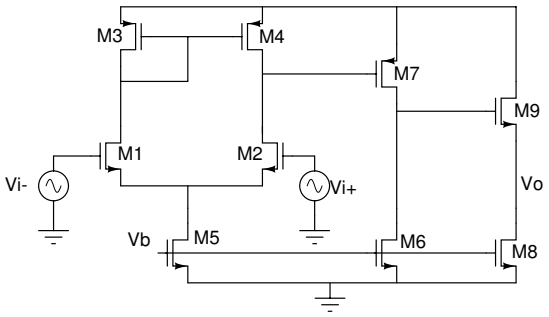


Fig. 5. The circuit schematic of CMOS operational amplifier.

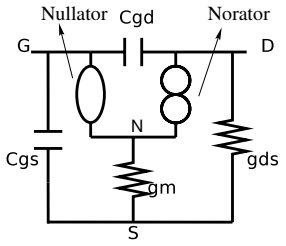
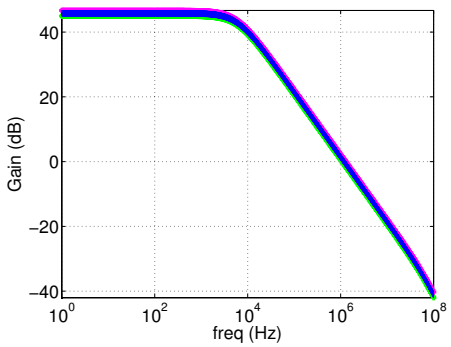


Fig. 6. The small-signal model for MOS transistor.

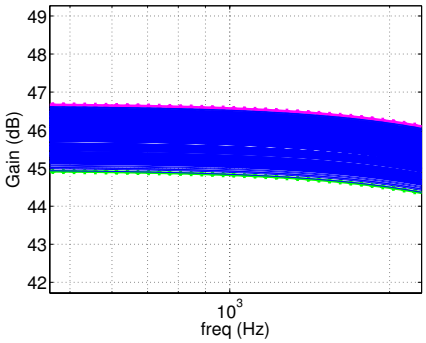
All running time are sampled from a Linux server with a 2.4 GHz Intel Xeon Quad-Core CPU, and 36 GBytes memory.

For running time comparisons, we also measure the time cost by the commercial HSPICE, which runs all the Monte Carlo simulations. While we note that some industrial Monte Carlo tools can run simulations in parallel, the experiments in this work still use serial HSPICE Monte Carlo for comparison. This is because we focus on the demonstration of the accuracy and effectiveness of our non Monte Carlo method. Future comparison with parallel Monte Carlo can be done when we fully implement our method in C and carry out the nonlinear optimization in parallel.

Now let us investigate the accuracy and efficiency of our method with typical circuit examples in detail. Fig. 5 shows the schematic of a CMOS operational amplifier circuit, which contains 9 transistors. Its differential inputs are provided at the gate terminals of the differential pair (M1 and M2), while the output is observed at the output node of the source follower stage. In our method, DC analysis is first performed by SPICE to obtain the operation point, and then small-signal models of nonlinear devices, such as MOS transistors, are used for DDD symbolic analysis and transfer function evaluation. For example, the original NMOS device is replaced by the equivalent circuit model consisted of voltage controlled current source (VCCS), gate-source capacitance (C_{GS}), gate-drain capacitance (C_{GD}), terminal resistance, and so on, as shown in Fig. 6. In this MOS small signal model, we use nullor elements, i.e. nurator an nullator elements. The combination of these elements as seen in the MOS model behaves as a VCCS. Since the nullator doesn't allow current through it and the voltages on its terminals are the same, the voltage on node G is equal to the voltage on node N and the current generated



(a) Monte Carlo simulations and magnitude bounds of op-amp circuit.



(b) Detailed view around 10^3 Hz.

Fig. 7. Monte Carlo simulations and magnitude bounds of op-amp circuit. The thick dashed lines are lower and upper bounds, and the thin solid lines are Monte Carlo results.

by the transistor flows only through the resistor gm and the norator as it allows any voltage and any current through it [27].

After the symbolic expressions, i.e., numerator and denominator, of the op-amp's transfer function is obtained, its nominal frequency response can be evaluated straightforward using the specified parameter values. The lower and upper bounds of the magnitude and phase are then obtained by the aforementioned nonlinear constrained optimization. Fig. 7 plots the nominal magnitude curve along with its lower and upper bounds. On the same figure, we also plot the Monte Carlo samples of the same circuits. It is obvious that our bounds include all possible variations, and do not show much over-conservativeness. The reason of its accuracy is because the optimization based method explores the entire uncertainty region, i.e., the multi-dimensional space represented by the device parameter intervals, $[\mathbf{x}_{\text{lower}}, \mathbf{x}_{\text{upper}}]$, and returns the bounds where the transfer function reaches its extremes.

For the same op-amp, yield estimation is calculated using preset specification. One important specification of op-amp is open-loop gain at a relatively low frequency. For the CMOS op-amp in Fig. 5, we set a requirement that the accepted

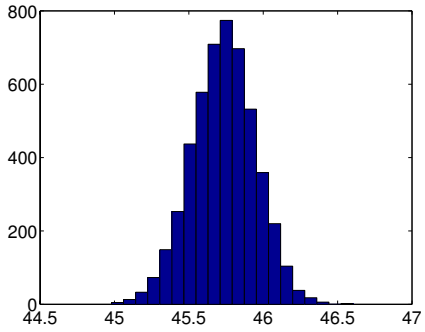


Fig. 8. The histogram of gain distribution of the CMOS op-amp at frequency $f = 1$ kHz. (5000 times Monte Carlo simulation.)

TABLE I
STATISTICAL INFORMATION OF THE CMOS OP-AMP CIRCUIT. (COMPARISON WITH 5000 TIMES MONTE CARLO.)

CMOS op-amp		
Runtime (seconds)	MC	85.2
	proposed	3.8
Mean value (μ) Unit: dB	MC	45.8
	proposed	45.8
Std. value (σ) Unit: dB	MC	0.214
	proposed	0.214
Yield rate	MC	98.8%
	proposed	98.4%

circuits should have gain larger than 45 dB at frequency $f = 1$ kHz. HSPICE Monte Carlo analysis gives the yield as 98.8%, and the histogram of all samples is drawn in Fig. 8. Meanwhile, the predicted yield using the proposed method is 98.4%, which is fairly close to that of the MC analysis. The detailed statistics of the comparison are shown in Table I.

With the accurate calculation of performance bounds and the yield, the presented method only takes 3.8 seconds. This is a 22× speedup over Monte Carlo method.

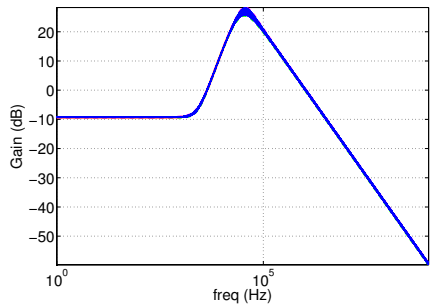
The proposed algorithm is also applied to a CMOS active filter [28] (circuit diagram not shown in this paper). Fig. 9 shows the magnitude bounds together with HSPICE Monte Carlo results. The statistical data is listed in Table II. A speedup of 13× is observed on this example.

5. Conclusion

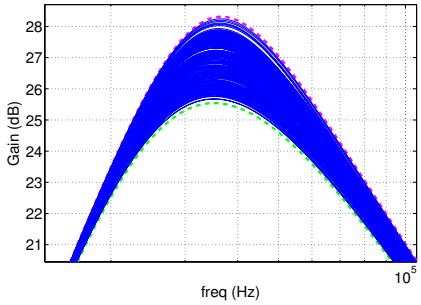
In this paper, we have proposed a novel frequency domain performance bound and yield estimation for analog integrated

TABLE II
STATISTICAL INFORMATION OF THE CMOS FILTER. (COMPARISON WITH 5000 TIMES MONTE CARLO.)

CMOS Filter		
Runtime (seconds)	MC	100.4
	proposed	8.2
Mean value (μ) Unit: dB	MC	26.83
	proposed	26.81
Std. value (σ) Unit: dB	MC	0.389
	proposed	0.384
Yield rate	MC	82.7%
	proposed	84.2%



(a) Monte Carlo simulations and magnitude bounds of active filter.



(b) Detailed view around 10^3 Hz.

Fig. 9. Monte Carlo simulations and magnitude bounds of active filter. The thick dashed lines are lower and upper bounds, and the thin solid lines are Monte Carlo results.

circuits under process variations. The new method generates circuit transfer functions using the graph-based symbolic analysis techniques. To evaluate the performance bounds, the transfer function is used as objective function in a nonlinear constrained optimization where the optimization variables are variational circuit parameters. With the bound information available, we then estimate the yield based on preset specifications. Experimental results show that the new method can achieve similar accuracy while delivers 20 times speedup over Monte Carlo simulation of HSPICE on some typical analog circuits.

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