

Efficient Power Grid Integrity Analysis Using On-the-Fly Error Check and Reduction *

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ABSTRACT

In this paper, we present a new voltage IR drop analysis approach for large on-chip power delivery networks. The new approach is based on recently proposed sampling based reduction technique to reduce the circuit matrices before the simulation. Due to the disruptive nature of tap current waveforms in typical industry power grid networks, input current sources typically has wide frequency power spectrum. To avoid the excessively sampling, the new approach introduces an error check mechanism and on-the-fly error reduction scheme during the simulation of the reduced circuits to improve the accuracy of estimating the the large IR drops. The proposed method presents a new way to combine model order reduction and simulation to achieve the overall efficiency of simulation. The new method can also easily trade errors for speed for different applications. Experimental results show the proposed IR drop analysis method can significantly reduce the errors of the existing ETBR method at the similar computing cost, while it can have 10X and more speedup over the the commercial power grid simulator in UltraSim with about 1-2% errors on a number of real industry benchmark circuits.

1. INTRODUCTION

Reliable on-chip power delivery is one of the difficult challenges for sub-100nm and below VLSI technology as voltage IR drops become more and more pronounced. This situation gets worse as technology continues to scale down. This has been reflected by the facts that more power has to be delivered into the chips for more packed devices, and supply voltage continues to decrease, which results in a decreased noise margin for signal transition, and makes transistor more vulnerable to supply voltage degradation. So efficient verification of power integrity becomes critical for final design power integrity closure.

Many research works have been done on efficient simulation of on-chip power grid networks. Methods such as multigrid-like [1, 2], hierarchical [3, 4], partition-based [5], fast iterative [6, 7] and random walk based [8] help improve scalability of power grid network analysis.

Recently simulation approaches based on frequency-domain reduction have been proposed [9, 4, 10]. These methods boost the efficiency by reducing the original circuits before the transition analysis on the reduced circuits. The reduction is performed on both a power grid system and its input signal sources. Existing approaches consists of the extended Krylov subspace based reduction methods (EKS) [9, 4] and the extended truncated balanced realization based method (ETBR) [10]. The EKS method is based on the moment matching scheme. It needs to present the current sources in the explicit moment forms, which may lead to less accuracy owing to

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the well-known numerical problems in explicit moment matching methods [11]. The ETBR method performs the response sampling over wide frequency range to build the reduced model and was shown to be more accurate than EKS [10]. However, how to select the sampling points to minimize the errors of reduced models still remains an open problem. This is especially the case for real industry power delivery networks where current waveforms are very disruptive and their frequency power spectrum is significant in wide frequency range, which may require a large number of samplings to meet the accuracy requirement. Also the simulation time period is typically very long (compared with the number of simulation steps) in those industry circuits.

In this paper, we propose efficient IR drop analysis approach based on the sampling-based reduction and simulation framework. The new approach tries to dynamically compensate error losses from the reduction during the simulation process of reduced models. The new approach introduces an error check mechanism based on the system residuals, which is an exact error indicator, as well as the novel effective resistance concept to compute the errors in terms of more useful voltage drop values. The on-the-fly error reduction works well for compensating high frequency accuracy loss related to disruptive tap current waveforms in typical industry power grid networks. The new method also presents a new way to closely combine model order reduction and simulation to achieve the overall efficiency of simulation. The proposed method provide an efficient way to easily trade errors for speedup to suit different applications. Experimental results show the proposed IR drop analysis method can significantly reduce the errors of the existing ETBR method, and meanwhile it can lead to up 10X speedup over the the latest commercial power grid simulator, UPS, in UltraSim, with about 1-2% errors on a number of real industry circuits.

The rest of this paper is organized as follows: Section 2 presents the power grid models used in the paper and IR drop analysis problem. We review the extended balanced truncation reduction methods in Section 3. Section 4 presents the new reduction based IR-drop analysis method. Section 5 presents the experimental results and Section 7 concludes this paper.

2. POWER GRID NETWORK MODELS AND IR DROP ANALYSIS PROBLEM

The power grid networks in this paper are modeled as RC networks with known time-variant tap current sources, which can be obtained by gate level logic simulations of the circuits under assumption that transistor circuit simulation and power grid network simulation are separated. Such RC model is still valid at least for the on-chip level power grid networks for current technologies [12].

Fig. 1 shows the power grid models used in this paper. For a power grid, some nodes having known voltage are modeled as constant voltage sources. For C4 power grids, the known voltage nodes can be internal nodes inside the power grid. Given the tap current source vector, $u(t)$, the node voltages can be obtained by solving the following differential equations, which is formulated using

modified nodal analysis (MNA) approach,

$$\begin{aligned} Gv(t) + C \frac{dv(t)}{dt} &= Bu(t) \\ y(t) &= L^T v(t) \end{aligned} \quad (1)$$

where $G \in R^{n \times n}$ is the conductance matrix, $C \in R^{n \times n}$ is the matrix resulting from storage elements. $v(t)$ is the vector of time-varying node voltages and branch currents of voltage sources. $y(t)$ is the observed output voltage vector. $u(t)$ is the vector of independent power sources, and $B \in R^{n \times p}$ is the input selector matrix and $L \in R^{n \times l}$ is the output selector matrix. p and l are the number of input and output terminals respectively.

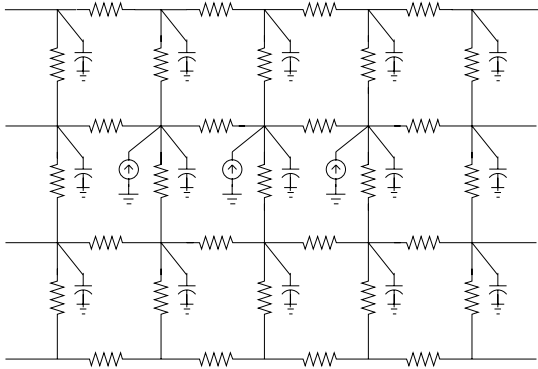


Figure 1: The power grid model used.

The on-chip power grids, one important integrity issue is excessive voltage IR drops due to the unavoidable wire resistance (and inductive effects when inductance are large). IR drop based power grid integrity analysis is different from the general transient analysis in that designers are mainly interested in the voltage drops in the tap current sources as the tap currents are where the power grid network are connected with the logic circuits and IR drops mainly matter from the logic circuit perspective. As a result in our program $L = B$ and $p = l$ in (1). This implies the passive model order reduction can be achieved and it will also lead to more efficient reduction-based simulation for power grid networks as shown later.

Second, for IR drop analysis, what matter are the excessive voltage drops occurring at a few time instances over the simulation period for each node. This is especially the case for real industry power grid networks, where the tap currents are very disruptive in nature as shown in Fig. 2 and so are the IR drops as shown in Fig. 3. Fig. 4 shows the frequency spectrum of the current shown in Fig. 2, which have shapes like sinc functions due to the impulse shapes of currents in time domain.

3. EXTENDED TRUNCATED BALANCED REALIZATION SCHEME

3.1 Extended truncated balanced realization scheme

The new method is based on the recently proposed extended truncated balanced realization method [10]. We first review this method.

For a linear system in (1) under truncated balanced realization reduction framework [13], one first computes the controllable and observable gramians, which measure the controllability and observability of a system to generate the projection matrix to perform the reduction. For instance, the controllable gramian X can also be represented in frequency domain as

$$X = \int_{-\infty}^{+\infty} (j\omega C + G)^{-1} B B^T (j\omega C + G)^{-H} d\omega \quad (2)$$

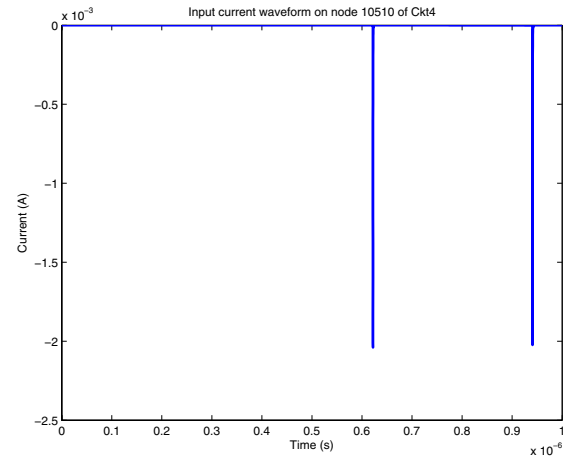


Figure 2: Input current waveform at the node 10510 of Ckt4 (the first one-tenth).

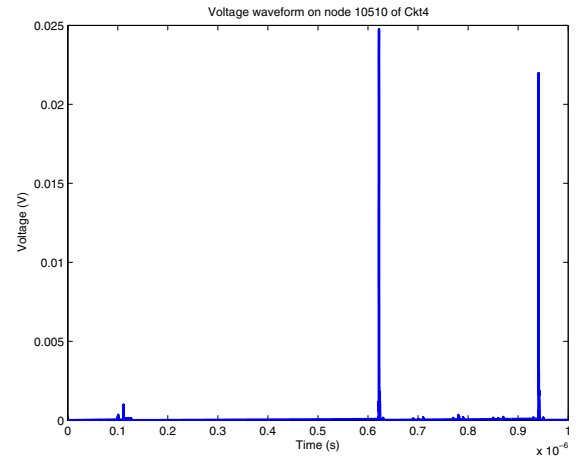


Figure 3: Voltage waveform at the node 10510 of Ckt4 (the first one-tenth).

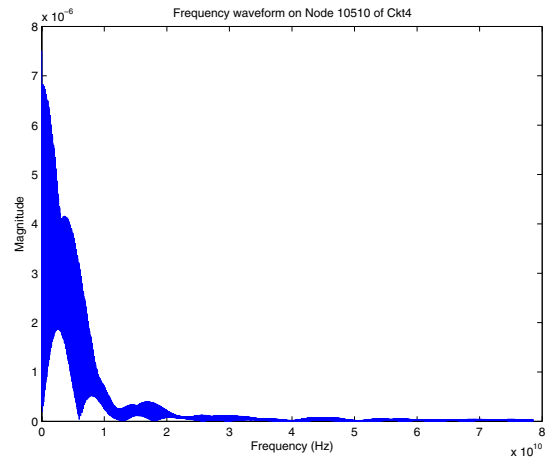


Figure 4: Frequency waveform at the node 10510 of Ckt4 (the first one-tenth).

For our analysis problem, we instead define the frequency-domain

Response gramian,

$$X_r = \int_{-\infty}^{+\infty} (j\omega C + G)^{-1} B u(j\omega) u^T(j\omega) B^T (j\omega C + G)^{-H} d\omega \quad (3)$$

which is different from the gramian concepts in the traditional TBR based reduction framework. Notice that in the new gramian definition, the input signals $u(j\omega)$ are considered. As a result, $(j\omega C + G)^{-1} B u(j\omega)$ serves as the system response with respect to the input signal $u(j\omega)$ and resulting X_r becomes the response Gramian.

To fast compute the response gramian X_r , we can use Monte Carlo based method to estimate the numerical value as done in [14]. Specifically, let ω_k be k th sampling point over the frequency range. If we further define

$$z_k^r = (j\omega_k C + G)^{-1} B u(j\omega_k) \quad (4)$$

then \hat{X}_r can be computed approximately by numerical quadrature methods

$$\hat{X}_r = \sum_k w_k z_k^r z_k^{rH} = Z_r W^2 Z_r^H \quad (5)$$

where Z_r is a matrix whose columns are z_k^r and W a diagonal matrix with diagonal entries $w_{kk} = \sqrt{w_k}$. w_k comes from a specific quadrature method.

The projection matrix V can then be obtained by singular value decomposition (SVD) of Z_r . After this, we can reduce the original matrices into small ones via congruence transformation and then perform the transient analysis on the reduced circuit matrices. If $v_r(t)$ is the response vector from the reduced circuit, then the original waveforms can be obtained by $v(t) = V v_r(t)$.

Notice that we need the frequency response caused by input signal $u(j\omega_k)$ in (4). This can be obtained by fast Fourier transformation on the input signals in time domain. The ETBR method is very amenable to the parallel computing as it essentially performs the Monte-Carlo like sampling in the frequency domain to compute projection matrix where each sampling can be computed independently and thus in parallel.

In our voltage IR drop analysis, as we mention early that the observable ports are also the tap current source nodes, i.e. $B = L$ in (1), the reduced system is passive owing to the property of congruence transformation [15].

4. NEW REDUCTION BASED IR DROP ANALYSIS METHOD

For IR drop analysis, many industry circuits exhibit rapid changing tap current waveforms as shown in Fig. 2. Such impulse-like current waveforms will have the frequency spectrum similar to sinc function in frequency domain as shown in Fig. 4, which has a long tail and thus is significant across wide frequency range. This requires large number of samplings to make ETBR accurate, which degrades its performance.

In this paper, we propose to reduce the errors during the transient simulation of the reduced models. In the new method, we monitor errors for the transient waveforms from the reduced model and switch to the original models when errors are large. Our experimental results show such large errors typically occur around the large voltage drop (spikes) and the proposed method can accurately estimate large voltage drops while still maintain decent speedup over traditional methods. We first present how errors are estimated in the time domain.

4.1 Error estimation in the time domain

One important aspect of the proposed method is to have accurate *a priori* error estimation at each time step t_i .

We propose to use the residual error information of the original on the states obtained from the reduced models. Specifically, for system (1), assume that h_i is the time step at time t_i and $v_r(t_i)$ and

$v_r(t_{i-1})$ are the voltage vectors in the reduced systems at time t_i and t_{i-1} after the time discretization. Then we can define the residual error in time domain as

$$R(t_i) = G V v_r(t_i) + (C/h_i) V (v_r(t_i) - v_r(t_{i-1})) - B u(t_i) \quad (6)$$

$$= (G + C/h_i) V v_r(t_i) - (C/h_i) V v_r(t_{i-1}) - B u(t_i) \quad (7)$$

where $V v_r(t_i)$ is an approximation of the original state $v(t_i)$, V is the project matrix computed from ETBR and $V \in R^{n \times q}$, q is the reduced order. Notice that if $V v_r(t_i)$ is exactly equal to $x(t_i)$, the residual error should be zero. As a result, the norm of $R(t_i)$, $\|R(t_i)\|$ can serve as a good error indicator for the reduced model at t_i . Practically, we take $\|R(t_i)\|_\infty$ as the error indicator, which is the maximum absolute value of the element in $R(t_i)$.

Notice that we are only interested in the tap current nodes and the largest IR drop must happen in one tap current node. As a result, we do not need to check the all the nodes. The new residual formula considering only tap current nodes becomes

$$R_{tap}(t_i) = B^T (G + C/h_i) V v_r(t_i) - B^T (C/h_i) V v_r(t_{i-1}) - B^T B u(t_i) \quad (8)$$

Although $R(t_i)$ still involves the original matrices G and C , only matrix multiplications are involved. The time complexity of (7) is $O(p \times q)$, where p is the number of nodes and q is the size of the reduced model.

4.2 Effective resistance

The residual definition in (8) mainly give the current residual as $u(t_i)$ mainly contains the tap current sources (with only a few voltage sources normally). However, to effectively control the errors, we need to know how much voltage errors such as current residuals will cause. As a result, we need to map from the current residual to the voltage residual (difference).

We introduce the effective resistance to perform the mapping. The effective resistance at time t_i is defined as

$$r_{eff}(t_i) = \frac{\max(v(t_i) - v_{dc}(t_i))}{\max(R_{tap}(t_i))} \quad (9)$$

where \max means taking the maximum value of a vector. To compute $r_{eff}(t_i)$, we have to know the exact response solved from the original system $v(t_i)$. Actually we do not need to compute the effective response at every time step. Instead, we only compute it at the first step and the steps where errors are large and the original solutions are solved.

Our experimental results show that the effective resistances are quite consistent through the time steps for each circuit. Fig. 5 show the histogram for the effective resistance distribution all over the time steps of Ckt4 in the experimental section. It can be seen that the effective resistance is dominated by values around 12. Practically we compute the average effective resistance r_{avg} all over the effective resistance computed seen so far to estimate the allowed maximum current residual.

4.3 Dynamic error control

To control the errors, we need to determine the maximum allowed current residual $i_{r,max}$. If the $\max(R_{tap}(t_i))$ is larger than $i_{r,max}$, the original model will be solved. Otherwise, the reduced model is solved. The $i_{r,max}$ will be computed as

$$i_{r,max} = \frac{v_{ir,max} \times \alpha_{th}}{r_{avg}} \quad (10)$$

where $v_{ir,max}$ is the largest IR drop seen so far and $0 < \alpha_{th} < 1$ is a user-defined threshold specifying the percentage of the allow voltage difference with respect to the largest voltage drop seen so far. Typically α_{th} is around 0.01 to 0.05.

At the beginning, the maximum voltage drop $v_{ir,max}$ may be small and it can lead to the necessary solving of the original models. To

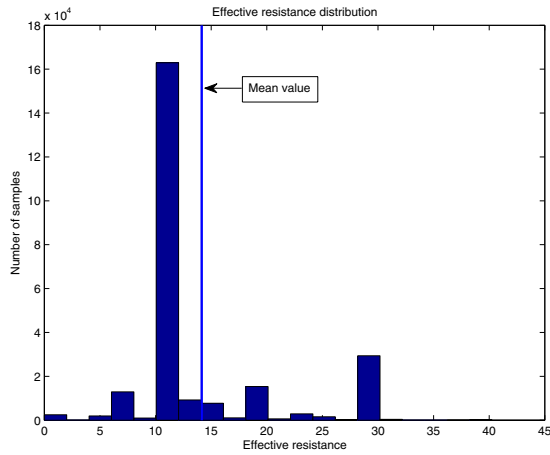


Figure 5: Effective resistance distribution of Ckt4.

avoid this problem, the initial current residual is determined by the largest current value, I_{max} , of all the current sources over all the time steps.

$$i_{r,max} = I_{max} \times \alpha_{th} \quad (11)$$

So the actual allowed current residual will take the larger one of the two $i_{r,max}S^2$.

4.4 The new IR drop analysis algorithm flow

In this subsection, we summarize all the steps we discuss before. We first present the proposed ETBR_IR method in *Algorithm 1*.

Algorithm 1: ETBR based IR drop analysis (ETBR_IR)

Input: Circuit of $G, C, B, u(t)$, number of samples: q , transient simulation step interval.
Output: Max IR drop for the given simulation interval.

1. Convert all the input signals $u(t)$ into $u(s)$ using FFT.
2. Select q frequency points s_1, s_2, \dots, s_q over the frequency range.
3. Compute $z_k^r = (s_k C + G)^{-1} B u(s_k)$.
4. Form the matrix $Z_r = [z_1^r, z_2^r, \dots, z_q^r]$.
5. Perform SVD on $Z_r, Z_r = V_r S_r U_r^T$.
6. $\hat{G} = V_r^T G V_r, \hat{C} = V_r^T C V_r, \hat{B} = V_r^T B$
7. Solve the i th step ($\hat{G}, \hat{C}, \hat{B}, u(t)$), and get $\hat{v}(t)$. $v(t) = V_r \hat{v}(t)$.
8. Substitute $v(t)$ into (G, C) , and get right hand side w_1 . $w = B \times u$.
9. Compute current residual error $R = abs(w - w_1)$. If $\|R\|_\infty$ is less than allowed residual $i_{r,max}$, then goto step 11, else goto step 10.
10. Solve the i th step ($G, C, B, u(t)$), and get $v(t)$. Update r_{avg} and $i_{r,max}$. Goto step 11.
11. Compute max IR drop. $i = i + 1$. Goto step 7.
12. Finish all the time steps and return max IR drop.

In the new algorithm, ETBR_IR first reduces the original circuits from step 1 to 6 using ETBR method. Then from step 7 to step 11, it performs the simulation on the reduced model. At the same time, it watches out for the error in each time step. If the error is larger than the given voltage IR drop threshold, ETBR_IR switches the simulation to the original model to get accurate results and then switch back the reduced model for the next step until we finish all the time step.

5. EXPERIMENTAL RESULTS

The proposed ETBR_IR algorithm has been implemented using C++ and CSparse package [16]. ETBR_IR has been tested on a

workstation with Intel quad-core 2.0GHz CPU and 8GB memory. All the benchmarks are power or ground grids from real industry designs. The statistics are summarized in Table 1. In the table, #Nodes means the total number of nodes in one test circuit. #VS means the total number of voltage sources and #IS means the total number of current sources. #Time Steps means the total number of simulation time steps.

In the experimental setting, the α_{th} is set to 0.05 except for Ckt6 and Ckt7 where α_{th} is set to 0.01. Also the number of samplings is set to 10 for all the case in ETBR_IR.

Table 1: Benchmark circuits

Test Ckts	#Nodes	#VS	#IS	#Time Steps
Ckt1	249475	1	5177	25001
Ckt2	154514	0	624	25001
Ckt3	60999	1	20901	250001
Ckt4	42222	0	10654	250001
Ckt5	49303	0	48756	79001
Ckt6	70127	1	28928	100001
Ckt7	75758	1	28048	100001

We compare ETBR_IR with original ETBR and UltraSim version 7.1, which is a commercial simulation tool from Cadence. UltraSim UPS (UltraSim Power network Solver) is the power grid analysis tool in UltraSim. It is an improved LU solver for power grid network analysis. We consider UltraSim UPS as the standard one, due to the reason that those real industry benchmarks are too large and too challenging for SPICE to solve it. We first show the performance comparison results in Table 2.

Table 2 shows the performance in CPU seconds of ETBR_IR, comparing with original ETBR and UltraSim. From Table 2, we can see ETBR_IR can finish much faster than UltraSim for Ckt1 and Ckt2. It can archive about 37X speedup in average. We notice that ETBR_IR favors circuits with less current sources as shown for Ckt1 and Ckt2 where we see much higher speedup. This is due to the less time spent on the mapping results from reduced models to the original one. For other cases such as Ckt5 where the #IS is almost equal to #Nodes, ETBR_IR still can finish 3x faster than UltraSim.

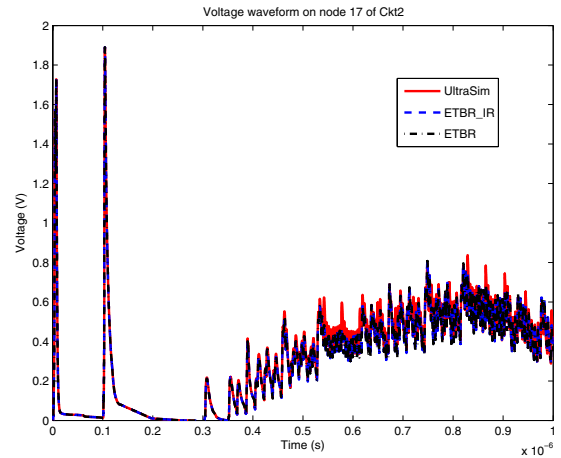


Figure 6: Voltage waveform at the node 17 of Ckt2.

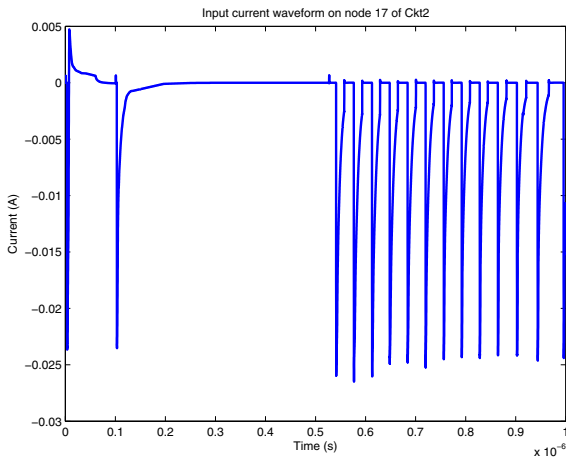
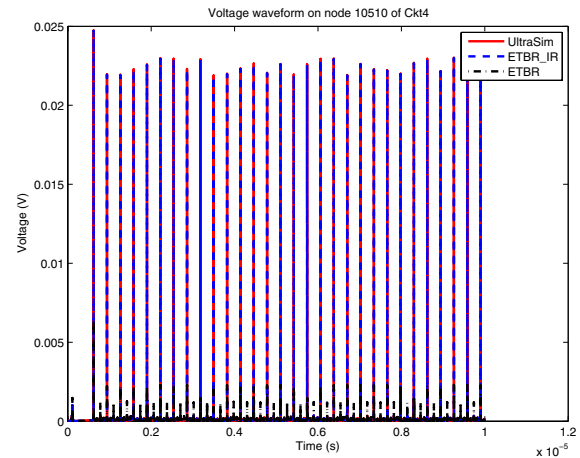
Table 3 shows the accuracy in maximum IR drop values of ETBR_IR compared with ETBR and UltraSim. Here we consider results from UltraSim UPS as the golden and errors are computed as the relative errors to the golden results in percentage.

Table 2: Performance comparison (CPU seconds) of UltraSim, ETBR and ETBR_IR

Test Ckts	UltraSim (s)	ETBR (s)	ETBR_IR (s)	ETBR speedup	ETBR_IR speedup
Ckt1	49653	236	278	210.39	178.61
Ckt2	6906	104	122	66.40	56.61
Ckt3	6130	350	1122	17.51	5.46
Ckt4	3969	234	629	16.96	6.31
Ckt5	3969	551	1182	7.20	3.34
Ckt6	6144	803	1020	7.65	6.02
Ckt7	6523	765	950	8.53	6.87
Avg.				47.81	37.60

Table 3: Accuracy comparison (max IR drop values) of UltraSim, ETBR and ETBR_IR

Test Ckts	UltraSim (mV)	ETBR (mV)	ETBR_IR (mV)	ETBR error	ETBR_IR error
Ckt1	1087.855	1087.812	1087.812	0.00%	0.00%
Ckt2	1899.810	1890.496	1890.500	0.49%	0.49%
Ckt3	12.230	6.021	12.222	50.77%	0.07%
Ckt4	24.734	15.549	24.707	37.14%	0.13%
Ckt5	8.424	5.055	8.363	39.99%	0.72%
Ckt6	196.300	181.251	197.468	7.67%	0.60%
Ckt7	255.920	196.102	252.613	23.37%	1.29%
Avg.				22.78%	0.47%

**Figure 7: Input current waveform at the node 17 of Ckt2.****Figure 8: Voltage waveform at the node 10510 of Ckt4.**

We can see that the max IR drop values computed by UltraSim and ETBR_IR are almost the same. The max difference is less than 2%, and the average difference is less than 1%. Fig. 6, Fig. 8 and Fig. 10 show the voltage waveforms on the max IR drop node of Ckt2, Ckt4 and Ckt5, respectively. The max IR drop values computed by ETBR_IR are sufficiently accurate for the practice purpose. As we can see that the voltage drops are very disruptive and shape. The maximum voltage drop only happens at a number of discrete time points over the the whole simulation period. Such disruptive waveforms comes from the similar input current waveforms as shown in Fig. 7, Fig. 9 and Fig. 11, which show the input current waveforms on the max IR drop node of Ckt2, Ckt4 and Ckt5, respectively. For the original ETBR, the errors for some circuits are quite large (22.78% in average) for the maximum voltage drops. We observe that ETBR works quite well for Ck1 and Ck2. The reason is that Ck1 and Ck2 have input waveforms that change less rapidly compared to other circuits as shown in Fig. 7, Fig. 9 and Fig. 11. We can increase the number of samples to improve the

accuracy at much more computational costs.

6. ACKNOWLEDGEMENT

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7. CONCLUSIONS

In this paper, we have presented a new voltage IR drop analysis approach for integrity verification of large on-chip power delivery networks with rapid-changing tap current sources. It is based on recently proposed sampling based reduction techniques to reduce the circuit matrices before the simulation. The new approach introduce a novel error check mechanism and on-the-fly error reduction during the simulation of the reduced circuits to improve the accuracy of estimating large IR drops. Experimental results have shown the proposed IR drop analysis method can significantly improve the accuracy of ETBR method at similar computing cost, while it can

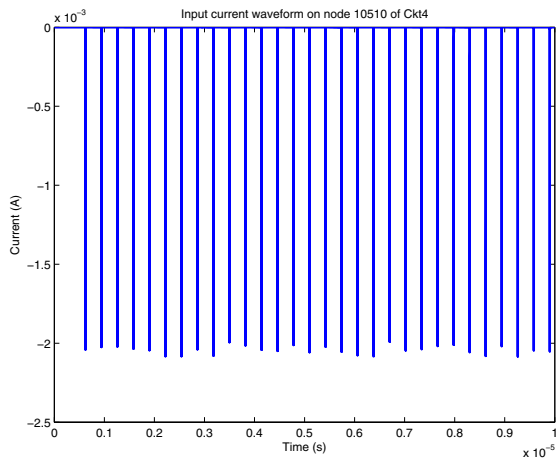


Figure 9: Input current waveform at the node 10510 of Ckt4.

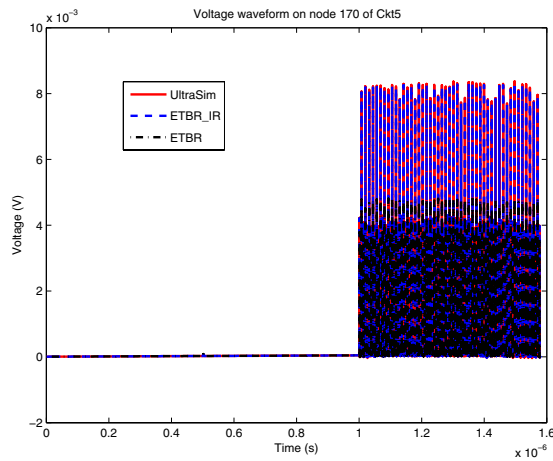


Figure 10: Voltage waveform at the node 107 of Ckt5.

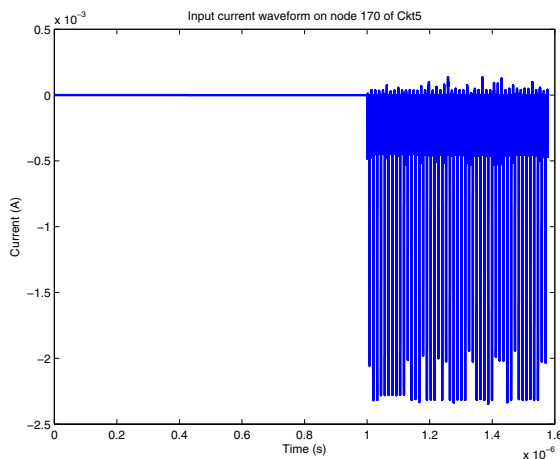


Figure 11: Input current waveform at the node 107 of Ckt5.

lead to 10X more speedup over commercial power grid solver UPS in UltraSim with about 1-2% errors on a number of real industry circuits.

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