Fast Two-Dimensional Finite Element Analysis for Power Network DC Integrity Checks of PCBs

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***Abstract*—Power delivery network integrity is very important for the high performance printed circuit boards (PCBs) designs. The direct current (DC) analysis of power/ground networks in PCBs plays the central roles for the power delivery integrity check. In this paper, we propose a novel two-dimensional finite element method (FEM) based DC power networks integrity analysis for PCBs. Unlike the existing 3D finite element based DC analysis such as the Cadence Sigrity PowerDC tool, 2D finite elements are used in the new method for space discretization so that the number of elements can be significantly reduced. To model the vertical vias and horizontal connects among different layers and parts in PCBs, simple resistive line elements are used to further redudce elements. To further reduce the number of elements, a novel contour shape modeling method is introduced so that we can easily trade off the efficiency and accuracy. Our experimental results show that the proposed 2D PCB DC solver is 29.29% faster than the commercial PowerDC tool with similar accuracy on the practical industry PCB designs.**

I. Introduction

For high-performance printed circuit board (PCB) and package designs, the power ground network integrity (such as DC current density, DC voltage IR drops) needs to be checked to ensure the long-term reliability operations of the PCBs and circuit systems. Improper power ground network design may lead to excessive voltage IR drops and DC current, which will cause serious reliability problems to the PCBs.

DC analysis for electronic circuits such as PCBs, packages and integrated circuits essentially boils down to solve the Laplace or Poisson partial differential equations (PDE), which comes from more general Maxwell equations [1]–[3]. There are many numerical methods in solving the differential equation or integral equation derived from the general Maxwell equations. 3D finite element method (FEM) based solution [4] is a general numerical approach to this problem with good accuracy. However, this method typically suffers high computational costs and large memory footprint due to too many unknowns (or large number of elements generated), especially in an iterative design of PCBs. Other methods like Partial Element Equivalent Circuit (PEEC) [5] and finite-difference time-domain (FDTD) method [6] also suffer the same problem. Method of moments [7] can solve electromagnetic boundary or volume integral equations in the frequency domain. But leads to dense, even full matrices to solve though it has fewer unknowns.

The highlighted area in Fig. 1(b) is part of the power network V1P0_S0 as shown in Fig. 1(a) which will be used as the example later. The practical network has many complicated structures (vias, planes) and layers and boundary conditions (voltage and current sources). As a result, finite element method (FEM) will be a good fit as it can deal with complicated structures and naturally handle the two boundary conditions. The challenge is how to mitigate its high computational cost.

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(a) (b)

Fig. 1. Network V1P0_S0 is picked from Intel Galileo_G87173_204 PCB on the purpose of testing. The board has totally six copper layers: top, power, lyr_1, lyr_2, ground and bottom while the V1P0_S0 network is distributed on top, power and bottom layers. (a) The geometrical 3D-display of the power network V1P0_S0. (b) Practical view of network V1P0_S0 presented in 1(a) on the power layer.

This paper focuses on DC analysis for PCBs, including detection of excessive voltage IR drop, areas of excess current density and even power and thermal hotspots. We propose a novel two-dimensional finite element method (FEM) based DC power networks integrity analysis for PCBs. Unlike the existing 3D finite element based DC analysis such as the Cadence PowerDC tool. We apply 2D finite elements for space discretization so that the number of elements can be significantly reduced. To model the vertical vias and horizontal connects among different layers and parts in PCBs, simple resistive line elements are employed. To further control the number of elements to be used, the contour shape modeling is introduced so that one can easily to trade off the efficiency and accuracy. Our numerical results show that the proposed 2D PCB DC solver is 29.29% faster than the commercial PowerDC with simular accuracy on the practical industry PCB designs.

II. Review of finite-element-based solver for steady state electrical field

Finite element method (FEM) introduced in 1940 is for solving partial differential equations (PDEs) for initial and boundary-value problems [8]. Based on the elegant mathematical theory of weak solution of PDEs, FEM can deal with Neumann boundary conditions (BCs) in a nature way and it can also deal with irregular geometrics much more easily. We briefly review steady-state electrical field solving process, which can be viewed as FEM for Poisson's equation with Dirichlet and Neumann boundary conditions.

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For electrical field in the steady state, we have

$$E = -\nabla V,\ \nabla \cdot E = \frac{\rho}{\epsilon_0}. \tag{1}$$

where V is the voltage potential and E is the electrical field vector. Then we have the so-called Poisson's equation in the differential form

$$\nabla^2 V = -\frac{\rho}{\epsilon_0} \tag{2}$$

For steady state electrical field with constant current flow, i.e., $\rho = 0$, we end up with a Laplace equation $\nabla^2 \phi = 0$, and we have the following boundary conditions:

$$\begin{aligned} v_i(t=0) = v_{i0}, i = 1...m \quad (voltage) \\ i_i(t=0) = i_{i0}, i = 1...k \quad (current) \end{aligned} \tag{3}$$

In general, the electrical potential V in steady state can be described by the Poisson's equation with both Dirichlet and Neumann boundary conditions given as follows:

$$\begin{aligned} \nabla^2 V = f(x),\ x \in \Omega, \\ V = u(x),\ x \in \Gamma_D, \\ \nabla V \cdot \mathbf{n} = g(x),\ x \in \Gamma_N, \end{aligned} \tag{4}$$

where $\Omega \subset R^n$ is the solution domain with the boundary $\partial\Omega$, Γ_D is the part of the boundary where Dirichlet boundary conditions are given, Γ_N is the part of the boundary where Neumann boundary conditions are given, $V(x)$ is unknown electrical field to be found, $f(x)$, $u(x)$, and $g(x)$ are given electrical charges and voltage sources and current sources.

The weak formulation for FEM is used for real computation due to that it is difficulty to enforce Dirichlet and Neumann boundary conditions. Given the test function s, then we have:

$$\int_\Omega (\triangle V - f) \cdot s d\Omega = 0. \tag{5}$$

Integrating this equation by part and applying the divergence theorem, we obtain

$$\begin{aligned} \int_\Omega \nabla V \cdot \nabla s d\Omega = \int_{\Gamma_D} s \cdot (\nabla V \cdot \mathbf{n}) d\Gamma \\ + \int_{\Gamma_N} s \cdot (\nabla V \cdot \mathbf{n}) d\Gamma - \int_\Omega f \cdot s d\Omega. \end{aligned} \tag{6}$$

For Dirichlet boundary condition, the integral term $\int_{\Gamma_D} s \cdot (\nabla V \cdot \mathbf{n}) d\Gamma$ in (6) vanishes and hence the weak form of Poisson's equation for $V \in V(\Omega)$ and $s \in V_0(\Omega)$ becomes:

$$\begin{aligned} \int_\Omega \nabla V \cdot \nabla s d\Omega = \int_{\Gamma_N} s \cdot (\nabla V \cdot n) d\Gamma - \int_\Omega f \cdot s d\Omega, \\ V(x) = u(x), x \in \Gamma_D. \end{aligned} \tag{7}$$

Dirichlet BC is called Essential Boundary Conditions, as it is not a part of the weak form. For Neumann boundary condition, we know $g(x) = \nabla V \cdot \mathbf{n}$ and the integral term over the Neumann surface in (7) contains exactly the same flux, so we have

$$\int_\Omega \nabla V \cdot \nabla s d\Omega = \int_{\Gamma_N} g \cdot s d\Gamma - \int_\Omega f \cdot s d\Omega. \tag{8}$$

Neumann BC is called Natural Boundary Conditions, as is part of the weak form. Now we can write the resulting weak form for the Poisson's problem in (4). For any test function $s \in V_0(\Omega)$, we need to find $V \in V(\Omega)$ such that:

$$\begin{aligned} \int_\Omega \nabla V \cdot \nabla s d\Omega = \int_{\Gamma_N} g \cdot s d\Gamma - \int_\Omega f \cdot s d\Omega, \\ V(x) = u(x), x \in \Gamma_D. \end{aligned} \tag{9}$$

To solve numerically given problem based on the weak form (9), we have to go through the following five steps in Algorithm I

Algorithm 1 Finite element solver for Poisson's equation

1: Define the domain Ω and the surfaces Γ_D and Γ_N.
2: Define the known functions f, u, and g.
3: Define the unknown function V and the test function s.
4: Define essential boundary conditions (Dirichlet conditions) $V(x) = u(x),\ x \in \Gamma_D$.
5: Define equation and natural boundary conditions (Neumann conditions) as the set of all integral terms $\int_\Omega \nabla V \cdot \nabla s d\Omega$,$\int_{\Gamma_N} g \cdot s d\Gamma$,$\int_\Omega f \cdot s d\Omega$.

III. New 2D FEM DC solution for PCBs

In this section, we present the new 2D FEM solver. We present the two new approximation techniques to speed the FEM analysis for power networks analysis of PCBs.

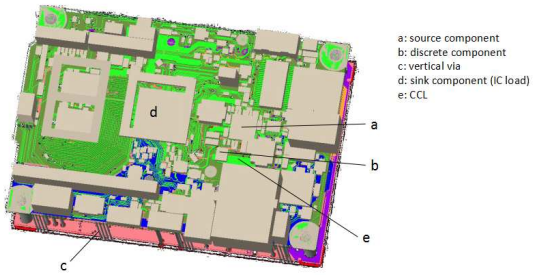
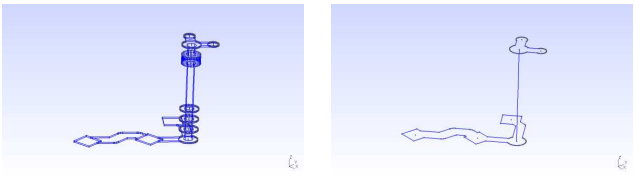


Fig. 2. A practical 3D-view of layouts of Intel Galileo PCB. The notation a, b, c, d and e are respectively represented for source component, discrete component, vertical via, sink component and CCL.

A power network in PCBs usually contains five elements: electrical source, copper clad laminate (CCL), via, discrete component and IC load as shown in Fig. 2. Since the thickness of the copper clad laminate is uniform on each layer (we may have many layers), thus we can assume an identical electrical potential value in the z direction. Therefore, we can regard the layer as a geometrical plane assuming the voltage are same in the z direction. As a result, we can reduce the original 3D voltage potential analysis problem into 2D voltage analysis problem.

However, for a practical power networks in PCBs, it is still 3D structures as we may have many layers which are connected by vias as shown in Fig. 3(a). To mitigate this problem, we regard vertical via as a vertical line segment and represent it with resistive 2-node line element in FEM method. As shown in Fig. 3(b), the original 3D structure has been converted to several 2D planes connected by vertical line segments, which can be represented by 2D elements (lines or triangles) completely.



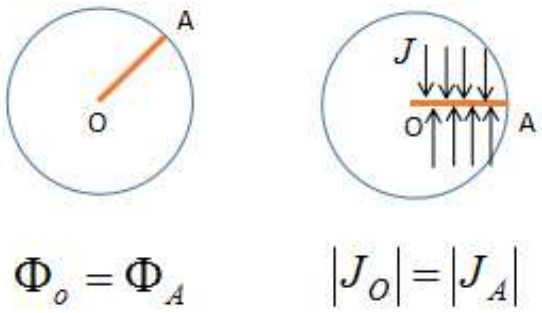
(a) (b)

Fig. 3. Transformation from 3D structure to 2D structure for power networks of PCBs. (a) Original 3D structure. (b) Transformed 2D structure by establishing a approximate 2D model.

To solve the extracted 2D model for a power network, we first use 2D elements (lines or triangles) to mesh 2D plane as introduced in Section II. Then we treat vertical vias and discrete components as pure resistance based on the simple Ohm's law. Next we set up in given voltage (Dirichlet) or current boundary (Neumann) conditions.

For voltage boundary condition which usually specified by source component pins, we add a line element connecting the pin center and an arbitrary point on the edge of the pin, which makes the Dirichlet boundary conditions. So the electrical potentials on the line are assumed to be identical. As shown in Fig. 4(a).

Similarly, for current boundary condition which usually specified by sink component pins, we take the same measure. We assume the magnitude of current density on the boundary line to be the same as shown in Fig. 4(b). The current boundary condition is recognized as Neumann BC here. The direction of positive current is ejected from the pin pad into the OA line orthogonal to the X-Y plane.



(a) (b)

Fig. 4. A round pin pad is taken for demonstration here both for voltage and current BCs. Point O is the pin center and A is an arbitrary point within the pin pad. (a) Suppose that line segment OA has identical electrical potential so we can build voltage boundary conditions on OA element. (b) Suppose that line segment OA has identical current density magnitude so we can build current boundary conditions on OA element. Note that the direction of postive current density is ejected from the pin pad into OA line orthogonally.

The second approximation method we employed is to control the number of elements at costs of very small accuracy degradation. In finite element meshing process, the complex contour may lead to very large numbers of elements if very fine lines are used to model the complicated shapes or contours like the cycles or arcs as very dense meshes are used around those complicated contours and shapes as shown in Fig. 5(a) and 5(b). Actually, those dense meshes are unnecessary as the voltages around those shapes will not change dramatically at least in the PCB case as shown in this figure.

As a result, we introduce the *Critical Angle* concept to reduce the number of contour points and thus control the number of the elements around those contours. Specifically, let p_1,p_2,...,p_n be the point sequence of the contour. Each time delete some point p_i if the included angle of the line segments $p_{i-1}p_i$ and p_ip_{i+1} is greater than the critical angle and then update the point range until there is no point to be deleted or there are only three points left. Algorithm 2 describes the details and Fig. 5 shows that the algorithm significantly reduce the number of elements for the same networks. Most important of all, we can regulate the number of meshes by setting the value of *Critical Angle*. The smaller the value of *Critical Angle* is set, the sparser the meshes will be. However, too small value will cause serious accuracy less. After some trial and error, we found that the low bound for the *Critical Angle* is about 150 degrees.

Algorithm 2 Critical Angle based contour modeling in meshing process

Input: An array A of original contour points, Critical Angle δ, length of array n
Output: A

```
for i = 1;i ≤ n;i++ do
    Calculate the included angle θ of line p_{i-1}p_i and p_ip_{i+1} (p_0 = p_n, p_{n+1} = p_1)
    if θ > δ && n > 3 then
        Delete p_i from A
        n = n − 1
        i = i − 1
    else if n > 3 then
        Continue;
    else
        Break;
    end if
end for
Return A
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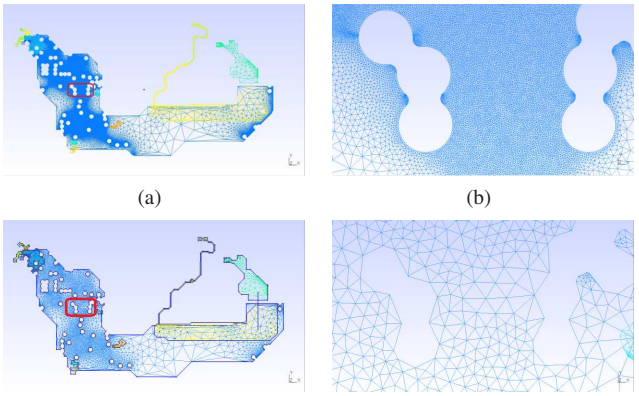


(a) (b) (c) (d)

Fig. 5. Boundary contour get simplified after the CriticalAngle algorithm is applied. (a) Dense meshing before simplified, with 147383 mesh nodes and 288436 mesh elements. (b) Partial enlarged area of the red rectangle in Fig. 5(a). (c) Sparse meshing after simplified, with 7157 mesh nodes and 13477 mesh elements. (d) Partial enlarged area of the red rectangle in Fig. 5(c).

IV. Experimental Results and Discussions

The proposed 2D FEM DC solver has been implemented in C++ with the Armadillo numerical package [9]. The experi-

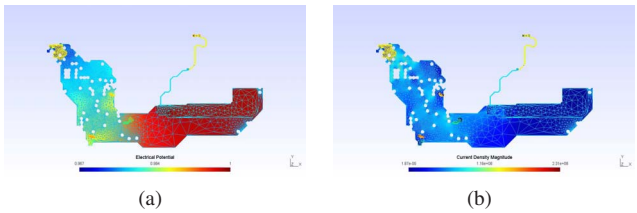
mental data are collected on the Linux severs with Intel Xeon E5-2698 CPU at 2.3GHz. We use the Gmesh program [10] to generate the 2D mesh for our 2D FEM solver.

We compare the numeration solution of 2D FEM with Cadence Sigrity PowerDC on a industry PCB design, the Galileo PCB [11]. The example tested here is a power network, named V1P0_S0. It consists of one source component pin C3B9.1 with voltage 1V, multiple pins of sink component U2A5 with total 10A current and V1P0_S0 net. We set the copper conductivity with 5.959e+7S/m as PowerDC does by default and employ the equal current model in pins belonging to U2A5.

Table I shows the comparison results of voltage IR drops between PowerDC and the 2D FEM solver. The voltage values calculated by our 2D FEM solver are consistently a little bigger than by PowerDC and the average IR drop is very close. However, the solver takes 5.441s CPU time totally while PowerDC takes 7.034423 according to its analysis report, reducing time cost by 29.29% against PowerDC. Voltage distribution and current density distribution plots are shown in Fig. 6.

TABLE I
VOLTAGE IR DROP COMPARISONS AGAINST POWERDC

U2A5 pin number	Voltage at pins (mV)	
	PowerDC	2D FEM
AD14	966.262	967.481
AB14	966.465	967.652
Y14	966.612	967.727
V14	966.558	967.707
Y16	966.742	967.894
V16	966.841	967.986
AB18	966.676	967.902
Y18	966.796	967.968
V18	967.229	968.26
T18	967.378	968.386
AB20	966.62	967.866
Y20	967.193	968.237
V20	967.45	968.575
Avg IR drop	33.168	32.028



(a) (b) (c) (d)

Fig. 6. Voltage distribution and current density distributions. (a) Voltage distribution plot resulted from the 2D FEM solver. (b) Current density distribution plot resulted from the 2D FEM solver. (c) Voltage distribution plot on PWR layer resulted from PowerDC. (d) Current density distribution plot on PWR layer resulted from PowerDC.

Now we study the impacts of the *Critical Angle* concept proposed in Section III, which allow us to perform the trade-off between the solver efficiency and accuracy. By setting the value of the *Critical Angle*, we can regulate the number of mesh nodes and elements and also the accuracy of the results. Here we also choose V1P0_S0 as the test power network. Table II shows the meshing results from Gmsh while different values of the *Critical Angle* are set. It is clearly seen that the meshing time decreases significantly when the critical angle decreases to $150°$. When it reaches below $150°$, it causes serious deformation of the contour area and thus poor accuracies. As a result, $150°$ is a good trade-off choice between solver efficiency and accuracy.

TABLE II
PERFORMANCE COMPARISON FOR DIFFERENT CONTOUR MODELINGS IN MESHING

Index	Critical Angle (°)			
	150	160	170	180
Meshing time (s)	0.869719	1.04875	3.87363	16.9746
No. of nodes	6437	10049	34023	146202
No. of elements	13883	21461	70603	298786
Solver run time (s)	5.441	21.281	-	-
Avg IR drop (mV)	32.028	32.621	-	-

V. CONCLUSION

In this paper, we have proposed fast 2D finite element method for DC integrity analysis of PCBs. The new method uses 2D mesh instead 3D mesh for the analysis so that the number of elements can be significantly reduced with marginal accuracy loss. We also use a simple resistive line to replace all the vias. To further reduce the number of elements, we proposed *Critical Angle* concept to approximate the contours of the complicate shapes in the PCBs so that better accuracy and efficiency trade-off can be made. The proposed 2D FEM DC solver was compared against the commercial Cadence PowerDC solver on an industry PCB design. The new solver shows similar accuracy while delivering 29.29% speedup over PowerDC.

VI. ACKNOWLEDGMENT

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