

# Recent Advance in Computational Prototyping for Analysis of High-performance Analog/RF ICs

Hao Yu, and Sheldon X.D. Tan

**Abstract**<sup>1</sup>—*The design of high-performance analog/RF ICs is challenging and requires numerical efficient design tools. This paper reviews a number of recent research advances in modeling and analysis of high-performance analog/RF ICs. We will discuss the structured analysis of EM-coupling, the non-Monte-Carlo mismatch analysis, and the nonlinear macromodeling for the system-level synthesis.*

**Index Terms** — Analog/RF ICs, EM-coupling, Mismatch, Nonlinear Macromodel

## I. INTRODUCTION

The smart mobile system has become the next-wave driving the entire chain of the semiconductor industry. A 2Gb/s wireless link can easily join a high-definition (HD) TV and a HD DVD, and upload a movie to iPhone or iPod. The use of (unlicensed) GHz-band is the current approach to provisioning this amount of bandwidth for the multimedia application. The design of front-end analog/RF ICs for this sake, however, requires a high-performance integration [1-2], which is currently realized in two orthogonal directions. The first direction goes vertically by scaling down the transistor size. A design at millimeter (mm)-wave (>10GHz) and nano-meter (<90nm) challenges the traditional electronic-design-automation (EDA) flow as there is no more single transistor recognizable because of the strong electromagnetic (EM) coupling and the process variation. The other direction goes horizontally to improve the performance by heterogeneously integrating multiple functionary modules under multiple process technologies. This leads to a problem on how to abstract the design complexity between the system-level synthesis/verification and the device-level details. Therefore, a high-performance integration operating at the mm-wave frequency needs to explore both design technique and high-frequency modeling of both active and passive devices. Moreover, a new system design methodology is also needed for the heterogeneous integration.

The particular computer-aided-design (CAD) techniques applied for this sake, called *computational prototyping* in this paper, have to ensure the device-level robustness under EM coupling or process variation, and also to provide an essential behavior mode for the system-level exploration. Though there are many works in this field recently, due to the limited space, this paper only reviews a few recent developments in the analysis of high-performance analog/RF ICs. In Section II, we

show the advance in dealing with EM-coupling. In Section III, we present the advance in analog mismatch analysis. In Section IV, we discuss the need of nonlinear macromodeling for the high-level analog/RF synthesis. We conclude the paper in Section V.

## II. EM COUPLING

Because of such a high-frequency operating region, interconnect, passive device (such as spiral inductor), active device (such as CMOS transistor), substrate and package are strongly coupled inside the electro-magnetic field. Everything is no longer ideal but lossy, distributed and noisy. From a design point of view, the use of distributed elements, matching networks and transmission lines can be employed to improve the performance of those building blocks in the front-end analog/RF ICs such as the LNA, mixer and VCO. However, the verification and optimization of a design has become typically challenging since EM-coupled devices are no longer individual but unified. Particularly, the magnetic coupling is a big-headache as it is a long-range effect. The defacto partial element equivalent circuit (PEEC) model assumes a branch current viable for each piece of coupled branch current. This leads to a concept of *partial-inductance*, which state matrix is dense, not diagonal dominant and hence slows down the verification/optimization time.

Recently, people find that the inverse of partial-inductance matrix is diagonal dominant and hence can be stably sparsified [3-4]. However, compared to the partial-inductance with the branch-current variable, it is still a mystery which state-viable would be associated with the new inverse-inductance element such that a new modified-nodal-analysis (MNA) can be employed to stamp the inverse-inductance into a circuit simulator like SPICE. A recent work in [5] reveals that the magnetic flux (or the volume integral of vector potential) is the state-variable associated with the inverse-inductance element, and a new modified-nodal-analysis in frequency(s) domain can be found below,

$$\left( \left[ \begin{array}{cc} G & E_i L^{-1} \\ -L^{-1} E_i^T & 0 \end{array} \right] + s \left[ \begin{array}{cc} C & 0 \\ 0 & L^{-1} \end{array} \right] \right) \begin{bmatrix} v_n \\ \phi_i \end{bmatrix} = B u(s) \quad (1)$$

where  $G$  is the conductance matrix,  $C$  is the capacitance matrix,  $L^{-1}$  is the inverse-inductance matrix,  $E_i$  is the incident matrix describing the topology of branch magnetic-fluxes, and  $B$  is the adjacent-matrix describing the topology of input ports. Moreover,  $v_n$  is the vector of nodal-voltage variables,  $\phi_i$  is the vector of branch-magnetic-flux variables, and  $u(s)$  is the

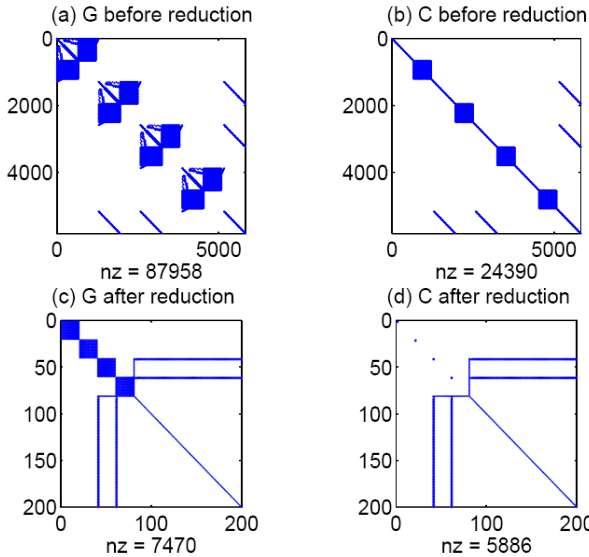
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vector of input sources. Such a new MNA, called VNA, is sparse since  $G, C, L^{-1}, E_f$  are all sparse. In addition, it is also symmetric and semi-positive-definite (s.p.d.).

A magnetic-coupling sparsified network is loosely coupled, and hence can be further reorganized into a bordered-block-diagonal form below [5] [19]

$$\begin{bmatrix} M_1 & & & X_1 \\ & \ddots & & \vdots \\ & & M_m & X_m \\ -X_1^T & \dots & -X_m^T & M_0 \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_m \\ x_0 \end{bmatrix} = \begin{bmatrix} B_1 \\ \vdots \\ B_m \\ 0 \end{bmatrix} u(s) \quad (2)$$

This can be either obtained by natively partitioning the network based-on the sub-circuit structure, or by directly performing a min-cut partitioned of the overall state-matrix using tools like *hmetis* [6]. For example,  $M_i$  in the diagonal can be blocks representing the internal nodes of sub-circuits,  $M_0$  is an interconnection block of external nodes, and  $X_i$  represents the boundary interconnections between internal nodes to external nodes. The state matrix under such a BBD form results in a fast-matrix solver using either the hierarchy or the parallelism. More importantly, after a stable sparsification of EM coupling, the circuits can be recognizable at the sub-circuit level.



**Fig. 1. Sparsity of state matrices  $G$  and  $C$  are preserved at block-level after reduction. A hybrid matrix solver can be applied to explore the sparsity at block-level for reduced state matrices.**

Particularly, when the linear part (passive devices) is separated from the nonlinear part (active derives), a BBD formed linear network can be further compacted by a structure-preserving model order reduction [5] [19]. As shown by [5], instead of applying a flat orthonormalized subspace during the reduction, a block-diagonal-structured subspace

$$\begin{bmatrix} Q_1 \\ \vdots \\ Q_m \\ Q_0 \end{bmatrix} \rightarrow \begin{bmatrix} Q_1 & & & \\ & \ddots & & \\ & & Q_m & \\ & & & Q_0 \end{bmatrix} \quad (3)$$

can be employed during the reduction to preserve the BBD structure. As a result, a hybrid matrix solver can be employed to further accelerate the analysis of dimension reduced system, where the sparse-BBD solver is applied on the top and each reduced dense block can be solved by a dense-matrix solver as an entry in the sparse-BBD matrix. Fig. 1 illustrates the BBD-structure preservation for the state matrices  $G$  and  $C$  before and after the reduction, where NZ is the non-zero entries of the state matrices. Clearly, the reduced state matrices preserve the BBD structure, where the reduced  $G$  and  $C$  have a 16.1% and 14.6% sparsification ratios, respectively.

### III. ANALOG MISMATCH

In addition to the EM-coupling, the device-level process variation, or so called mismatch, is the key to a precision analog circuit design such as ADC/DACs in sub-90nm technologies. For example, the  $3\sigma$ -variation of CMOS drain currents nearly doubles for every process generation [7]. There are two types of mismatch. One is systematical (or global spatial variation), and the other is stochastic (or local random variation). The stochastic mismatch is the most difficult one to analyze. Most CMOS mismatch models are based on the Pelgrom's work [8], which relates the local mismatch variance of the channel current  $I_d$  with the area  $A$  by a geometrical dependence equation

$$\sigma_{I_d} = \frac{\kappa^\beta}{\sqrt{A}} \quad (4)$$

for two devices closely laid out. Note that  $A=W \times L$  is the area of a width  $W$  and length  $L$ , and  $\kappa^\beta$  is an extracted constant depending on the operating region  $\beta$ . For other transistors such as diode, BJT and etc. and to consider process parameters other than the geometry, a more general purposed mismatch model can be derived through a backward propagation of variance (BPV) method [9]. The BPV model relates the local mismatch of an electrical property  $e$  with those process parameters  $p_i$  by a first-order sensitivity equation

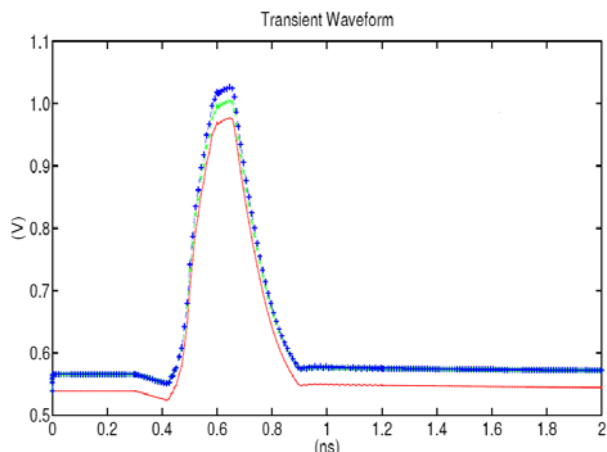
$$\sigma_e = \sum_i \left( \frac{\partial e}{\partial p_i} \right) \sigma_{p_i} \quad (5)$$

Traditionally, Monte-Carlo (MC) analysis is used to analyze the stochastic mismatch and predict the statistical functionality. Its computational cost is high since MC analysis requires a large number of repeated circuit simulations. Many non-Monte-Carlo methods [10-11] are developed recently for the stochastic mismatch analysis. The work in [10] first calculated  $dc$  sensitivities with respect to small device-

parameter perturbations and scaled them as desired mismatches. SiSMA [11] studies the mismatch within the framework of the stochastic differential algebra equation (SDAE) similar to deal with the transient noise [12]. Due to the introduction of the random variable into the DAE, it is unknown if the derivative is still continuous. Moreover, designers' top interest is the mismatch of the channel current in CMOS transistors. SiSMA thereby models the mismatch as a stochastic current-source and formed a SDAE.

$$f(x, \dot{x}, t) = Fi(x, \xi) + Bu(t) \quad (6)$$

where  $x$  ( $\dot{x} = dx/dt$ ) is the state variable including nodal voltage and branch current,  $f(x, \dot{x}, t)$  is to describe the nonlinear i-v relation, and  $u(t)$  is the external sources with a topology matrix  $B$  describing how to add them into the circuit. We model the mismatch as a current source  $i(x, \xi)$  added at the right-hand-side (rhs), where  $F$  is the topology matrix describing how to connect  $i(x, \xi)$  into the circuit.



**Fig. 2. Transient waveform comparison for a diode-chain: the nominal transient (red line “- - - -”); the transient with mismatch by SiSMA (green line “- . \* - .”), where mismatch is added at  $ic$  only; and the transient with mismatch by the method adding mismatch at transient trajectory (blue line “- . - . -”).**

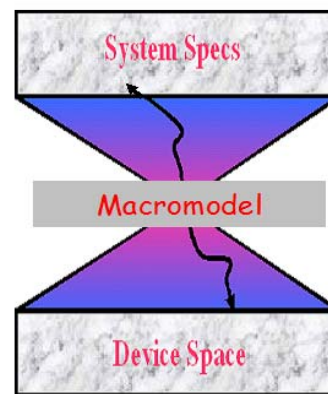
By assuming that the magnitude of the stochastic mismatch is much smaller than the nominal case, SiSMA linearizes the nominal SDAE at  $dc$  with the stochastic current source. The obtained  $dc$  solution is used as an initial condition ( $ic$ ) for the transient analysis. As the stochastic current source is only included during  $dc$ , this assumption may not hold to accurately describe the mismatch during the transient simulation. Fig. 2 shows the transient waveforms comparison for a diode-chain by the nominal transient, the transient with mismatch by SiSMA, where mismatch is added at  $ic$  only; and the transient with mismatch by a method adding mismatch at transient trajectory. Clearly, adding mismatch only at  $ic$  can lead significant waveform error.

Moreover, instead of performing the Monte-Carlo simulation, SiSMA calculates the mismatch by the extraction and analysis of a covariance matrix. It would be slow to analyze the covariance matrix for thousands of devices.

Therefore, there is still a need to develop a fast transient mismatch analysis with a different non-Monte-Carlo method.

#### IV. NONLINEAR MACROMODEL

The heterogeneous integration of multiple functionary components under multiple process technologies dramatically improves the system performance. However, at the same time, it introduces a huge design complexity, in terms of a large gap between the system and the device. A behavior model for the system exploration only needs an essential abstraction of the device detail including the EM-coupling and mismatch. Macromodeling becomes an important bi-directional link for such a need, which can either have a top-down mapping from the system to device spaces, or have a bottom-up abstraction from device to system specs.



**Fig. 3. The use of macromodeling helps heterogeneous integration in twofold: (a) a top-down mapping from system specs to device spaces; (b) a bottom-up abstraction from device details for system optimizations.**

Macromodeling, or so-called model order reduction, is essentially to identify the dominant state variables of a linear/nonlinear circuit and system. This can be viewed as a coordinate transformation. For linear time-invariant (LTI) circuits such as the interconnect, package, power/grid, clock network and etc., the coordinate transformation can be described by a linear mapping (projection)

$$z = V^T x, \quad x = Vz \quad (7)$$

where a small dimensioned projection matrix  $V$  ( $N \times q$ ,  $q \ll N$ ) can be constructed from a subspace [19]. Some methods [13] construct such a subspace by moments, expanding a system transfer function at one or multiple frequency points. The other methods such as the POD and fast TBR [14] construct the subspace by taking the spectrum (eigenvalue/singular-value vector) of snapshots of waveforms in frequency domain.

As an extension to the linear time-variant circuits such as the switch-cap, filter, dc-dc converter and etc., an equivalent system transfer function similar to the LTI system can be formed near the periodic-steady-state (PSS). Due to the

boundary condition usually enforced for a two-point PSS problem, the state-matrix shows a cyclic structure. Therefore, a (triangular) structured approach can be employed to facilitate the construction of a structured subspace [15].

For weakly nonlinear circuits such as the LNA, mixer and etc., Volterra series have been tried to form an exact frequency-domain bilinear transfer function through a Carleman linearization [15]. However, due to the curse of exponentially increased dimension, its according system transfer function is too prohibitive to expand and to generate moments, or subspaces for a nonlinear model order reduction. The work in [16] introduces an iterative algorithm that can alleviate the computational cost up to 3<sup>rd</sup> order. As such, constructing the subspace from expanded moments may not show any light for the nonlinear model order reduction.

The more viable approaches construct subspaces based on the transient trajectory [17-18]. Similar to the linear mapping in (7), a nonlinear mapping function defined by a function  $\lambda$

$$z = \lambda(x), \quad x = \lambda^{-1}(z). \quad (8)$$

For the simplicity of illustration, we assume an ordinary differential equation (ODE) form below

$$\dot{x} = f(x, t) + Bu(t) \quad (9)$$

for a general differential-algebra-equation (DAE) representation of a nonlinear system (See defined terms in equation (6) for a DAE). Note that

$$\dot{z} = \frac{d\lambda}{dx} \frac{dx}{dt} = \left( \frac{d\lambda}{dx} f(x, t) \right) + \left( \frac{d\lambda}{dx} B \right) u(t). \quad (10)$$

As such, if we can find a lower-dimensioned nonlinear mapping function  $\lambda$  ( $N \times q$ ,  $q \ll N$ ), the original nonlinear system can be reduced using its tangent (linearized) subspace spanned by  $d\lambda/dx$ , or called manifold.

The work in [18] relates the above nonlinear mapping function  $\lambda$  with a trajectory piecewise linear (TPWL) method [17]. It leads to a local two-dimensional (2D) projection, called maniMOR. Since such a local 2D-projection is constructed from local tangent subspaces, maniMOR maintains a high accuracy. However, it could be computationally expensive to project and store when the number of local tangent subspaces is large. In contrast, the TPWL method [17] approximated the nonlinear mapping function  $\lambda$  by further aggregating those local tangent subspaces with the use of a global singular-valued composition (SVD). This results in a global one-dimensional (1D) projection. Obviously, the global 1D-projection in TPWL leads to an efficient runtime. On the other hand, the accuracy of the TPWL model order reduction is limited because the information in the dominant bases of each local tangent subspace may be lost during the global SVD [18]. A method that can balance the accuracy and efficiency thereby is still a need.

## V. CONCLUSION

This paper reviews a number of recent advances from an aspect of the computational prototyping for design challenges of front-end analog/RF ICs in high-performance communication systems. We have discussed the existing researches on the EM-coupling, the non-Monte-Carlo mismatch analysis, and the nonlinear macromodeling for the system-level synthesis. A number of challenges are summarized for the future study.

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